

# 具有可调频率的 LM21212-2 2.95V 至 5.5V、12A、电压模式同步降压稳压器

## 1 特性

- 集成 7mΩ 高侧和 4.3mΩ 低侧 FET 开关
- 可通过电阻器在 300kHz 至 1.55MHz 范围内调节频率
- 可调输出电压范围为 0.6V 至  $V_{IN}$ （支持 100% 占空比），基准为  $\pm 1\%$
- 输入电压范围为 2.95V 至 5.5V
- 启动至预偏置负载
- 输出电压跟踪功能
- 高带宽电压环路误差放大器
- 可通过外部电容器进行可调软启动
- 具有迟滞功能的精密使能引脚
- 集成 OVP、OCP、OTP、UVLO 和电源正常状态
- 热增强型 20 引脚 HTSSOP 外露焊盘封装
- 使用 LM21212-2 并借助 WEBENCH® 电源设计器创建定制设计方案

## 2 应用

- 宽带、网络和无线通信
- 高性能 FPGA、ASIC 和微处理器
- 通过 5V 或 3.3V 总线实现轻松设计和高效负载点调节

## 3 说明

LM21212-2 是一款单片同步降压稳压器，能够提供高达 12A 的持续输出电流，同时以出色的效率产生低至 0.6V 的输出电压。该器件经过优化，可在 2.95V 至 5.5V 的输入电压范围内工作，因此适合各种低电压系统。电压模式控制环路可提供高噪声抗扰度和低占空比能力，并且可通过任何类型的输出电容补偿至稳定状态，从而提供最大的灵活度和易用性。

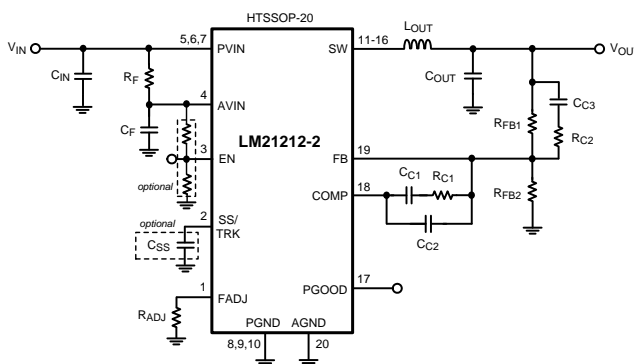
LM21212-2 具有内部过压保护 (OVP) 和过流保护 (OCP) 功能，可提高系统可靠性。精密使能引脚和集成 UVLO 支持对器件的打开进行严格的控制和定序。启动浪涌电流受内部固定和外部可调的软启动电路限制。借助集成电源正常状态电路，可实现故障检测和电源定序。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
LM21212-2	HTSSOP (20)	6.50mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 简化应用电路



## 目录

<b>1</b>	特性 .....	<b>1</b>	8.4	Device Functional Modes .....	<b>14</b>
<b>2</b>	应用 .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>15</b>
<b>3</b>	说明 .....	<b>1</b>	9.1	Application Information .....	<b>15</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	9.2	Typical Application .....	<b>15</b>
<b>5</b>	说明 (续) .....	<b>3</b>	<b>10</b>	<b>Layout</b> .....	<b>27</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>4</b>	10.1	Layout Considerations .....	<b>27</b>
<b>7</b>	<b>Specifications</b> .....	<b>5</b>	10.2	Layout Example .....	<b>27</b>
7.1	Absolute Maximum Ratings .....	<b>5</b>	10.3	Thermal Considerations .....	<b>28</b>
7.2	ESD Ratings .....	<b>5</b>	<b>11</b>	<b>器件和文档支持</b> .....	<b>30</b>
7.3	Recommended Operating Ratings .....	<b>5</b>	11.1	器件支持 .....	<b>30</b>
7.4	Electrical Characteristics .....	<b>5</b>	11.2	接收文档更新通知 .....	<b>30</b>
7.5	Typical Characteristics .....	<b>7</b>	11.3	社区资源 .....	<b>30</b>
<b>8</b>	<b>Detailed Description</b> .....	<b>10</b>	11.4	商标 .....	<b>30</b>
8.1	Overview .....	<b>10</b>	11.5	静电放电警告 .....	<b>30</b>
8.2	Functional Block Diagram .....	<b>10</b>	11.6	Glossary .....	<b>30</b>
8.3	Feature Description .....	<b>11</b>	<b>12</b>	<b>机械、封装和可订购信息</b> .....	<b>31</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision A (March 2013) to Revision B

**Page**

- 仅有编辑更改，无技术性修订；添加了 WEBENCH 链接 .....

**1**

### Changes from Original (March 2013) to Revision A

**Page**

- Changed layout of National Semiconductor data sheet to TI format .....

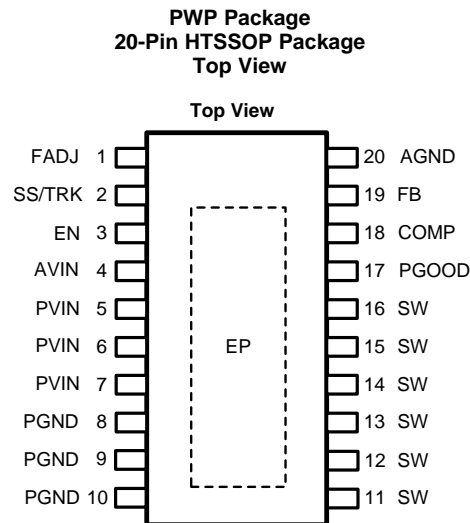
**4**

## 5 说明 (续)

LM21212-2 设计用于在多轨电源架构中良好运行。可使用 **SS/TRK** 引脚将该器件的输出电压配置为跟踪外部电压轨。可通过外部电阻器在 300kHz 至 1.55MHz 范围内对开关频率进行编程。

如果在启动时对输出进行预偏置，则不会灌入电流，从而使输出电压平稳上升，超过预偏置电压。该稳压器采用具有外露焊盘的 20 引脚 HTSSOP 封装，该焊盘可焊接至 PCB，因而无需大型散热装置。

## 6 Pin Configuration and Functions



### Pin Descriptions

PIN		
NO.	NAME	Description
1	FADJ	Frequency Adjust pin. The switching frequency can be set to a predetermined rate by connecting a resistor between FADJ and AGND.
2	SS/TRK	Soft-start control pin. An internal 2 $\mu$ A current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during startup. This pin can also be used to configure the tracking feature.
3	EN	Active high enable input for the device. If not used, the EN pin can be left open, which will go high due to an internal current source.
4	AVIN	Analog input voltage supply that generates the internal bias. It is recommended to connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry.
5,6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR input capacitance should be located as close as possible to these pins.
8,9,10	PGND	Power ground pins for the internal power switches.
11-16	SW	Switch node pins. These pins should be tied together locally and connected to the filter inductor.
17	PGOOD	Open-drain power good indicator.
18	COMP	Compensation pin is connected to the output of the voltage loop error amplifier.
19	FB	Feedback pin is connected to the inverting input of the voltage loop error amplifier.
20	AGND	Quiet analog ground for the internal reference and bias circuitry.
EP	Exposed Pad	Exposed metal pad on the underside of the package with an electrical and thermal connection to PGND. It is recommended to connect this pad to the PC board ground plane in order to improve thermal dissipation.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

See <sup>(1)(2)</sup>

PVIN <sup>(3)</sup> , AVIN to GND	-0.3V to +6V
SW <sup>(4)</sup> , EN, FB, COMP, PGOOD, SS/TRK, FADJ to GND	-0.3V to PVIN + 0.3V
Storage Temperature	-65°C to 150°C
Soldering Specification for TSSOP Pb-Free Infrared or Convection (30 sec)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the [Electrical Characteristics](#).
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The PVIN pin can tolerate transient voltages up to 6.5 V for a period of up to 6ns. These transients can occur during the normal operation of the device.
- (4) The SW pin can tolerate transient voltages up to 9 V for a period of up to 6 ns, and -1 V for a duration of 4 ns. These transients can occur during the normal operation of the device.

### 7.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Ratings

PVIN, AVIN to GND	+2.95V to +5.5V
Junction Temperature	-40°C to +125°C
θ <sub>JA</sub> <sup>(1)</sup>	24°C/W

- (1) Thermal measurements were performed on a 2x2 inch, 4 layer, 2 oz. copper outer layer, 1 oz.copper inner layer board with twelve 8 mil. vias underneath the EP of the device and an additional sixteen 8 mil. vias under the unexposed package.

### 7.4 Electrical Characteristics

Unless otherwise stated, the following conditions apply: V<sub>PVIN, AVIN</sub> = 5V. Limits in standard type are for T<sub>J</sub> = 25°C only, limits in **boldface type** apply over the junction temperature (T<sub>J</sub>) range of -40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>J</sub> = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SYSTEM</b>						
V <sub>FB</sub>	Feedback pin voltage	V <sub>IN</sub> = 2.95V to 5.5V	-1%	0.6	1%	V
ΔV <sub>OUT</sub> /ΔI <sub>OUT</sub>	Load Regulation			0.02		%V <sub>OUT</sub> / A
ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	Line Regulation			0.1		%V <sub>OUT</sub> / V
R <sub>DS(on) HS</sub>	High Side Switch On Resistance	I <sub>SW</sub> = 12A		7.0	<b>9.0</b>	mΩ
R <sub>DS(on) LS</sub>	Low Side Switch On Resistance	I <sub>SW</sub> = 12A		4.3	<b>6.0</b>	mΩ
I <sub>CLR</sub>	HS Rising Switch Current Limit		<b>15</b>	17	<b>19</b>	A
I <sub>CLF</sub>	LS Falling Switch Current Limit			12		A
V <sub>ZX</sub>	Zero Cross Voltage		-8	3	12	mV
I <sub>Q</sub>	Operating Quiescent Current			1.5	<b>3.0</b>	mA
I <sub>SD</sub>	Shutdown Quiescent Current	V <sub>EN</sub> = 0V		50	<b>70</b>	μA
V <sub>UVLO</sub>	AVIN Undervoltage Lockout	AVIN Rising	<b>2.45</b>	2.70	<b>2.95</b>	V
V <sub>UVLOHYS</sub>	AVIN Undervoltage Lockout Hysteresis		<b>140</b>	200	<b>280</b>	mV
V <sub>TRACKOS</sub>	SS/TRACK PIN accuracy (V <sub>SS</sub> - V <sub>FB</sub> )	0 < V <sub>TRACK</sub> < 0.55V	<b>-10</b>	6	<b>20</b>	mV
I <sub>SS</sub>	Soft-Start Pin Source Current		<b>1.3</b>	1.9	<b>2.5</b>	μA

## Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply:  $V_{PVIN, AVIN} = 5V$ . Limits in standard type are for  $T_J = 25^\circ C$  only, limits in **boldface type** apply over the junction temperature ( $T_J$ ) range of  $-40^\circ C$  to  $+125^\circ C$ . Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ C$ , and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{INTSS}$	Internal Soft-Start Ramp to Vref	$C_{SS} = 0$	<b>350</b>	500	<b>675</b>	$\mu s$
$t_{RESETSS}$	Device Reset to Soft-Start Ramp		<b>50</b>	110	<b>200</b>	$\mu s$
<b>OSCILLATOR</b>						
$f_{RNG}$	FADJ Frequency Range		<b>300</b>		<b>1550</b>	kHz
$f_{SW}$	Switching Frequency	$R_{ADJ} = 22.6k\Omega$	<b>1400</b>	1550	<b>1700</b>	kHz
		$R_{ADJ} = 95.3k\Omega$	<b>465</b>	500	<b>535</b>	
$t_{HSBLANK}$	HS OCP Blanking Time	Rising edge of SW to $I_{CLR}$ comparison		55		ns
$t_{LSBLANK}$	LS OCP Blanking Time	Falling edge of SW to $I_{CLF}$ comparison		400		ns
$t_{ZXBLANK}$	Zero Cross Blanking Time	Falling edge of SW to $V_{ZX}$ comparison		120		ns
$t_{MINON}$	Minimum HS on-time			140		ns
$\Delta V_{ramp}$	PWM Ramp p-p Voltage			0.8		V
<b>ERROR AMPLIFIER</b>						
$V_{OL}$	Error Amplifier Open Loop Voltage Gain	$I_{COMP} = -65\mu A$ to 1mA		95		dBV/V
GBW	Error Amplifier Gain-Bandwidth Product			11		MHz
$I_{FB}$	Feedback Pin Bias Current	$V_{FB} = 0.6V$		1		nA
$I_{COMPSRC}$	COMP Output Source Current			1		mA
$I_{COMPSINK}$	COMP Output Sink Current			65		$\mu A$
<b>POWERGOOD</b>						
$V_{OVP}$	Overvoltage Protection Rising Threshold	$V_{FB}$ Rising	<b>105</b>	112.5	<b>120</b>	$\%V_{FB}$
$V_{OVPHYS}$	Overvoltage Protection Hysteresis	$V_{FB}$ Falling		2		$\%V_{FB}$
$V_{UVP}$	Undervoltage Protection Rising Threshold	$V_{FB}$ Rising	<b>82</b>	90	<b>97</b>	$\%V_{FB}$
$V_{UVPHYS}$	Undervoltage Protection Hysteresis	$V_{FB}$ Falling		2.5		$\%V_{FB}$
$t_{PGDGL}$	PGOOD Deglitch Low (OVP/UVP Condition Duration to PGOOD Falling)			15		$\mu s$
$t_{PGDGH}$	PGOOD Deglitch High (minimum low pulse)			12		$\mu s$
$R_{PGOOD}$	PGOOD Pulldown Resistance		<b>10</b>	20	<b>40</b>	$\Omega$
$I_{PGOODLEAK}$	PGOOD Leakage Current	$V_{PGOOD} = 5V$		1		nA
<b>LOGIC</b>						
$V_{IHSYNC}$	SYNC Pin Logic High		2.0			V
$V_{ILSYNC}$	SYNC Pin Logic Low				0.8	V
$V_{IHENR}$	EN Pin Rising Threshold	$V_{EN}$ Rising	<b>1.20</b>	1.35	<b>1.45</b>	V
$V_{ENHYS}$	EN Pin Hysteresis		<b>50</b>	110	<b>180</b>	mV
$I_{EN}$	EN Pin Pullup Current	$V_{EN} = 0V$		2		$\mu A$
<b>THERMAL SHUTDOWN</b>						
$T_{THERMSD}$	Thermal Shutdown			165		$^\circ C$
$T_{THERMSDHYS}$	Thermal Shutdown Hysteresis			10		$^\circ C$

### 7.5 Typical Characteristics

Unless otherwise specified:  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $L = 0.56\text{ }\mu\text{H}$  ( $1.8\text{-m}\Omega\text{ }R_{DCR}$ ),  $C_{SS} = 33\text{ nF}$ ,  $f_{SW} = 500\text{ kHz}$  ( $R_{ADJ} = 95.3\text{ k}\Omega$ ),  $T_A = 25^\circ\text{C}$  for efficiency curves, loop gain plots and waveforms, and  $T_J = 25^\circ\text{C}$  for all others.

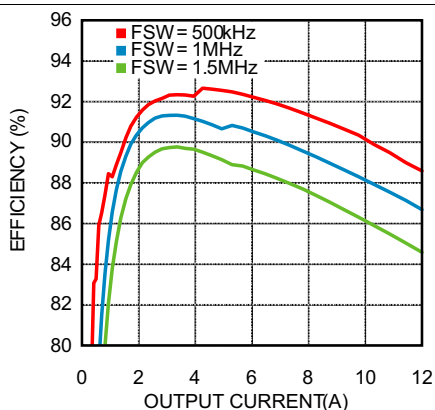


Figure 1. Efficiency

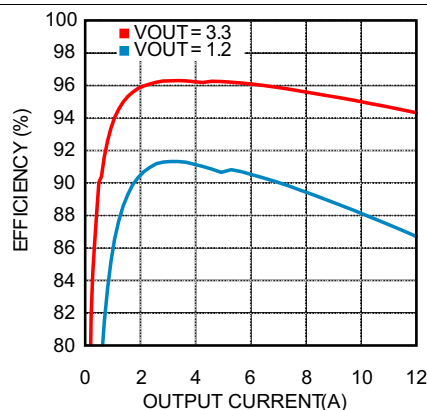


Figure 2. Efficiency

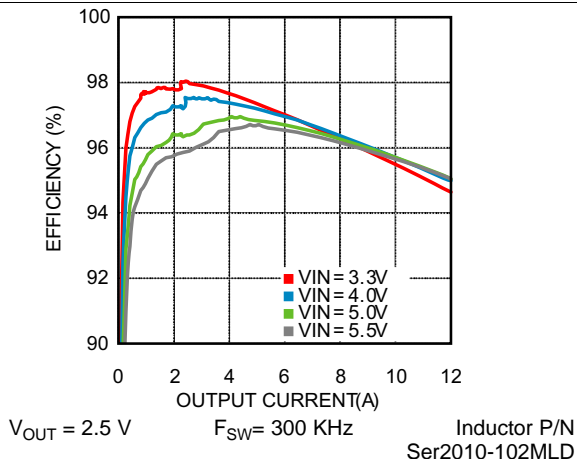


Figure 3. Efficiency

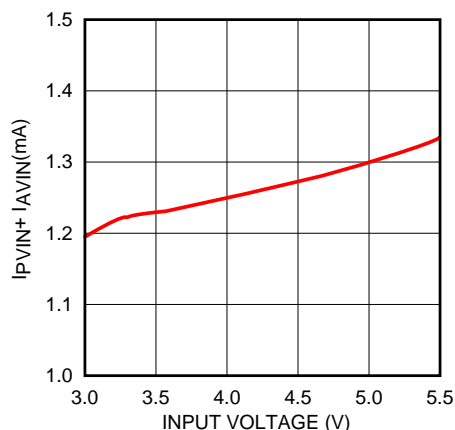


Figure 4. Non-Switching  $I_{QTOTAL}$  vs  $V_{IN}$

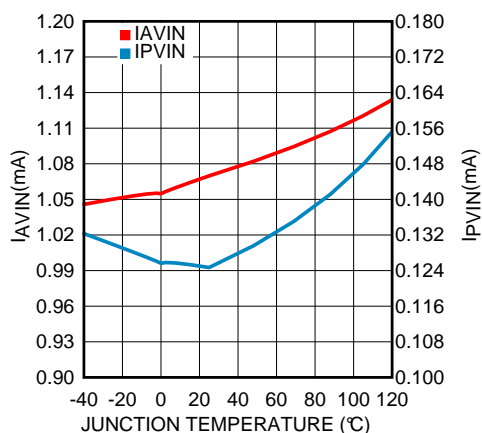


Figure 5. Non-Switching  $I_{AVIN}$  and  $I_{PVIN}$  vs Temperature

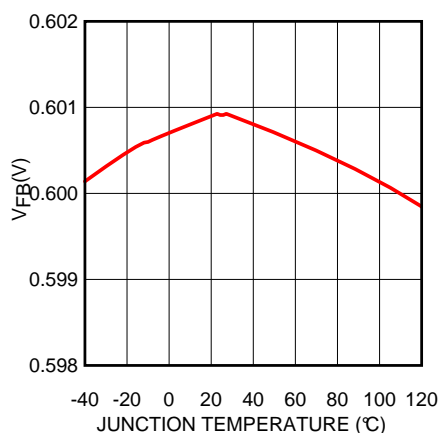


Figure 6.  $V_{FB}$  vs Temperature

### Typical Characteristics (continued)

Unless otherwise specified:  $V_{VIN} = 5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $L = 0.56\text{ }\mu\text{H}$  ( $1.8\text{-m}\Omega$   $R_{DCR}$ ),  $C_{SS} = 33\text{ nF}$ ,  $f_{SW} = 500\text{ kHz}$  ( $R_{ADJ} = 95.3\text{ k}\Omega$ ),  $T_A = 25^\circ\text{C}$  for efficiency curves, loop gain plots and waveforms, and  $T_J = 25^\circ\text{C}$  for all others.

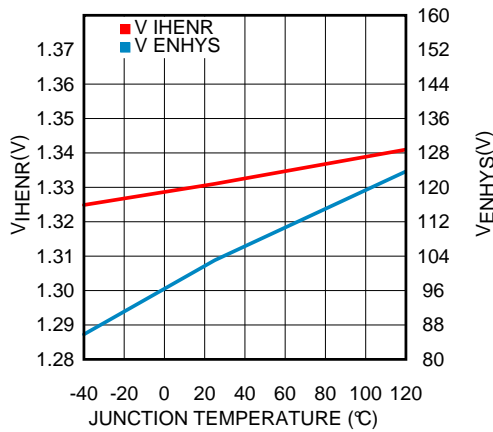


Figure 7. Enable Threshold and Hysteresis vs Temperature

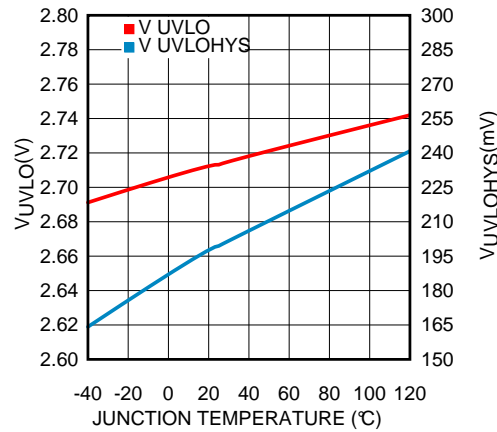


Figure 8. UVLO Threshold and Hysteresis vs Temperature

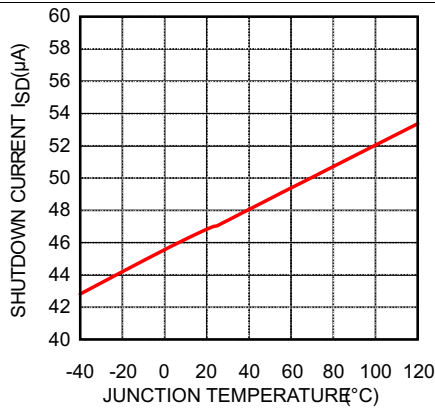


Figure 9. Enable Low Current vs Temperature

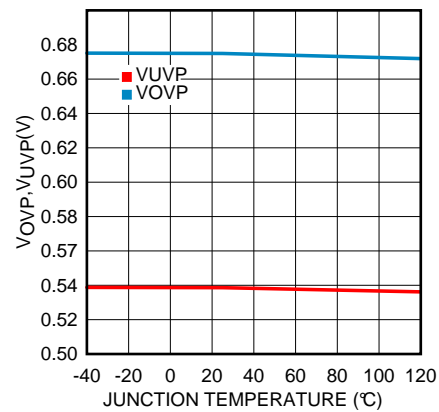


Figure 10. OVP/UVP Threshold vs Temperature

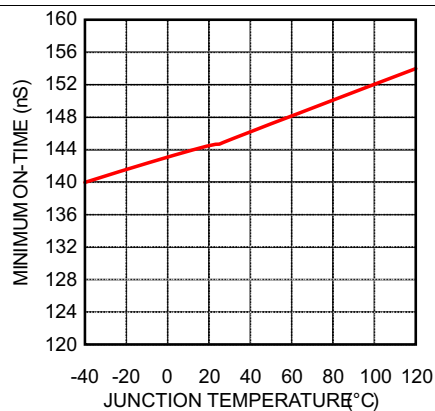


Figure 11. Minimum On-Time vs Temperature

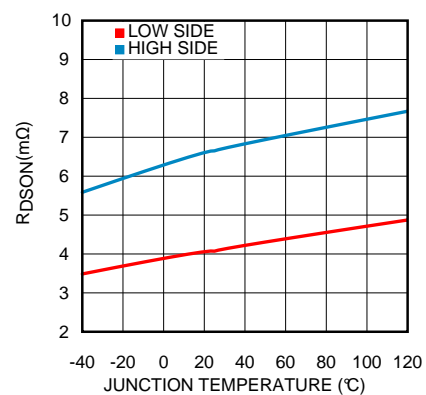


Figure 12. FET Resistance vs Temperature



Typical Characteristics (continued)

Unless otherwise specified:  $V_{VIN} = 5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $L = 0.56\text{ }\mu\text{H}$  ( $1.8\text{-m}\Omega\text{ }R_{DCR}$ ),  $C_{SS} = 33\text{ nF}$ ,  $f_{SW} = 500\text{ kHz}$  ( $R_{ADJ} = 95.3\text{ k}\Omega$ ),  $T_A = 25^\circ\text{C}$  for efficiency curves, loop gain plots and waveforms, and  $T_J = 25^\circ\text{C}$  for all others.

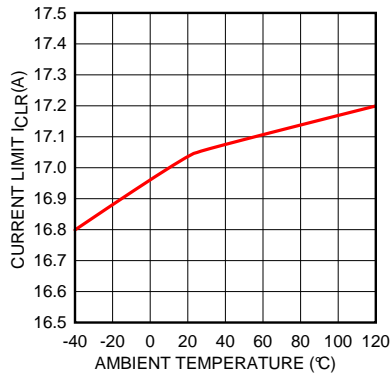
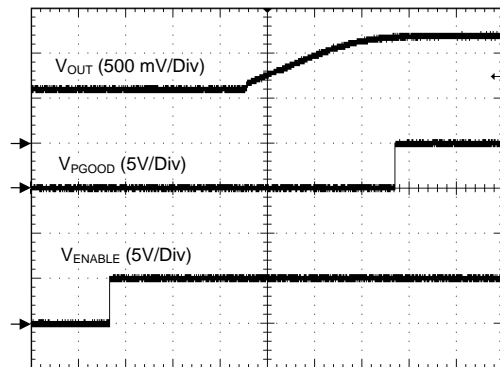
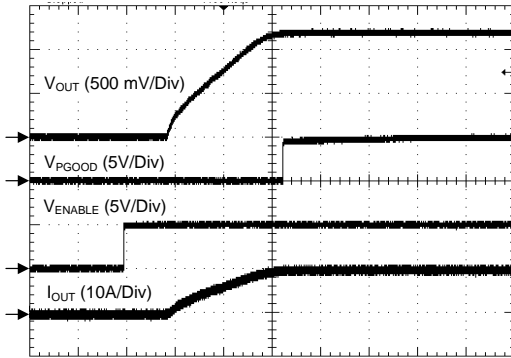


Figure 13. Peak Current Limit vs Temperature



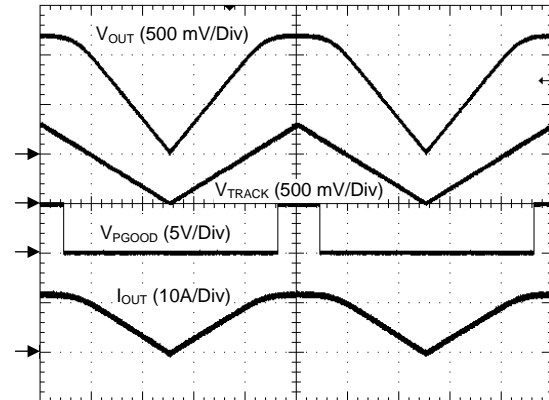
2 ms/DIV

Figure 14. Start-up With Prebiased Output



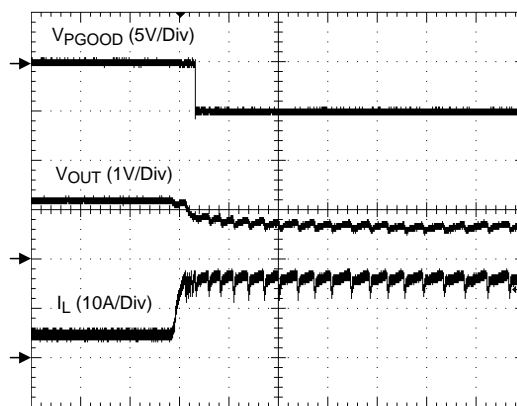
200  $\mu\text{s}$ /DIV

Figure 15. Start-up With SS/TRK Open Circuit



200 ms/DIV

Figure 16. Start-up With Applied Track Signal



10  $\mu\text{s}$ /DIV

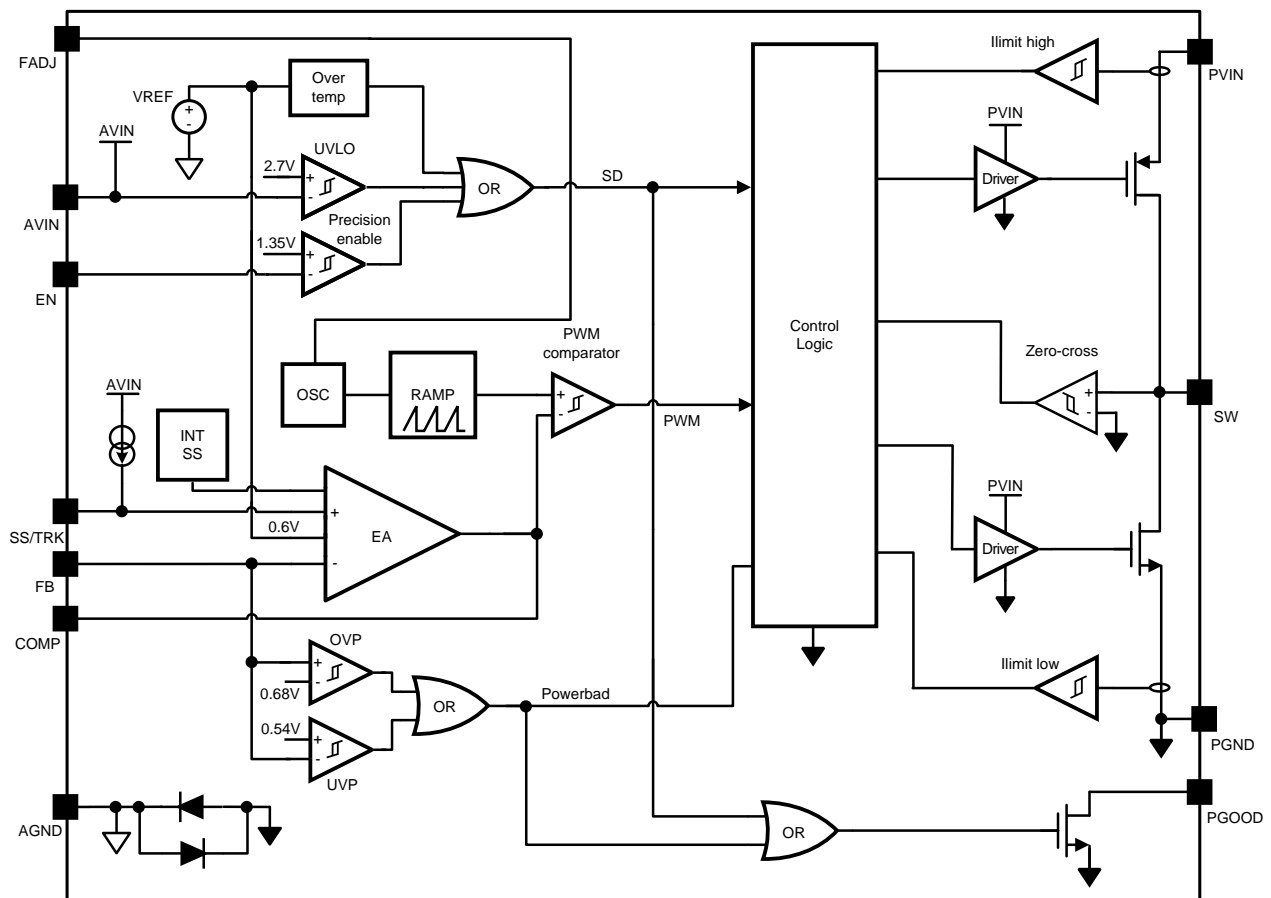
Figure 17. Output Overcurrent Condition

## 8 Detailed Description

### 8.1 Overview

The LM21212-2 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 12 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The device can operate at high switching frequency allowing use of a small inductor while still achieving high efficiency. The precision internal voltage reference allows the output to be set as low as 0.6 V. Fault protection features include: current limiting, thermal shutdown, overvoltage protection, and shutdown capability. The device is available in the 20-pin HTSSOP package featuring an exposed pad to aid thermal dissipation. The LM21212-2 can be used in numerous applications to efficiently step-down from a 5-V or 3.3-V bus.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Precision Enable

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.35V (typical). The EN pin has 110 mV of hysteresis and will disable the output when the enable voltage falls below 1.24 V (typical). If the EN pin is not used, it can be left open, and will be pulled high by an internal 2- $\mu$ A current source. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from VIN to configure the device to turn on at a precise input voltage.

### 8.3.2 UVLO

The LM21212-2 has a built-in undervoltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turnon point of the supply can be changed by using the precision enable pin and a resistor divider network connected to VIN as shown in [Figure 23](#) in the design guide.

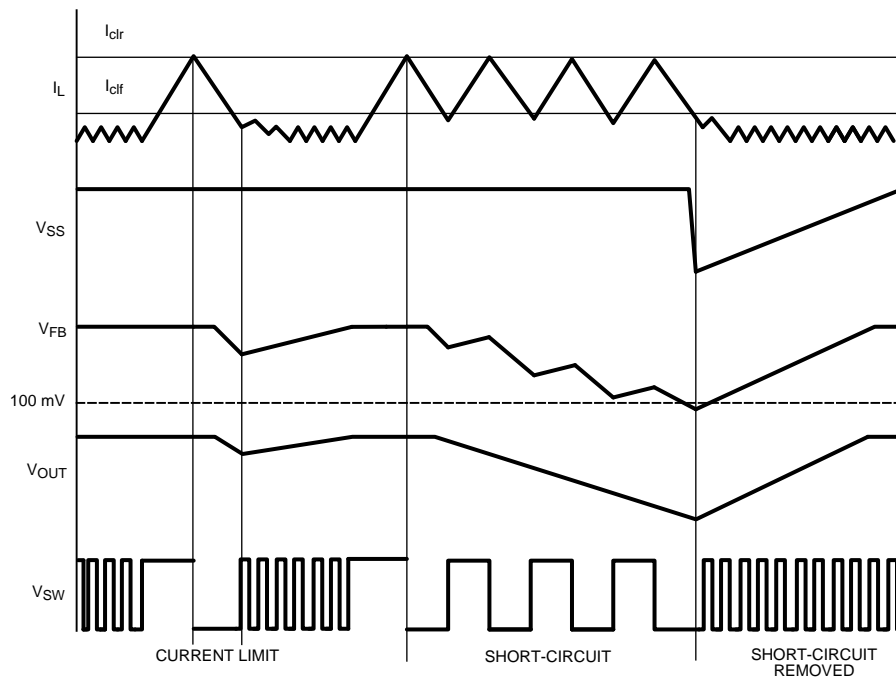
### 8.3.3 Current Limit

The LM21212-2 has current limit protection to avoid dangerous current levels on the power FETs and inductor. A current limit condition is met when the current through the high side FET exceeds the rising current limit level ( $I_{CLR}$ ). The control circuitry will respond to this event by turning off the high side FET and turning on the low side FET. This forces a negative voltage on the inductor, thereby causing the inductor current to decrease. The high-side FET does not conduct again until the lower current limit level ( $I_{CLF}$ ) is sensed on the low side FET. At this point, the device resumes normal switching.

A current limit condition will cause the internal soft-start voltage to ramp downward. After the internal soft-start ramps below the feedback (FB) pin voltage, (nominally 0.6 V), FB begins to ramp downward, as well. This voltage foldback limits the power consumption in the device, thereby protecting the device from continuously supplying power to the load under a condition that does not fall within the device SOA. After the current limit condition is cleared, the internal soft-start voltage will ramp up again. [Figure 18](#) shows current limit behavior with  $V_{SS}$ ,  $V_{FB}$ ,  $V_{OUT}$  and  $V_{SW}$ .

### 8.3.4 Short-Circuit Protection

In the unfortunate event that the output is shorted with a low impedance to ground, the LM21212-2 will limit the current into the short by resetting the device. A short-circuit condition is sensed by a current-limit condition coinciding with a voltage on the FB pin that is lower than 100 mV. When this condition occurs, the device will begin its reset sequence, turning off both power FETs and discharging the soft-start capacitor after  $t_{RESETSS}$  (nominally 110  $\mu$ s). The device will then attempt to restart. If the short-circuit condition still exists, it will reset again, and repeat until the short-circuit is cleared. The reset prevents excess current flowing through the FETs in a highly inefficient manner, potentially causing thermal damage to the device or the bus supply.

**Feature Description (continued)**

**Figure 18. Current Limit Conditions**
**8.3.5 Thermal Protection**

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the LM21212-2 tri-states the power FETs and resets soft start. After the junction cools to approximately 155°C, the device starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating. Note that thermal limit will not stop the die from operating above the specified operating maximum temperature, 125°C. The die should be kept under 125°C to ensure correct operation.

**8.3.6 Power-Good Flag**

The PGOOD pin provides the user with a way to monitor the status of the LM21212-2. In order to use the PGOOD pin, the application must provide a pullup resistor to a desired DC voltage (in other words,  $V_{IN}$ ). PGOOD responds to a fault condition by pulling the PGOOD pin low with the open-drain output. PGOOD will pull low on the following conditions – 1)  $V_{FB}$  moves above or below the  $V_{OVP}$  or  $V_{UVP}$ , respectively 2) The enable pin is brought below the enable threshold 3) The device enters a prebiased output condition ( $V_{FB} > V_{SS}$ ).

Figure 19 shows the conditions that will cause PGOOD to fall.

Feature Description (continued)

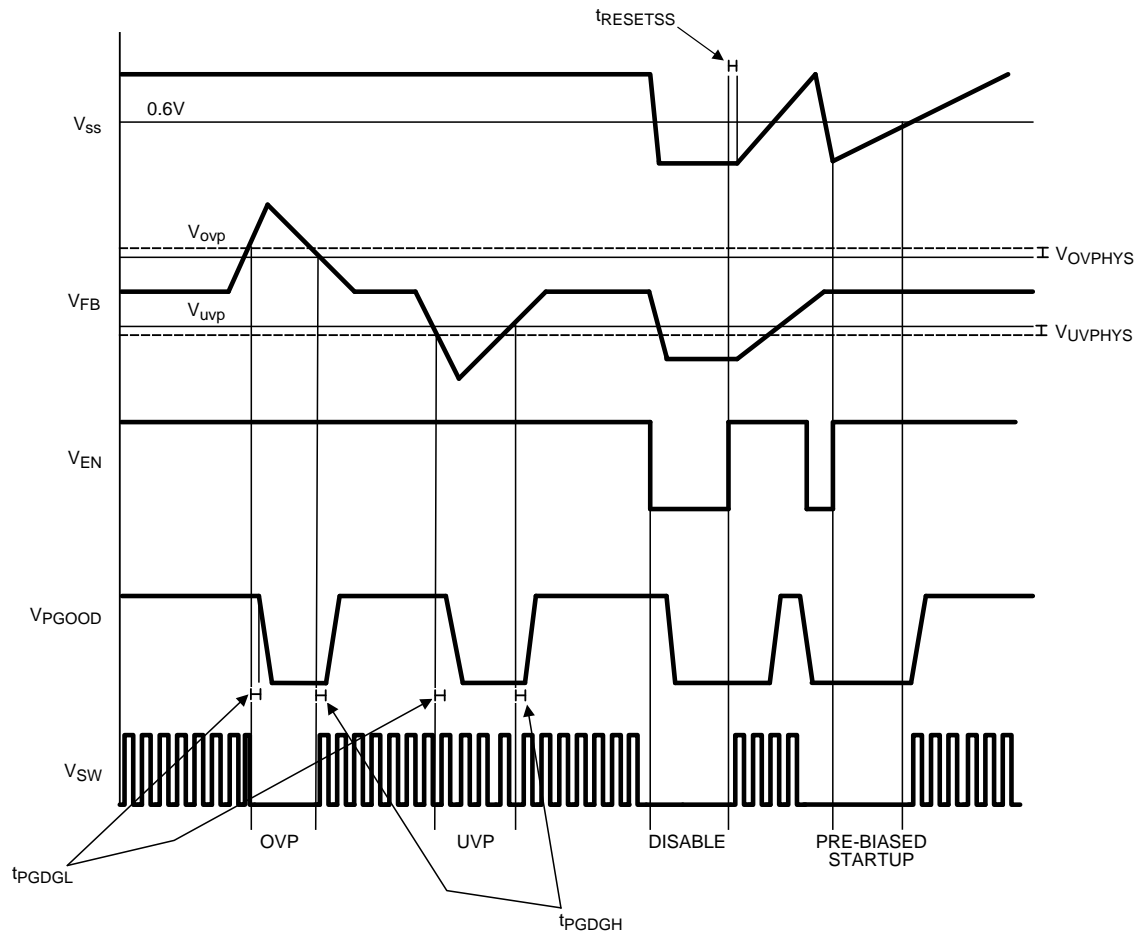


Figure 19. PGOOD Conditions

8.3.7 Light Load Operation

The LM21212-2 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak-to-peak inductor ripple current is greater than two times the load current, the device will enter the diode emulation mode preventing significant negative inductor current. The output current at which this occurs is the critical conduction boundary and can be calculated by Equation 1:

$$I_{\text{BOUNDARY}} = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times D}{2 \times L \times f_{\text{SW}}} \tag{1}$$

It can be seen that in diode emulation mode, whenever the inductor current reaches zero the SW node becomes high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground.

At very light loads, usually below 500 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

### 8.4 Device Functional Modes

Several diagrams are shown in Figure 20 illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.

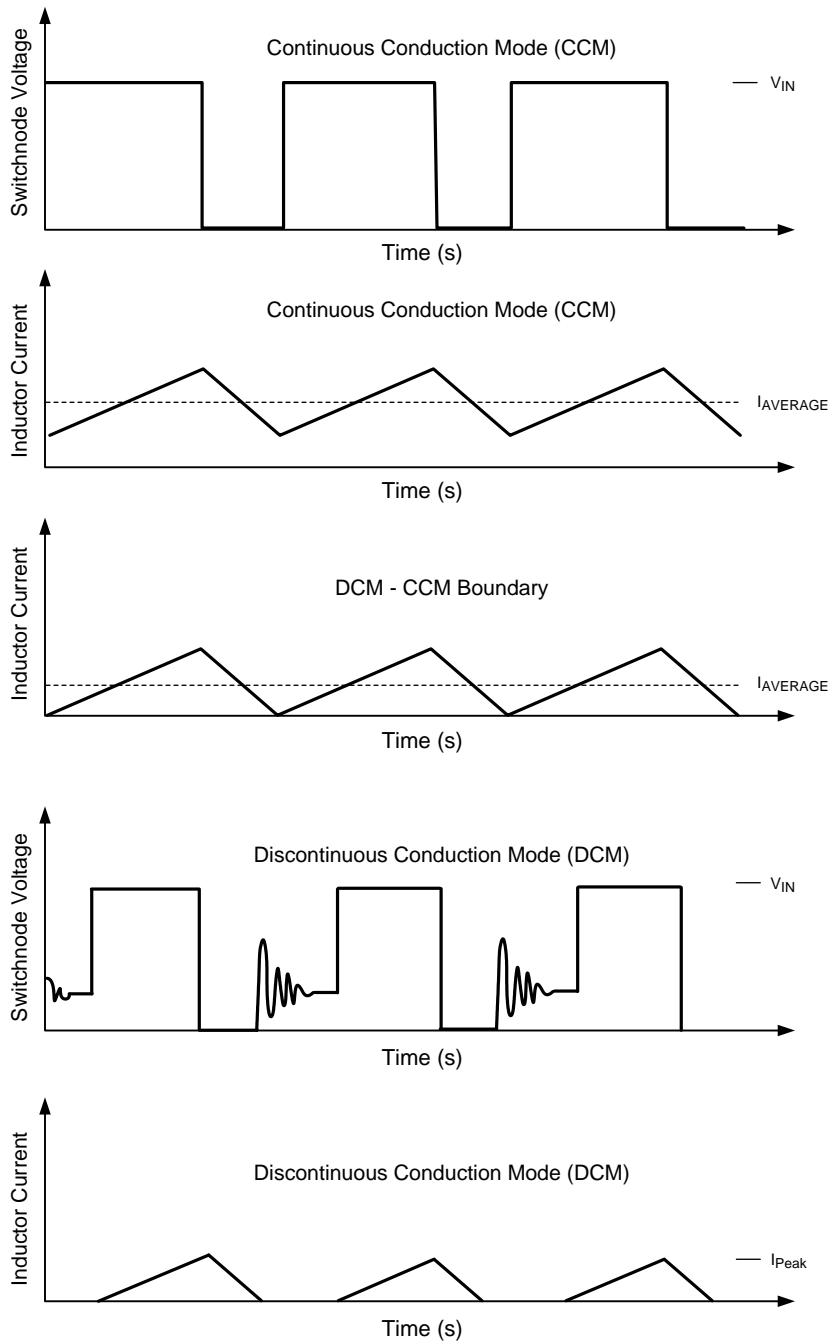


Figure 20. Modes Of Operation for LM21212-2

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LM21212-2 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy-to-use regulator features two integrated switches and is capable of supplying up to 12 A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The device can operate at high switching frequency allowing use of a small inductor while still achieving high efficiency.

### 9.2 Typical Application

#### 9.2.1 Typical Application 1

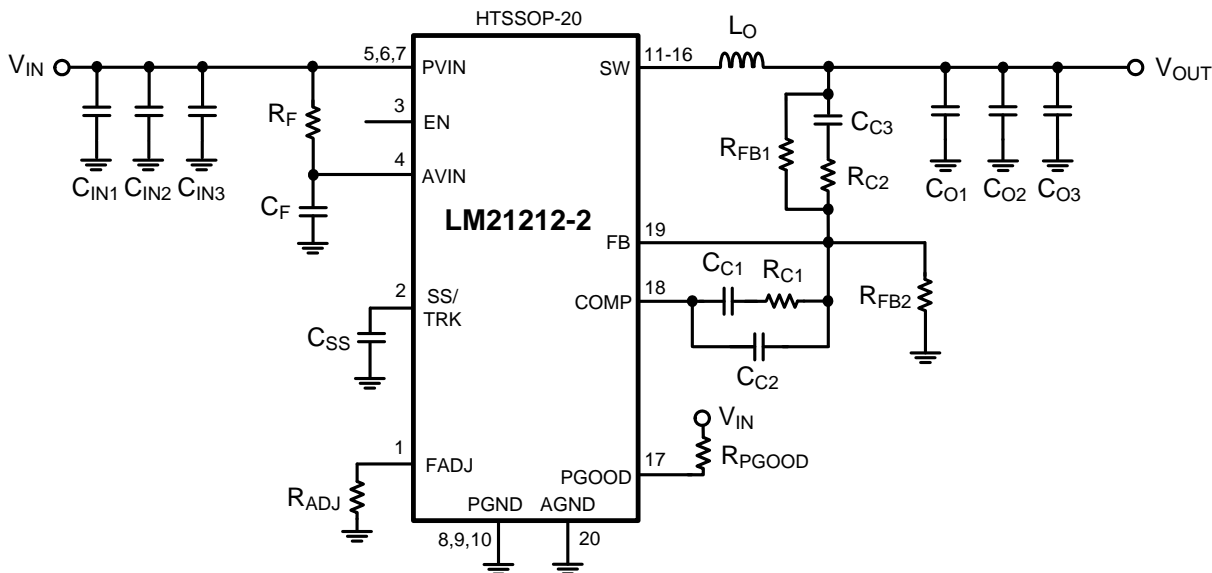


Figure 21. Typical Application Schematic 1

## Typical Application (continued)

### 9.2.1.1 Design Requirements

**Table 1. Bill Of Materials ( $V_{IN} = 3.3\text{ V} - 5.5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ ,  $I_{OUT} = 12\text{ A}$ ,  $F_{SW} = 500\text{ kHz}$ )**

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C <sub>F</sub>	CAP, CERM, 1 uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C <sub>IN1</sub> , C <sub>IN2</sub> , C <sub>IN3</sub> , C <sub>O1</sub> , C <sub>O2</sub> , C <sub>O3</sub>	CAP, CERM, 100 uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C <sub>C1</sub>	CAP, CERM, 1800 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H182J	1
C <sub>C2</sub>	CAP, CERM, 68 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C <sub>C3</sub>	CAP, CERM, 820 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C <sub>SS</sub>	CAP, CERM, 0.033 uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L <sub>O</sub>	Inductor, Shielded Drum Core, Powdered Iron, 560nH, 27.5A, 0.0018 ohm, SMD	Vishay-Dale	IHLP4040DZERR56M01	1
R <sub>F</sub>	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R <sub>C1</sub>	RES, 9.31 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06039K31FKEA	1
R <sub>C2</sub>	RES, 165 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165RFKEA	1
R <sub>FB1</sub> , R <sub>FB2</sub> , R <sub>PGOOD</sub>	RES, 10 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R <sub>ADJ</sub>	RES, 95.3 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060395K3FKEA	1

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM21212-2 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

#### 9.2.1.2.2 Output Voltage

The first step in designing the LM21212-2 application is setting the output voltage. This is done by using a voltage divider between  $V_{OUT}$  and AGND, with the middle node connected to  $V_{FB}$ . When operating under steady-state conditions, the LM21212-2 will force  $V_{OUT}$  such that  $V_{FB}$  is driven to 0.6 V.



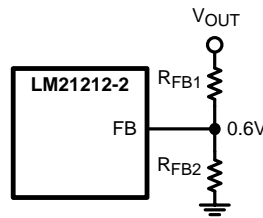


Figure 22. Setting  $V_{OUT}$

A good starting point for the lower feedback resistor,  $R_{FB2}$ , is 10k $\Omega$ .  $R_{FB1}$  can then be calculated the following equation:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} 0.6V \quad (2)$$

### 9.2.1.2.3 Precision Enable

The enable (EN) pin of the LM21212-2 allows the output to be toggled on and off. This pin is a precision analog input. When the voltage exceeds 1.35V, the controller will try to regulate the output voltage as long as the input voltage has exceeded the UVLO voltage of 2.70V. There is an internal current source connected to EN so if enable is not used, the device will turn on automatically. If EN is not toggled directly the device can be preprogrammed to turn on at a certain input voltage higher than the UVLO voltage. This can be done with an external resistor divider from AVIN to EN and EN to AGND as shown below in Figure 23.

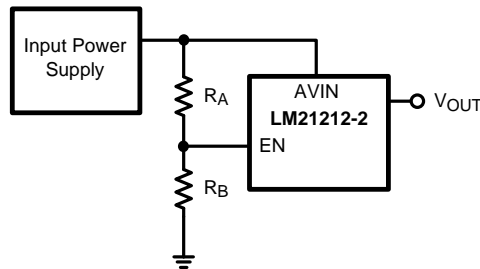


Figure 23. Enable Start-up Through  $V_{IN}$

The resistor values of  $R_A$  and  $R_B$  can be relatively sized to allow EN to reach the enable threshold voltage depending on the input supply voltage. With the enable current source accounted for, the equation solving for  $R_A$  is shown below:

$$R_A = \frac{R_B(V_{PVIN} - 1.35V)}{1.35V - I_{EN}R_B} \quad (3)$$

In the Equation 3  $R_A$  is the resistor from  $V_{IN}$  to enable,  $R_B$  is the resistor from enable to ground,  $I_{EN}$  is the internal enable pullup current (2  $\mu$ A) and 1.35 V is the fixed precision enable threshold voltage. Typical values for  $R_B$  range from 10 k $\Omega$  to 100 k $\Omega$ .

### 9.2.1.2.4 Soft Start

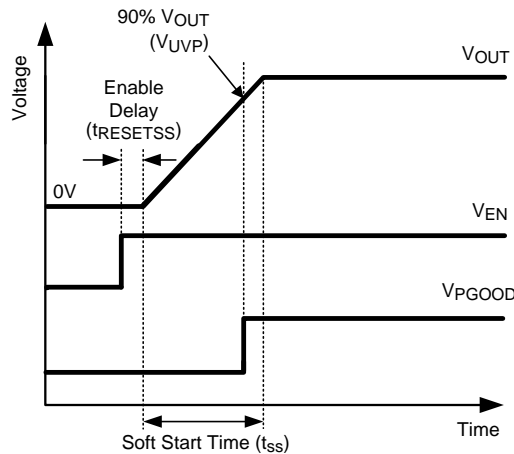
When EN has exceeded 1.35 V, and both PVIN and AVIN have exceeded the UVLO threshold, the LM21212-2 begins charging the output linearly to the voltage level dictated by the feedback resistor network. The LM21212-2 has a user adjustable soft-start circuit to lengthen the charging time of the output set by a capacitor from the soft start pin to ground. After enable exceeds 1.35 V, an internal 2- $\mu$ A current source begins to charge the soft start capacitor. This allows the user to limit inrush currents due to a high output capacitance and not cause an over current condition. Adding a soft-start capacitor can also reduce the stress on the input rail. Larger capacitor values will result in longer start-up times. Use the equation below to approximate the size of the soft-start capacitor:

$$\frac{t_{SS} \times I_{SS}}{0.6V} = C_{SS}$$

where

- $I_{SS}$  is nominally 2  $\mu A$
- $t_{SS}$  is the desired start-up time (4)

If  $V_{IN}$  is higher than the UVLO level and enable is toggled high the soft start sequence will begin. There is a small delay between enable transitioning high and the beginning of the soft-start sequence. This delay allows the LM21212-2 to initialize its internal circuitry. Once the output has charged to 90% of the nominal output voltage the power-good flag will transition high. This behavior is illustrated in Figure 24.



**Figure 24. Soft Start Timing**

As shown above, the size of the capacitor is influenced by the nominal feedback voltage level 0.6 V, the soft-start charging current  $I_{SS}$  (2  $\mu A$ ), and the desired soft start time. If no soft-start capacitor is used then the LM21212-2 defaults to a minimum startup time of 500  $\mu s$ . The LM21212-2 will not start up faster than 500  $\mu s$ . When enable is cycled or the device enters UVLO, the charge developed on the soft-start capacitor is discharged to reset the startup process. This also happens when the device enters short circuit mode from an overcurrent event.

**9.2.1.2.5 Resistor-Adjustable Frequency**

The frequency adjust (FADJ) pin allows the LM21212-2 to be programmed to a predetermined switching frequency between 300 kHz to 1.55 MHz by connecting a resistor between FADJ and AGND. To determine the resistor ( $R_{ADJ}$ ) value for a desired frequency, the following equation can be used:

$$R_{ADJ} = \frac{54680}{f_{SW}} - 13.15$$

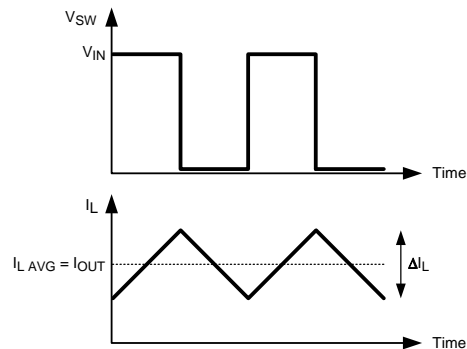
where

- $R_{ADJ}$  is resistance in k $\Omega$
- $f_{SW}$  is frequency in kHz (5)

The desired frequency must fall within the operational frequency range, 300 kHz to 1550 kHz, and a corresponding resistor must be used for normal operation.

**9.2.1.2.6 Inductor Selection**

The inductor (L) used in the application will influence the ripple current and the efficiency of the system. The first selection criteria is to define a ripple current,  $\Delta I_L$ . In a buck converter, it is typically selected to run between 20% to 30% of the maximum output current. Figure 25 shows the ripple current in a standard buck converter operating in continuous conduction mode. Larger ripple current results in a smaller inductance value, which will lead to lower inductor series resistance, and improved efficiency. However, larger ripple current will also cause the device to operate in discontinuous conduction mode at a higher average output current.


**Figure 25. Switch And Inductor Current Waveforms**

Once the ripple current has been determined, the appropriate inductor size can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{\Delta I_L \cdot f_{SW}} \quad (6)$$

#### 9.2.1.2.7 Output Capacitor Selection

The output capacitor,  $C_{OUT}$ , filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM21212-2 that provide various advantages. The best performance is typically obtained using ceramic, SP or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the following formula:

$$\Delta V_{OUT} \approx \Delta I_L \times \left[ R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right]$$

where

- $\Delta V_{OUT}$  (V) is the amount of peak to peak voltage ripple at the power supply output
  - $R_{ESR}$  ( $\Omega$ ) is the series resistance of the output capacitor
  - $f_{SW}$  (Hz) is the switching frequency
  - $C_{OUT}$  (F) is the output capacitance used in the design
- (7)

The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using the following equation:

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

where

- $C_{OUT}$  (F) is the minimum required output capacitance
- $L$  (H) is the value of the inductor
- $V_{DROOP}$  (V) is the output voltage drop ignoring loop bandwidth considerations

- $\Delta I_{\text{OUTSTEP}}$  (A) is the load step change
  - $R_{\text{ESR}}$  ( $\Omega$ ) is the output capacitor ESR
  - $V_{\text{IN}}$  (V) is the input voltage
  - $V_{\text{OUT}}$  (V) is the set regulator output voltage
- (8)

Both the tolerance and voltage coefficient of the capacitor must be examined when designing for a specific output ripple or transient droop target.

#### 9.2.1.2.8 Input Capacitor Selection

Quality input capacitors are necessary to limit the ripple voltage at the PVIN pin while supplying most of the switch current during the on-time. Additionally, they help minimize input voltage droop in an output current transient condition. In general, it is recommended to use a ceramic capacitor for the input as it provides both a low impedance and small footprint. Use of a high-grade dielectric for the ceramic capacitor, such as X5R or X7R, will provide improved performance over temperature and also minimize the DC voltage derating that occurs with Y5V capacitors. The input capacitors should be placed as close as possible to the PVIN and PGND pins.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{\text{IN-RMS}} = I_{\text{OUT}} \sqrt{D(1 - D)} \quad (9)$$

As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, place low ESR ceramic capacitors in parallel with higher capacitance capacitors to provide the best input filtering for the device.

When operating at low input voltages (3.3 V or lower), additional capacitance may be necessary to protect from triggering an under-voltage condition on an output current transient. This will depend on the impedance between the input voltage supply and the LM21212-2, as well as the magnitude and slew rate of the output transient.

The AVIN pin requires a 1- $\mu\text{F}$  ceramic capacitor to AGND and a 1- $\Omega$  resistor to PVIN. This RC network filter inherent noise on PVIN from the sensitive analog circuitry connected to AVIN.

#### 9.2.1.2.9 Control Loop Compensation

The LM21212-2 incorporates a high bandwidth amplifier between the FB and COMP pins to allow the user to design a compensation network that matches the application. This section will walk through the various steps in obtaining the open loop transfer function.

There are three main blocks of a voltage mode buck switcher that the power supply designer must consider when designing the control system; the power train, modulator, and the compensated error amplifier. A closed loop diagram is shown in [Figure 26](#).

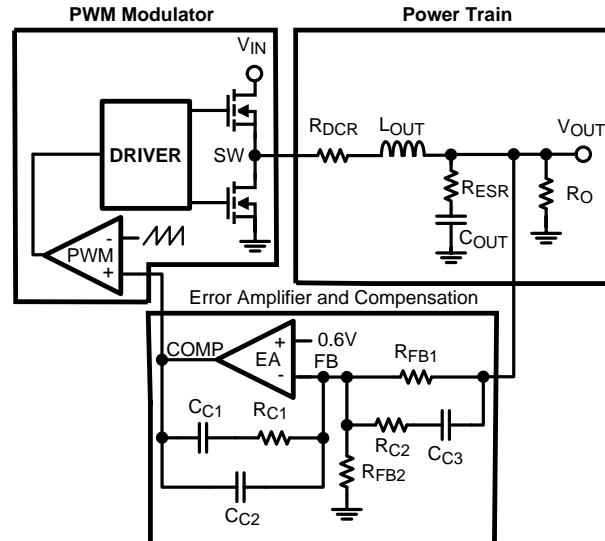


Figure 26. Loop Diagram

The power train consists of the output inductor (L) with DCR (DC resistance  $R_{DCR}$ ), output capacitor ( $C_0$ ) with ESR (effective series resistance  $R_{ESR}$ ), and load resistance ( $R_0$ ). The error amplifier (EA) constantly forces FB to 0.6 V. The passive compensation components around the error amplifier help maintain system stability. The modulator creates the duty cycle by comparing the error amplifier signal with an internally generated ramp set at the switching frequency.

There are three transfer functions that must be taken into consideration when obtaining the total open loop transfer function; COMP to SW (modulator) , SW to  $V_{OUT}$  (power train), and  $V_{OUT}$  to COMP (error amplifier). The COMP to SW transfer function is simply the gain of the PWM modulator.

$$G_{PWM} = \frac{V_{in}}{\Delta V_{ramp}}$$

where

- $\Delta V_{RAMP}$  is the oscillator peak-to-peak ramp voltage (nominally 0.8 V) (10)

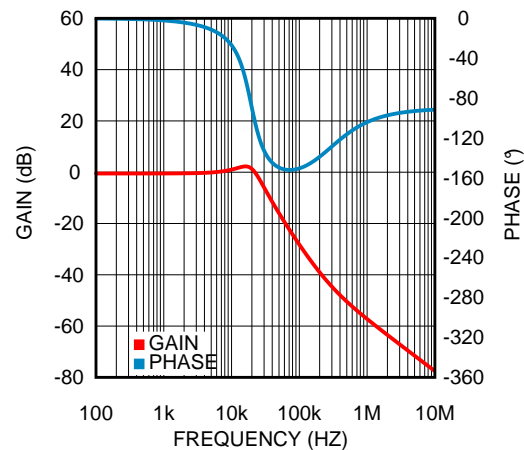
The SW-to-COMP transfer function includes the output inductor, output capacitor, and output load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi} \sqrt{\frac{R_0 + R_{DCR}}{L_{OUT}C_{OUT}(R_0 + R_{ESR})}} \quad (11)$$

In addition to two complex poles, a left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{ESR} = \frac{1}{2\pi C_{OUT}R_{ESR}} \quad (12)$$

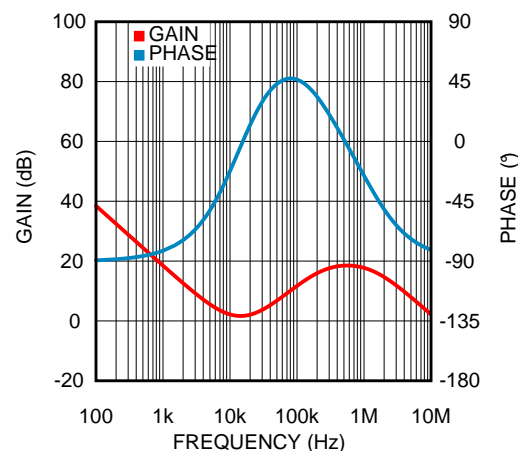
A Bode plot showing the power train response is shown in [Figure 27](#)


**Figure 27. Power Train Bode Plot**

The complex poles created by the output inductor and capacitor cause a 180° phase shift at the resonant frequency as seen in [Figure 27](#). The phase is boosted back up to -90° because of the output capacitor ESR zero. The 180° phase shift must be compensated out and phase boosted through the error amplifier to stabilize the closed loop response. The compensation network shown around the error amplifier in [Figure 26](#) creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies will stabilize the closed loop response. The Compensated Error Amplifier transfer function is:

$$G_{EA} = K_m \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \quad (13)$$

The pole located at the origin gives high open loop gain at DC, translating into improved load regulation accuracy. This pole occurs at a very low frequency due to the limited gain of the error amplifier; however, it can be approximated at DC for the purposes of compensation. The other two poles and two zeros can be located accordingly to stabilize the voltage mode loop depending on the power stage complex poles and Q. [Figure 28](#) is an illustration of what the Error Amplifier Compensation transfer function will look like.


**Figure 28. Type 3 Compensation Network Bode Plot**

As seen in [Figure 28](#), the two zeros ( $f_{LC}/2$ ,  $f_{LC}$ ) in the compensation network give a phase boost. This will cancel out the effects of the phase loss from the output filter. The compensation network also adds two poles to the system. One pole should be located at the zero caused by the output capacitor ESR ( $f_{ESR}$ ) and the other pole should be at half the switching frequency ( $f_{SW}/2$ ) to roll off the high frequency response. The dependency of the pole and zero locations on the compensation components is described below.

$$\begin{aligned}
 f_{Z1} &= \frac{f_{LC}}{2} = \frac{1}{2\pi R_{C1} C_{C1}} \\
 f_{Z2} &= f_{LC} = \frac{1}{2\pi(R_{C1} + R_{FB1})C_{C3}} \\
 f_{P1} &= f_{ESR} = \frac{1}{2\pi R_{C2} C_{C3}} \\
 f_{P2} &= \frac{f_{SW}}{2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}}
 \end{aligned}
 \tag{14}$$

An example of the step-by-step procedure to generate compensation component values using the typical application setup (see [Figure 21](#)) is given. The parameters needed for the compensation values are given in the table below.

PARAMETER	VALUE
$V_{IN}$	5 V
$V_{OUT}$	1.2 V
$I_{OUT}$	12 A
$f_{CROSSOVER}$	100 kHz
L	0.56 $\mu$ H
$R_{DCR}$	1.8 m $\Omega$
$C_O$	150 $\mu$ F
$R_{ESR}$	1 m $\Omega$
$\Delta V_{RAMP}$	0.8 V
$f_{SW}$	500 kHz

where  $\Delta V_{RAMP}$  is the oscillator peak-to-peak ramp voltage (nominally 0.8V), and  $f_{CROSSOVER}$  is the frequency at which the open-loop gain is a magnitude of 1. It is recommended that the  $f_{crossover}$  not exceed one-fifth of the switching frequency. The output capacitance,  $C_O$ , depends on capacitor chemistry and bias voltage. For Multi-Layer Ceramic Capacitors (MLCC), the total capacitance will degrade as the DC bias voltage is increased. Measuring the actual capacitance value for the output capacitors at the output voltage is recommended to accurately calculate the compensation network. The example given here is the total output capacitance using the three MLCC output capacitors biased at 1.2V, as seen in the typical application schematic, . Note that it is more conservative, from a stability standpoint, to err on the side of a smaller output capacitance value in the compensation calculations rather than a larger, as this will result in a lower bandwidth but increased phase margin.

First, a the value of  $R_{FB1}$  should be chosen. A typical value is 10 k $\Omega$ . From this, the value of  $R_{C1}$  can be calculated to set the mid-band gain so that the desired crossover frequency is achieved:

$$\begin{aligned}
 R_{C1} &= \frac{f_{CROSSOVER}}{f_{LC}} \cdot \frac{\Delta V_{RAMP}}{V_{IN}} \cdot R_{FB1} \\
 &= \frac{100 \text{ kHz}}{17.4 \text{ kHz}} \frac{0.8 \text{ V}}{5.0 \text{ V}} 10 \text{ k}\Omega \\
 &= 9.2 \text{ k}\Omega
 \end{aligned}
 \tag{15}$$

Next, the value of  $C_{C1}$  can be calculated by placing a zero at half of the LC double pole frequency ( $f_{LC}$ ):

$$\begin{aligned}
 C_{C1} &= \frac{1}{\pi f_{LC} R_{C1}} \\
 &= 1.99 \text{ nF}
 \end{aligned}
 \tag{16}$$

Now the value of  $C_{C2}$  can be calculated to place a pole at half of the switching frequency ( $f_{SW}$ ):

$$\begin{aligned}
 C_{C2} &= \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1} \\
 &= 71 \text{ pF}
 \end{aligned}
 \tag{17}$$

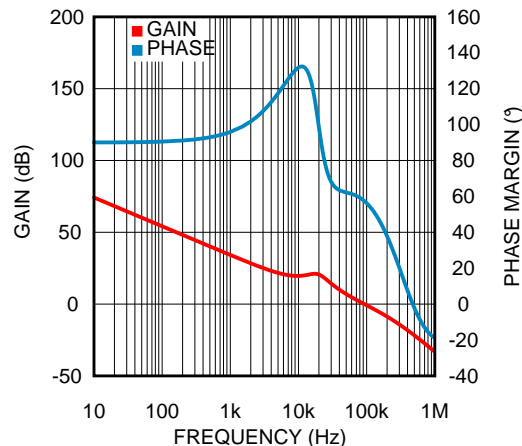
$R_{C2}$  can then be calculated to set the second zero at the LC double pole frequency:

$$\begin{aligned}
 R_{C2} &= \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}} \\
 &= 166 \Omega
 \end{aligned}
 \tag{18}$$

Last,  $C_{C3}$  can be calculated to place a pole at the same frequency as the zero created by the output capacitor ESR:

$$\begin{aligned}
 C_{C3} &= \frac{1}{2\pi f_{ESR} R_{C2}} \\
 &= 898 \text{ pF}
 \end{aligned}
 \tag{19}$$

An illustration of the total loop response can be seen in [Figure 29](#).



**Figure 29. Loop Response**

It is important to verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between  $45^\circ$  and  $70^\circ$  is usually desired for voltage mode systems. Excessive phase margin can cause slow system response to load transients and low phase margin may cause an oscillatory load transient response. If the load step response peak deviation is larger than desired, increasing  $f_{CROSSOVER}$  and recalculating the compensation components may help but usually at the expense of phase margin.



9.2.1.3 Application Curves

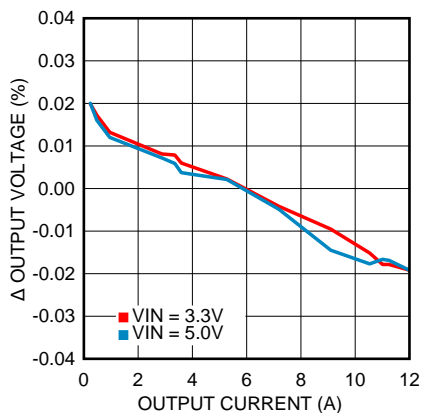


Figure 30. Load Regulation

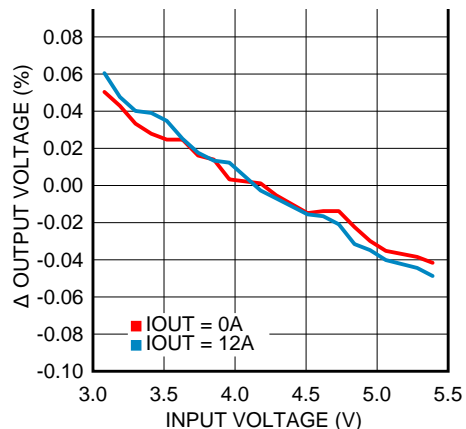


Figure 31. Line Regulation

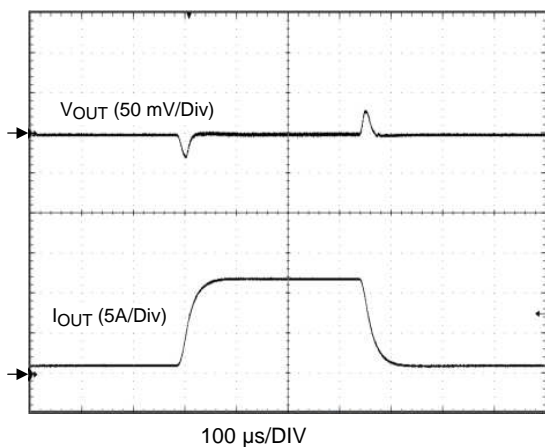


Figure 32. Load Transient Response ( $F_{SW} = 650 \text{ kHz}$ )

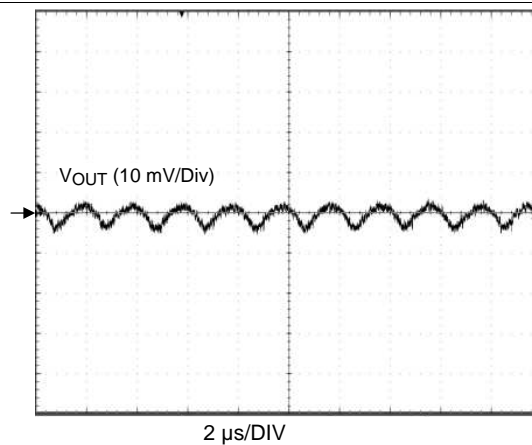


Figure 33. Output Voltage Ripple

### 9.2.2 Typical Application Schematic 2

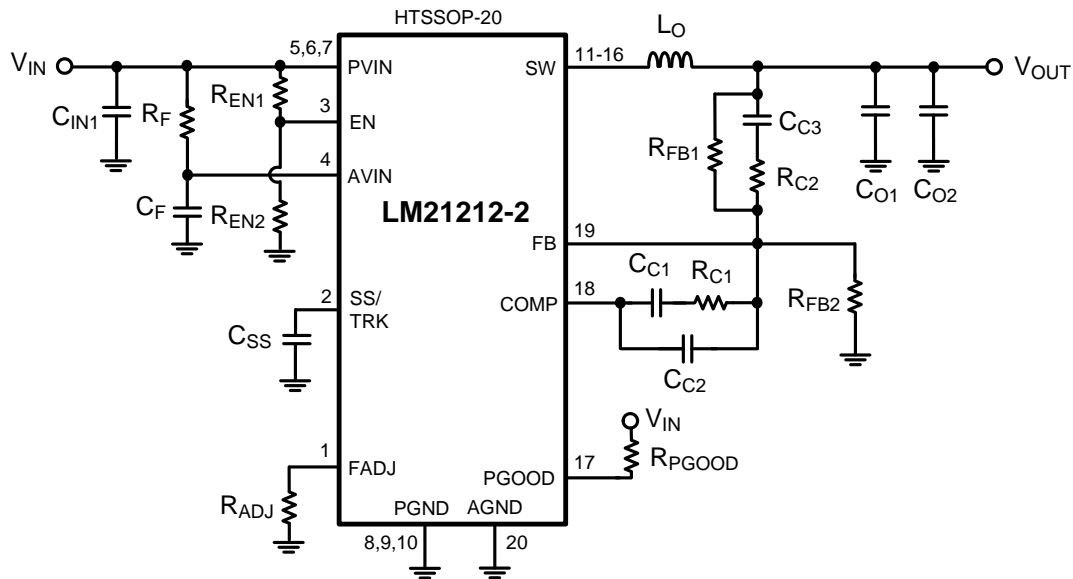


Figure 34. Typical Application Schematic 2

#### 9.2.2.1 Design Requirements

Table 2. Bill Of Materials ( $V_{IN} = 4\text{ V} - 5.5\text{ V}$ ,  $V_{OUT} = 0.9\text{ V}$ ,  $I_{OUT} = 8\text{ A}$ ,  $F_{SW} = 1\text{ MHz}$ )

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C <sub>F</sub>	CAP, CERM, 1 uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C <sub>IN1</sub> , C <sub>O1</sub> , C <sub>O2</sub>	CAP, CERM, 100 uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	3
C <sub>C1</sub>	CAP, CERM, 1800 pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H182JA01D	1
C <sub>C2</sub>	CAP, CERM, 68 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C <sub>C3</sub>	CAP, CERM, 470 pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H471J	1
C <sub>SS</sub>	CAP, CERM, 0.033 uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L <sub>O</sub>	Inductor, Shielded Drum Core, Superflux, 240nH, 20A, 0.001 ohm, SMD	Würth Elektronik	744314024	1
R <sub>F</sub>	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R <sub>C1</sub>	RES, 4.87 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K87FKEA	1
R <sub>C2</sub>	RES, 210 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603210RFKEA	1
R <sub>EN1</sub> , R <sub>FB1</sub> , R <sub>PG00D</sub>	RES, 10k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R <sub>EN2</sub>	RES, 19.6 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060319K6FKEA	1
R <sub>FB2</sub>	RES, 20.0 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA	1
R <sub>ADJ</sub>	RES, 41.2 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060341K2FKEA	1

#### 9.2.2.2 Detailed Design Procedure

See [Detailed Design Procedure](#)

## 10 Layout

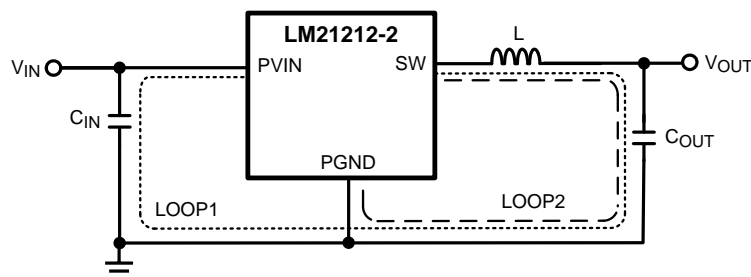
### 10.1 Layout Considerations

PC board layout is an important part of DC/DC converter design. Poor board layout can disrupt the performance of a DC/DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC/DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched at high slew rates. The first loop starts from the input capacitor, to the regulator PVIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to the load (see [Figure 35](#)). To minimize both loop areas, the input capacitor must be placed as close as possible to the VIN pin. Grounding for both the input and output capacitor must be close. Ideally, a ground plane must be placed on the top layer that connects the PGND pins, the exposed pad (EP) of the device, and the ground connections of the input and output capacitors in a small area near pins 10 and 11 of the device. The inductor must be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The six SW pins must be routed on a single top plane to the pad of the inductor. The inductor must be placed as close as possible to the switch pins of the device with a wide trace to minimize conductive losses. The inductor can be placed on the bottom side of the PCB relative to the LM21212-2, but care must be taken to not allow any coupling of the magnetic field of the inductor into the sensitive feedback or compensation traces.
3. Have a solid ground plane between PGND, the EP and the input and output cap. ground connections. The ground connections for the AGND, compensation, feedback, and soft-start components must be physically isolated (located near pins 1 and 20) from the power ground plane but a separate ground connection is not necessary. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Carefully route the connection from the VOUT signal to the compensation network. This node is high impedance and can be susceptible to noise coupling. The trace must be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise. Additionally, feedback resistors  $R_{FB1}$  and  $R_{FB2}$  must be located near the device to minimize the trace length to FB between these resistors.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Voltage accuracy at the load is important so make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.
6. Provide adequate device heatsinking. For most 12A designs a four layer board is recommended. Use as many vias as possible to connect the EP to the power plane heatsink. The vias located underneath the EP will wick solder into them if they are not filled. Complete solder coverage of the EP to the board is required to achieve the  $\theta_{JA}$  values described in the previous section. Either an adequate amount of solder must be applied to the EP pad to fill the vias, or the vias must be filled during manufacturing. See the [Thermal Considerations](#) section to ensure enough copper heatsinking area is used to keep the junction temperature below 125°C.

### 10.2 Layout Example



**Figure 35. Schematic of LM21212-2 Highlighting Layout Sensitive Nodes**

### 10.3 Thermal Considerations

The thermal characteristics of the LM21212-2 are specified using the parameter  $\theta_{JA}$ , which relates the junction temperature to the ambient temperature. Although the value of  $\theta_{JA}$  is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \cdot \theta_{JA} + T_A$$

where

- $T_J$  is the junction temperature in °C
  - $\theta_{JA}$  is the junction to ambient thermal resistance for the LM21212-2
  - $T_A$  is the ambient temperature in °C
- (20)

and

$$P_D = P_{IN} \cdot (1 - \text{Efficiency}) - I_{OUT}^2 \cdot R_{DCR}$$

where

- $P_{IN}$  is the input power in Watts ( $P_{IN} = V_{IN} \times I_{IN}$ )
  - $I_{OUT}$  is the output load current in A
- (21)

It is important to always keep the operating junction temperature ( $T_J$ ) below 125°C for reliable operation. If the junction temperature exceeds 165°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 36, shown below, provides a better approximation of the  $\theta_{JA}$  for a given PCB copper area. The PCB used in this test consisted of 4 layers: 1 oz. copper was used for the internal layers while the external layers were plated to 2 oz. copper weight. To provide an optimal thermal connection, a 3 x 4 array of 8 mil. vias under the thermal pad were used, and an additional sixteen 8 mil. vias under the rest of the device were used to connect the 4 layers.

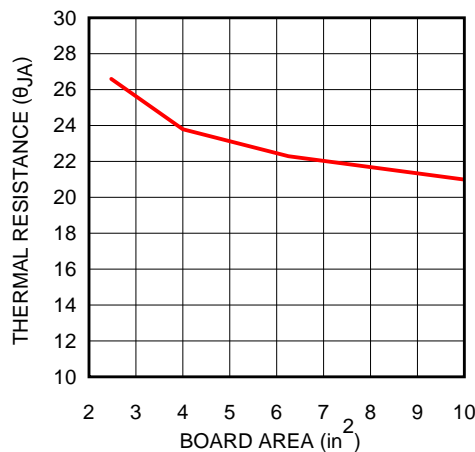
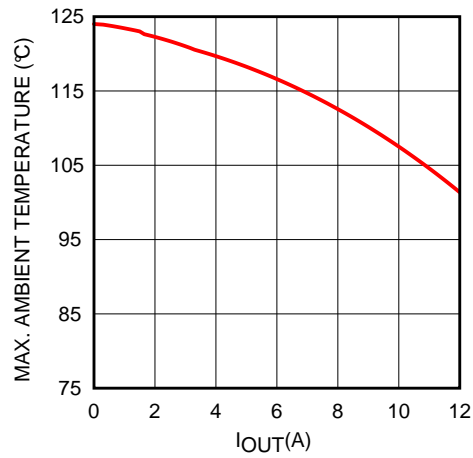


Figure 36. Thermal Resistance vs PCB Area (4-Layer Board)

**Thermal Considerations (continued)**

Figure 37 shows a plot of the maximum ambient temperature vs output current for the typical application circuit shown in , assuming a  $\theta_{JA}$  value of 24°C/W.



**Figure 37. Maximum Ambient Temperature vs Output Current (0 LFM)**

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

#### 11.1.2 开发支持

##### 11.1.2.1 使用 **WEBENCH®** 工具创建定制设计

单击[此处](#)，使用 LM21212-2 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 ( $V_{IN}$ )、输出电压 ( $V_{OUT}$ ) 和输出电流 ( $I_{OUT}$ ) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 [www.ti.com.cn/WEBENCH](http://www.ti.com.cn/WEBENCH)。

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商标

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.6 Glossary




**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM21212MH-2/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2	
LM21212MHE-2/NOPB	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2	
LM21212MHX-2/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-2	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21212MHE-2/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM21212MHX-2/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21212MHE-2/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM21212MHX-2/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM21212MH-2/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06

# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE

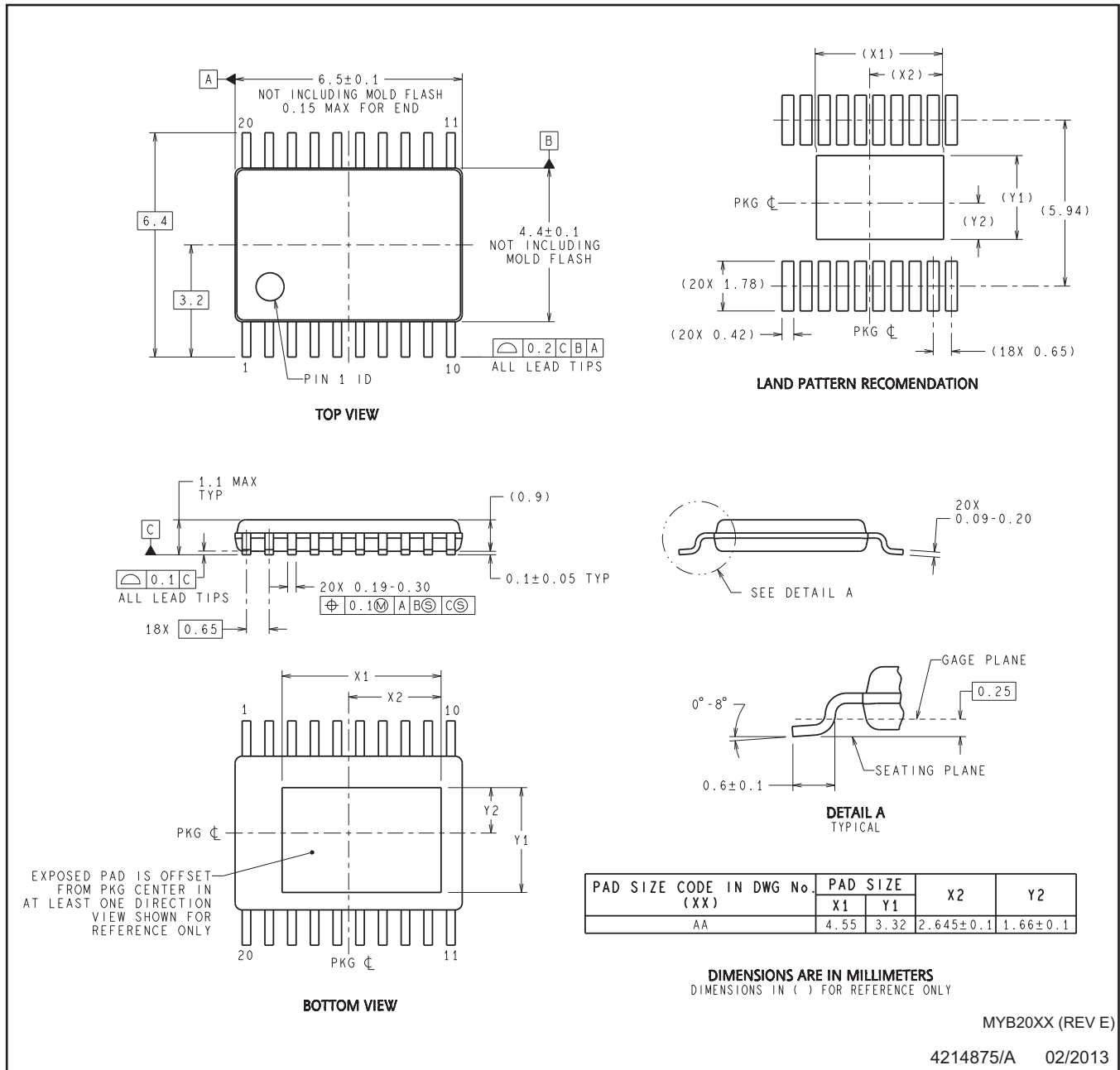


4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

PWP0020AA



MYB20XX (REV E)

4214875/A 02/2013

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Reference JEDEC Registration MO-153, Variation ACT.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司