

## EMC 性能优异的 ISO14xx 5kV<sub>RMS</sub> 隔离式 RS-485/RS-422 收发器

### 1 特性

- 符合 TIA/EIA-485-A 标准
- 在 5V 总线侧电源下与 PROFIBUS 兼容
- 总线 I/O 保护
  - ±30kV HBM
  - ±16kV IEC 61000-4-2 接触放电
  - ±4kV IEC 61000-4-4 电气快速瞬变
- 低 EMI 500kbps、12Mbps 和 50Mbps 数据速率
- 1.71V 至 5.5V 逻辑侧电源 (V<sub>CC1</sub>)，3V 至 5.5V 总线侧电源 (V<sub>CC2</sub>)
- 失效防护接收器（总线开路、短路和空闲）
- 1/8 单位负载：多达 256 个总线节点
- 100kV/μs（典型值）高共模瞬态抗扰度
- 扩展温度范围为 -40°C 至 +125°C
- 适用于热插拔功能的无干扰加电和断电
- 宽体 SOIC-16 封装
- 引脚兼容大多数隔离式 RS-485 收发器
- 安全相关认证：
  - 符合 DIN VDE V 0884-11:2017-01 标准的 7071V<sub>PK</sub> V<sub>IOTM</sub> 和 1500V<sub>PK</sub> V<sub>IORM</sub>（增强型和基本型选项）
  - UL 1577 标准下，长达 1 分钟的 5000V<sub>RMS</sub> 隔离
  - IEC 60950-1、IEC 62368-1、IEC 60601-1 和 IEC 61010-1 认证
  - CQC、TUV 和 CSA 认证
  - VDE（增强型）、UL、CQC 和 TUV 认证完成；VDE（基本型）和 CSA 审批正在处理中

### 2 应用

- 电网基础设施
- 光伏逆变器
- 工厂自动化与控制
- 电机驱动器
- HVAC 系统和楼宇自动化

### 3 说明

ISO14xx 器件是适用于 TIA/EIA RS-485 和 RS-422 应用的电隔离差分线路收发器。这些抗噪声收发器设计用于恶劣的工业环境。这些器件的总线引脚可承受高级别的 IEC 静电放电 (ESD) 和 IEC 电子快速瞬变 (EFT) 事件，无需在总线上使用额外组件进行系统级保护。这些器件提供有基础型和增强型隔离可供选择（请参阅 [增强型和基础型隔离选项](#)）。

#### 器件信息<sup>(1)</sup>

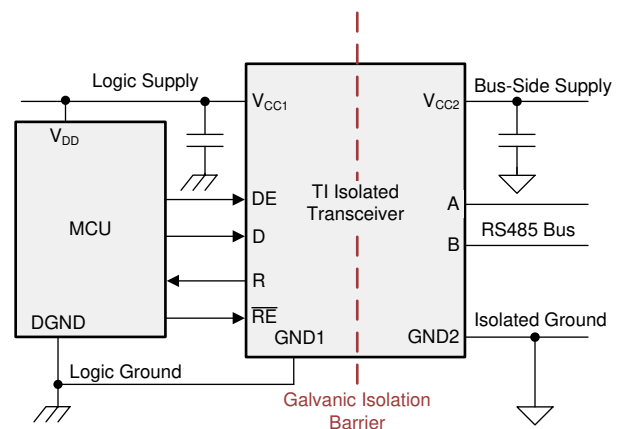
| 器件型号             | 封装        | 封装尺寸（标称值）        |
|------------------|-----------|------------------|
| ISO1410、ISO1410B | SOIC (16) | 10.30mm x 7.50mm |
| ISO1412、ISO1412B |           |                  |
| ISO1430、ISO1430B |           |                  |
| ISO1432、ISO1432B |           |                  |
| ISO1450、ISO1450B |           |                  |
| ISO1452、ISO1452B |           |                  |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

#### 增强型和基础型隔离选项

| 特性            | ISO14xx                                       | ISO14xxB                                      |
|---------------|---|---|
| 保护级别          | 加强版   | 基础版   |
| VDE 标准的浪涌测试电压 | 10000V <sub>PK</sub>                          | 6000V <sub>PK</sub>                           |
| UL 标准的隔离等级    | 5000V <sub>RMS</sub>                          | 5000V <sub>RMS</sub>                          |
| VDE 标准的工作电压   | 1060V <sub>RMS</sub> /<br>1500V <sub>PK</sub> | 1060V <sub>RMS</sub> /<br>1500V <sub>PK</sub> |

#### 简化应用电路原理图



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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| • Added footnote to Pin functions table for NC pins .....  | 5    |
| • Changed certification information in Safety related certifications table .....   | 10   |
| • Changed the V <sub>th+</sub> spec in Electrical characteristics: Receiver for -15 ≤ V <sub>CM</sub> ≤ 15 V from -20 mV to -10 mV ..... | 11   |
| • Added 1 line item for V <sub>th+</sub> in Electrical characteristics: Receiver for -7 ≤ V <sub>CM</sub> ≤ 12 V .....                   | 11   |

| Changes from Revision C (April 2019) to Revision D | Page |
|--|------|
| • 已添加 在整个数据表中添加了 B 器件编号 .....                      | 1    |

| Changes from Revision B (November 2018) to Revision C                                  | Page |
|--|------|
| • 已更改 将整个数据表中引用的 ISO141x 更改为 ISO14xx .....   | 1    |
| • 已添加 在“器件信息”表中添加了 ISO1430、ISO1432、ISO1450、ISO1452 .....                               | 1    |
| • Changed the position of Device Features labels .....                                 | 4    |
| • Added footnote to Pin Functions: Full-Duplex Device .....                            | 5    |
| • Added footnote to Pin Functions: Half-Duplex Device .....                            | 6    |
| • 已添加 Typical curves for ISO143x and ISO145x in <i>Typical Characteristics</i> .....   | 17   |
| • 已添加 Section 11.2.3 Application Curves and Section 11.2.3.1 Insulation Lifetime ..... | 33   |

**Changes from Revision A (August 2018) to Revision B**
**Page**

- 
- 已更改 将状态更改为生产数据 ..... 1
- 

**Changes from Original (July 2018) to Revision A**
**Page**

- 
- Changed the designator of common mode voltage in Recommended operating condition to  $V_I$  ..... 7
  - Added test condition for CMTI in Electrical characteristics: Driver ..... 11
  - Added test condition for CMTI in Electrical characteristics: Receiver ..... 12
  - 已更改  $V_{TEST}$  to  $V_{CM}$  in the *Common Mode Transient Immunity (CMTI)—Full Duplex* and *Common Mode Transient Immunity (CMTI)—Half Duplex* figures in the *Parameter Measurement Information* section ..... 23
  - 已更改  $t_{PLH}$  to  $t_{PZH}$  and  $t_{PLZ}$  to  $t_{PHZ}$  in the first *Driver Enable and Disable Times* timing diagram in the *Parameter Measurement Information* section ..... 24
  - 已添加  $t_{PHZ}$  to the first *Receiver Enable and Disable Times* timing diagram in the *Parameter Measurement Information* section ..... 25
-

## 5 说明（续）

这些器件用于长距离通信。隔离会破坏通信节点之间的接地回路，从而获得更大的共模电压范围。经测试，每个器件的对称隔离栅可在总线收发器和逻辑电平接口之间按照 UL 1577 标准提供为时 1 分钟的 5000V<sub>RMS</sub> 隔离。

ISO14xx 器件可由 1 侧的 1.71V 至 5.5V 电压供电运行，此电压范围使器件能够与低压 FPGA 和 ASIC 连接。2 侧上具有 3V 至 5.5V 的宽电源电压范围，因此无需在隔离侧提供稳压电源。这些器件支持 -40°C 至 +125°C 的宽工作环境温度范围。

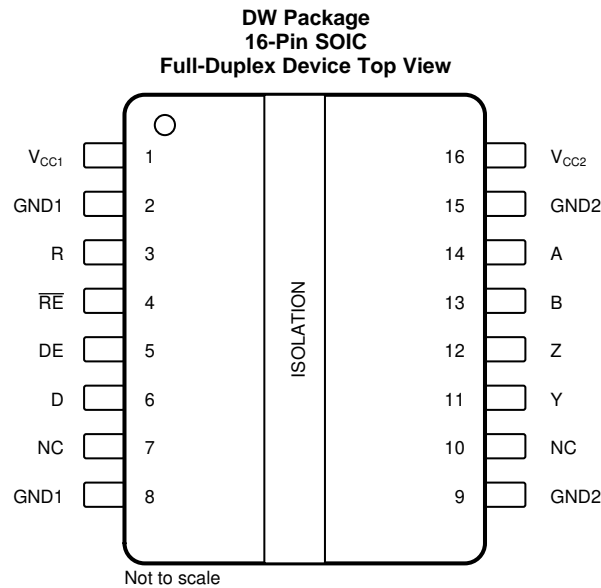
## 6 Device Options

Table 1 shows an overview of the options available for this family of devices.

**Table 1. Device Features**

| PART NUMBER       | ISOLATION         | DUPLEX | DATA RATE | PACKAGE   |
|-------------------|-------------------|--------|-----------|-----------|
| ISO1410, ISO1410B | Reinforced, Basic | Half   | 500 Kbps  | 16-pin DW |
| ISO1412, ISO1412B |                   | Full   | 500 Kbps  | 16-pin DW |
| ISO1430, ISO1430B |                   | Half   | 12 Mbps   | 16-pin DW |
| ISO1432, ISO1432B |                   | Full   | 12 Mbps   | 16-pin DW |
| ISO1450, ISO1450B |                   | Half   | 50 Mbps   | 16-pin DW |
| ISO1452, ISO1452B |                   | Full   | 50 Mbps   | 16-pin DW |

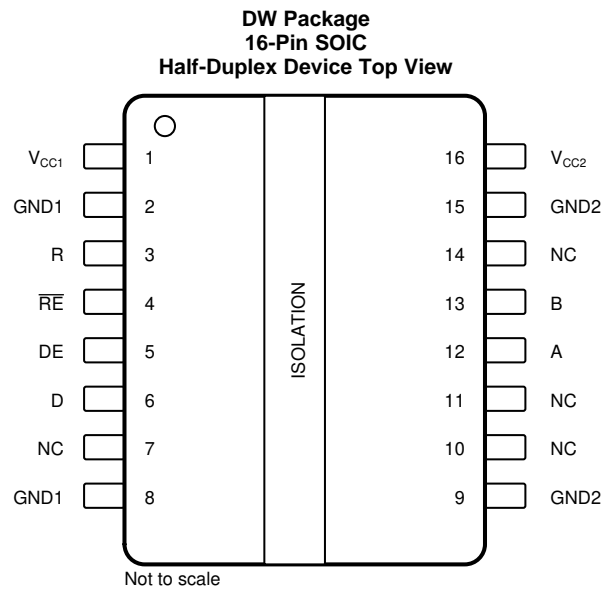
## 7 Pin Configuration and Functions



**Pin Functions: Full-Duplex Device**

| PIN                 |     | I/O | DESCRIPTION  |
|---------------------|-----|-----|--|
| NAME                | NO. |     |  |
| A                   | 14  | I   | Receiver non-inverting input on the bus side   |
| B                   | 13  | I   | Receiver inverting input on the bus side   |
| D                   | 6   | I   | Driver input   |
| DE                  | 5   | I   | Driver enable. This pin enables the driver output when high and disables the driver output when low or open.       |
| GND1 <sup>(1)</sup> | 2   | —   | Ground connection for V <sub>CC1</sub>   |
| GND1 <sup>(1)</sup> | 8   | —   | Ground connection for V <sub>CC1</sub>   |
| GND2 <sup>(1)</sup> | 9   | —   | Ground connection for V <sub>CC2</sub>   |
| GND2 <sup>(1)</sup> | 15  | —   | Ground connection for V <sub>CC2</sub>   |
| NC <sup>(2)</sup>   | 7   | —   | No internal connection   |
| NC <sup>(2)</sup>   | 10  | —   | No internal connection   |
| R                   | 3   | O   | Receiver output  |
| RE                  | 4   | I   | Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low. |
| V <sub>CC1</sub>    | 1   | —   | Logic-side power supply  |
| V <sub>CC2</sub>    | 16  | —   | Transceiver-side power supply  |
| Y                   | 11  | O   | Driver non-inverting output  |
| Z                   | 12  | O   | Driver inverting output  |

- (1) For Logic side, both Pin 2 and Pin 8 must be connected to GND1. For Bus side, both Pin 9 and Pin 15 must be connected to GND2.  
 (2) Device functionality is not affected if NC pins are connected to supply or ground on PCB



**Pin Functions: Half-Duplex Device**

| PIN                 |     | I/O | DESCRIPTION  |
|---------------------|-----|-----|--|
| NAME                | NO. |     |  |
| A                   | 12  | I/O | Transceiver non-inverting input or output (I/O) on the bus side  |
| B                   | 13  | I/O | Transceiver inverting input or output (I/O) on the bus side  |
| D                   | 6   | I   | Driver input   |
| DE                  | 5   | I   | Driver enable. This pin enables the driver output when high and disables the driver output when low or open.       |
| GND1 <sup>(1)</sup> | 2   | —   | Ground connection for V <sub>CC1</sub>   |
| GND1 <sup>(1)</sup> | 8   | —   | Ground connection for V <sub>CC1</sub>   |
| GND2 <sup>(1)</sup> | 9   | —   | Ground connection for V <sub>CC2</sub>   |
| GND2 <sup>(1)</sup> | 15  | —   | Ground connection for V <sub>CC2</sub>   |
| NC <sup>(2)</sup>   | 7   | —   | No internal connection   |
| NC <sup>(2)</sup>   | 10  | —   | No internal connection   |
| NC <sup>(2)</sup>   | 11  | —   | No internal connection   |
| NC <sup>(2)</sup>   | 14  | —   | No internal connection   |
| R                   | 3   | O   | Receiver output  |
| $\overline{RE}$     | 4   | I   | Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low. |
| V <sub>CC1</sub>    | 1   | —   | Logic-side power supply  |
| V <sub>CC2</sub>    | 16  | —   | Transceiver-side power supply  |

- (1) For Logic side, both Pin 2 and Pin 8 must be connected to GND1. For Bus side, both Pin 9 and Pin 15 must be connected to GND2.  
 (2) Device functionality is not affected if NC pins are connected to supply or ground on PCB

## 8 Specifications

### 8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

|                  |  | MIN  | MAX                                  | UNIT |
|------------------|--|------|--------------------------------------|------|
| V <sub>CC1</sub> | Supply voltage, side 1                           | -0.5 | 6                                    | V    |
| V <sub>CC2</sub> | Supply voltage, side 2                           | -0.5 | 6                                    | V    |
| V <sub>IO</sub>  | Logic voltage level (D, DE, $\overline{RE}$ , R) | -0.5 | V <sub>CC1</sub> +0.5 <sup>(3)</sup> | V    |
| I <sub>O</sub>   | Output current on R pin                          | -15  | 15                                   | mA   |
| V <sub>BUS</sub> | Voltage on bus pins (A, B, Y, Z w.r.t GND2)      | -18  | 18                                   | V    |
| T <sub>J</sub>   | Junction temperature                             | -40  | 150                                  | °C   |
| T <sub>STG</sub> | Storage temperature                              | -65  | 150                                  | °C   |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- Maximum voltage must not exceed 6 V

### 8.2 ESD Ratings

|                    |   |   | VALUE  | UNIT |
|--------------------|---|---|--------|------|
| V <sub>(ESD)</sub> | Contact Discharge, per IEC 61000-4-2  | Pins Bus terminals and GND2                                     | ±16000 | V    |
| V <sub>(ESD)</sub> | Contact Discharge, per IEC 61000-4-2  | ISO141x, Pins Bus terminals and GND1 (across isolation barrier) | ±8000  | V    |
| V <sub>(ESD)</sub> | Contact Discharge, per IEC 61000-4-2  | ISO143x, Pins Bus terminals and GND1 (across isolation barrier) | ±8000  | V    |
| V <sub>(ESD)</sub> | Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001              | All pins except bus pins <sup>(1)</sup>                         | ±6000  | V    |
|                    |   | Bus terminals to GND2 <sup>(1)</sup>                            | ±30000 | V    |
|                    | Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101 | All pins <sup>(2)</sup>   | ±1500  |      |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

|                   |  | MIN                  | MAX                  | UNIT |
|-------------------|--|----------------------|----------------------|------|
| V <sub>CC1</sub>  | Supply Voltage, Side 1, 1.8-V operation                  | 1.71                 | 1.89                 | V    |
|                   | Supply Voltage, Side 1, 2.5-V, 3.3-V and 5.5-V operation | 2.25                 | 5.5                  | V    |
| V <sub>CC2</sub>  | Supply Voltage, Side 2                                   | 3                    | 5.5                  | V    |
| V <sub>I</sub>    | Common Mode voltage at any bus terminal: A or B          | -7                   | 12                   | V    |
| V <sub>IH</sub>   | High-level input voltage (D, DE, $\overline{RE}$ inputs) | 0.7*V <sub>CC1</sub> | V <sub>CC1</sub>     | V    |
| V <sub>IL</sub>   | Low-level input voltage (D, DE, $\overline{RE}$ inputs)  | 0                    | 0.3*V <sub>CC1</sub> | V    |
| V <sub>ID</sub>   | Differential input voltage, A with respect to B          | -15                  | 15                   | V    |
| I <sub>O</sub>    | Output current, Driver                                   | -60                  | 60                   | mA   |
| I <sub>OR</sub>   | Output current, Receiver                                 | -4                   | 4                    | mA   |
| R <sub>L</sub>    | Differential load resistance                             | 54                   |                      | Ω    |
| 1/t <sub>UI</sub> | Signaling rate ISO141x                                   |                      | 500                  | kbps |
| 1/t <sub>UI</sub> | Signaling Rate ISO143x                                   |                      | 12                   | Mbps |
| 1/t <sub>UI</sub> | Signaling rate ISO145x                                   |                      | 50                   | Mbps |
| T <sub>A</sub>    | Operating ambient temperature                            | -40                  | 125                  | °C   |

## 8.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ISO14xx   | UNIT |
|-------------------------------|--|-----------|------|
|                               |  | DW (SOIC) |      |
|                               |  | 16 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 67.9      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 27.7      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 29.4      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 12.9      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 28.8      | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | —         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 8.5 Power Ratings

| PARAMETER              |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----|-----|-----|------|
| <b>ISO1410_ISO1412</b> |  |  |     |     |     |      |
| $P_D$                  | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , A-B load = $54\ \Omega \parallel 50\text{pF}$ , Load on R=15pF<br>Input a 250kHz 50% duty cycle square wave to D pin with<br>$V_{DE}=V_{CC1}$ , $V_{RE}=GND1$ |     |     | 556 | mW   |
| $P_{D1}$               | Maximum power dissipation (side-1)     |  |     |     | 28  | mW   |
| $P_{D2}$               | Maximum power dissipation (side-2)     |  |     |     | 528 | mW   |
| <b>ISO1430_ISO1432</b> |  |  |     |     |     |      |
| $P_D$                  | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , A-B load = $54\ \Omega \parallel 50\text{pF}$ , Load on R=15pF<br>Input a 6MHz 50% duty cycle square wave to D pin with<br>$V_{DE}=V_{CC1}$ , $V_{RE}=GND1$   |     |     | 352 | mW   |
| $P_{D1}$               | Maximum power dissipation (side-1)     |  |     |     | 33  | mW   |
| $P_{D2}$               | Maximum power dissipation (side-2)     |  |     |     | 319 | mW   |
| <b>ISO1450_ISO1452</b> |  |  |     |     |     |      |
| $P_D$                  | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , A-B load = $54\ \Omega \parallel 50\text{pF}$ , Load on R=15pF<br>Input a 25MHz 50% duty cycle square wave to D pin with<br>$V_{DE}=V_{CC1}$ , $V_{RE}=GND1$  |     |     | 588 | mW   |
| $P_{D1}$               | Maximum power dissipation (side-1)     |  |     |     | 49  | mW   |
| $P_{D2}$               | Maximum power dissipation (side-2)     |  |     |     | 539 | mW   |



## 8.6 Insulation Specifications

| PARAMETER                                      |   | TEST CONDITIONS  | SPECIFICATIONS     | UNIT             |
|--|---|--|--------------------|------------------|
|  |   |  | DW-16              |                  |
| <b>IEC 60664-1</b>                             |   |  |                    |                  |
| CLR  | External clearance <sup>(1)</sup>                       | Side 1 to side 2 distance through air  | >8                 | mm               |
| CPG  | External creepage <sup>(1)</sup>                        | Side 1 to side 2 distance across package surface   | >8                 | mm               |
| DTI  | Distance through the insulation                         | Minimum internal gap (internal clearance)  | >17                | μm               |
| CTI  | Comparative tracking index                              | IEC 60112; UL 746A   | >600               | V                |
|  | Material Group  | According to IEC 60664-1   | I                  |                  |
|  | Overvoltage category                                    | Rated mains voltage ≤ 600 V <sub>RMS</sub>   | I-IV               |                  |
|  |   | Rated mains voltage ≤ 1000 V <sub>RMS</sub>  | I-III              |                  |
| <b>DIN VDE V 0884-11:2017-01<sup>(2)</sup></b> |   |  |                    |                  |
| V <sub>IORM</sub>                              | Maximum repetitive peak isolation voltage               | AC voltage (bipolar)   | 1500               | V <sub>PK</sub>  |
| V <sub>IOWM</sub>                              | Maximum working isolation voltage                       | AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test; see <a href="#">Figure 56</a>   | 1060               | V <sub>RMS</sub> |
|  |   | DC voltage   | 1500               | V <sub>DC</sub>  |
| V <sub>IOTM</sub>                              | Maximum transient isolation voltage                     | V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)  | 7071               | V <sub>PK</sub>  |
| V <sub>IOSM</sub>                              | Maximum surge isolation voltage ISO141x <sup>(3)</sup>  | Test method per IEC 62368-1, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 10000 V <sub>PK</sub> (qualification)   | 6250               | V <sub>PK</sub>  |
|  | Maximum surge isolation voltage ISO141xB <sup>(3)</sup> | Test method per IEC 62368-1, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.3 × V <sub>IOSM</sub> = 6000 V <sub>PK</sub> (qualification)  | 4615               | V <sub>PK</sub>  |
| q <sub>pd</sub>                                | Apparent charge <sup>(4)</sup>                          | Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s   | ≤ 5                | pC               |
|  |   | Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; ISO14xx: V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s; ISO14xxB: V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s                              | ≤ 5                |                  |
|  |   | Method b1: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; ISO14xx: V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s; ISO14xxB: V <sub>pd(m)</sub> = 1.5 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s | ≤ 5                |                  |
| C <sub>IO</sub>                                | Barrier capacitance, input to output <sup>(5)</sup>     | V <sub>IO</sub> = 0.4 × sin(2 πft), f = 1 MHz  | 1                  | pF               |
| R <sub>IO</sub>                                | Insulation resistance, input to output <sup>(5)</sup>   | V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C   | > 10 <sup>12</sup> | Ω                |
|  |   | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 150°C  | > 10 <sup>11</sup> |                  |
|  |   | V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C  | > 10 <sup>9</sup>  |                  |
|  | Pollution degree  |  | 2                  |                  |
|  | Climatic category                                       |  | 40/125/<br>21      |                  |
| <b>UL 1577</b>                                 |   |  |                    |                  |
| V <sub>ISO</sub>                               | Withstand isolation voltage                             | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)  | 5000               | V <sub>RMS</sub> |

- Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- ISO14xx is suitable for *safe electrical insulation* and ISO14xxB is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-pin device.

## 8.7 Safety-Related Certifications

| VDE   | CSA   | UL   | CQC  | TUV  |
|---|---|--|--|--|
| Certified according to DIN VDE V 0884-11:2017- 01   | Plan to certify according to IEC 60950-1, IEC 62368-1 and IEC 60601-1   | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011   | Certified according to EN 61010-1:2010/A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014  |
| Maximum transient isolation voltage, 7071 V <sub>PK</sub> ;<br>Maximum repetitive peak isolation voltage, 1500 V <sub>PK</sub> ;<br>Maximum surge isolation voltage, ISO141x, ISO143x, ISO145x: 6250 V <sub>PK</sub> (Reinforced)<br>ISO141xB, ISO143xB, ISO145xB: 4600 V <sub>PK</sub> (Basic) | CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., for pollution degree 2, material group I<br>ISO141x, ISO143x, ISO145x: 800 V <sub>RMS</sub> reinforced isolation<br>ISO141xB, ISO143xB, ISO145xB: 800 V <sub>RMS</sub> basic isolation<br>-----<br>CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1, ISO141x, ISO143x, ISO145x: 2 MOPP (Means of Patient Protection) 250 V <sub>RMS</sub> (354 V <sub>PK</sub> ) maximum working voltage | Single protection, 5000 V <sub>RMS</sub>               | Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V <sub>RMS</sub> maximum working voltage | EN 61010-1:2010 /A1:2019<br>ISO141x, ISO143x, ISO145x: 600 V <sub>RMS</sub> reinforced isolation<br>ISO141xB, ISO143xB, ISO145xB: 1000 V <sub>RMS</sub> basic isolation<br>-----<br>EN 60950-1:2006/A2:2013 and EN 62368-1:2014<br>ISO141x, ISO143x, ISO145x: 800 V <sub>RMS</sub> reinforced isolation<br>ISO141xB, ISO143xB, ISO145xB: 1060 V <sub>RMS</sub> basic isolation |
| Reinforced Certificate:40040142<br>Basic certificate planned  | Certificate planned   | File number: E181974                                   | Certificate number: CQC15001121716   | Client ID number: 77311  |

## 8.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER            |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------------|---|--|-----|-----|------|------|
| <b>DW-16 PACKAGE</b> |   |  |     |     |      |      |
| I <sub>S</sub>       | Safety input, output, or supply current | R <sub>θJA</sub> = 67.9°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Fig 1</a>  |     |     | 334  | mA   |
|                      |   | R <sub>θJA</sub> = 67.9°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Fig 1</a>  |     |     | 511  |      |
|                      |   | R <sub>θJA</sub> = 67.9°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Fig 1</a> |     |     | 669  |      |
|                      |   | R <sub>θJA</sub> = 67.9°C/W, V <sub>I</sub> = 1.89 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Fig 1</a> |     |     | 974  |      |
| P <sub>S</sub>       | Safety input, output, or total power    | R <sub>θJA</sub> = 67.9°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, see <a href="#">Fig 2</a>                          |     |     | 1837 | mW   |
| T <sub>S</sub>       | Maximum safety temperature              |  |     |     | 150  | °C   |

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$$T_J = T_A + R_{\theta JA} \times P, \text{ where } P \text{ is the power dissipated in the device.}$$

$$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S, \text{ where } T_{J(max)} \text{ is the maximum allowed junction temperature.}$$

$$P_S = I_S \times V_I, \text{ where } V_I \text{ is the maximum input voltage.}$$

## 8.9 Electrical Characteristics: Driver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER           |   | TEST CONDITIONS  | MIN  | TYP                  | MAX       | UNIT        |
|---------------------|---|--|------|----------------------|-----------|-------------|
| $ V_{Odl}$          | Driver differential-output voltage magnitude                          | Open circuit voltage, unloaded bus, $3V \leq V_{CC2} \leq 5.5V$  | 1.5  | 5                    | $V_{CC2}$ | V           |
|                     |   | $R_L = 60\ \Omega$ , $-7V \leq V_{TEST} \leq 12V$ (see Fig 35), $3V \leq V_{CC2} \leq 3.6V$ , $T_A < 100^\circ C$          | 1.5  | 2.3                  |           | V           |
|                     |   | $R_L = 60\ \Omega$ , $-7V \leq V_{TEST} \leq 12V$ (see Fig 35), $3.1V \leq V_{CC2} \leq 3.6V$ , $T_A > 100^\circ C$        | 1.5  | 2.3                  |           |             |
|                     |   | $R_L = 60\ \Omega$ , $-7V \leq V_{TEST} \leq 12V$ , $4.5V < V_{CC2} < 5.5V$ (see Fig 35)                                   | 2.1  | 3.7                  |           | V           |
|                     |   | $R_L = 100\ \Omega$ (see Fig 36), RS-422 load  | 2    | 4.2                  |           | V           |
|                     |   | $R_L = 54\ \Omega$ (see Fig 36), RS-485 load, $V_{CC2} = 3V$ to $3.6V$   | 1.5  | 2.3                  |           | V           |
|                     | $R_L = 54\ \Omega$ (see Fig 36), RS-485 load, $4.5V < V_{CC2} < 5.5V$ | 2.1  | 3.7  |                      | V         |             |
| $\Delta V_{Odl} $   | Change in differential output voltage between two states              | $R_L = 54\ \Omega$ or $R_L = 100\ \Omega$ , see Fig 36   | -200 |                      | 200       | mV          |
| $V_{OC}$            | Common-mode output voltage  | $R_L = 54\ \Omega$ or $R_L = 100\ \Omega$ , see Fig 36   | 1    | $0.5 \times V_{CC2}$ | 3         | V           |
| $\Delta V_{OC(SS)}$ | change in steady-state common-mode output voltage between two states  | $R_L = 54\ \Omega$ or $R_L = 100\ \Omega$ , see Fig 36   | -200 |                      | 200       | mV          |
| $I_{OS}$            | Short-circuit output current  | $V_D = V_{CC1}$ or $V_D = V_{GND1}$ , $V_{DE} = V_{CC1}$ , $V_{CC2} = 3.3V \pm 10\%$<br>$-7V \leq V \leq 12V$ , see Fig 45 | -250 |                      | 250       | mA          |
|                     |   | $V_D = V_{CC1}$ or $V_D = V_{GND1}$ , $V_{DE} = V_{CC1}$ , $V_{CC2} = 5V \pm 10\%$<br>$-7V \leq V \leq 12V$ , see Fig 45   |      | 250                  |           | mA          |
| $I_i$               | Input current   | $V_D$ and $V_{DE} = 0V$ or $V_D$ and $V_{DE} = V_{CC1}$  | -10  |                      | 10        | $\mu A$     |
| CMTI                | Common-mode transient immunity  | $V_D = V_{CC1}$ or $GND1$ , $V_{CC1} = 1.71V$ to $5.5V$ , $V_{CM} = 1200V$ , ISO141x, See Fig 38                           | 85   | 100                  |           | kV/ $\mu s$ |
| CMTI                | Common-mode transient immunity  | $V_D = V_{CC1}$ or $GND1$ , $V_{CC1} = 1.71V$ to $5.5V$ , $V_{CM} = 1200V$ , ISO143x, See Fig 38                           | 85   | 100                  |           | kV/ $\mu s$ |
| CMTI                | Common-mode transient immunity  | $V_D = V_{CC1}$ or $GND1$ , $V_{CC1} = 2.25V$ to $5.5V$ , $V_{CM} = 1200V$ , ISO145x, See Fig 38                           | 85   | 100                  |           | kV/ $\mu s$ |

## 8.10 Electrical Characteristics: Receiver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS   | MIN             | TYP  | MAX     | UNIT    |
|-----------|--|---|-----------------|------|---------|---------|
| $I_{i1}$  | Bus input current                        | $V_{DE} = 0V$ , $V_{CC2} = 0V$ or $V_{CC2} = 5.5V$ , 500-kbps devices, $V_I = -7V$ or $V_I = 12V$ , other input at $0V$             | -100            |      | 125     | $\mu A$ |
| $I_{i1}$  | Bus input current                        | $V_{DE} = 0V$ , $V_{CC2} = 0V$ or $V_{CC2} = 5.5V$ , 12-Mbps and 50-Mbps devices, $V_I = -7V$ or $V_I = 12V$ , other input at $0V$  | -100            |      | 125     | $\mu A$ |
| $I_{i1}$  | Bus input current                        | $V_{DE} = 0V$ , $V_{CC2} = 0V$ or $V_{CC2} = 5.5V$ , 500-kbps devices, $V_I = -15V$ or $V_I = 15V$ , other input at $0V$            | -200            |      | 125     | $\mu A$ |
| $I_{i1}$  | Bus input current                        | $V_{DE} = 0V$ , $V_{CC2} = 0V$ or $V_{CC2} = 5.5V$ , 12-Mbps and 50-Mbps devices, $V_I = -15V$ or $V_I = 15V$ , other input at $0V$ | -200            |      | 125     | $\mu A$ |
| $V_{TH+}$ | Positive-going input threshold voltage   | $-15V \leq V_{CM} \leq 15V$   | See (1)         | -100 | -10     | mV      |
|           |  | $-7V \leq V_{CM} \leq 12V$  | See (1)         | -100 | -20     | mV      |
| $V_{TH-}$ | Negative-going input threshold voltage   | $-15V \leq V_{CM} \leq 15V$   | -200            | -130 | See (1) | mV      |
| $V_{hys}$ | Input hysteresis ( $V_{TH+} - V_{TH-}$ ) | $-15V \leq V_{CM} \leq 15V$   |                 | 30   |         | mV      |
| $V_{OH}$  | Output high voltage on the R pin         | $V_{CC1} = 5V \pm 10\%$ , $I_{OH} = -4mA$ , $V_{ID} = 200mV$  | $V_{CC1} - 0.4$ |      |         | V       |
|           |  | $V_{CC1} = 3.3V \pm 10\%$ , $I_{OH} = -2mA$ , $V_{ID} = 200mV$  | $V_{CC1} - 0.3$ |      |         | V       |
|           |  | $V_{CC1} = 2.5V \pm 10\%$ , $1.8V \pm 5\%$ , $I_{OH} = -1mA$ , $V_{ID} = 200mV$   | $V_{CC1} - 0.2$ |      |         | V       |

(1) Under any specific conditions,  $V_{TH+}$  is ensured to be at least  $V_{hys}$  higher than  $V_{TH-}$ .

## Electrical Characteristics: Receiver (continued)

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT       |
|-----------|--|--|-----|-----|-----|------------|
| $V_{OL}$  | Output low voltage on the R pin            | $V_{CC1}=5V \pm 10\%$ , $I_{OL} = 4 \text{ mA}$ , $V_{ID} = -200 \text{ mV}$   |     |     | 0.4 | V          |
|           |  | $V_{CC1}=3.3V \pm 10\%$ , $I_{OL} = 2 \text{ mA}$ , $V_{ID} = -200 \text{ mV}$   |     |     | 0.3 | V          |
|           |  | $V_{CC1}=2.5V \pm 10\%$ , $1.8V \pm 5\%$ , $I_{OL} = 1 \text{ mA}$ , $V_{ID} = -200 \text{ mV}$  |     |     | 0.2 | V          |
| $I_{OZ}$  | Output high-impedance current on the R pin | $V_R = 0 \text{ V}$ or $V_R = V_{CC1}$ , $\overline{V_{RE}} = V_{CC1}$   | -1  |     | 1   | $\mu A$    |
| $I_i$     | Input current on the $\overline{RE}$ pin   | $\overline{V_{RE}} = 0 \text{ V}$ or $\overline{V_{RE}} = V_{CC1}$   | -10 |     | 10  | $\mu A$    |
| CMTI      | Common-mode transient immunity             | $V_{CC1}=1.71 \text{ V}$ to $5.5 \text{ V}$ , $V_{ID} = 1.5 \text{ V}$ or $-1.5 \text{ V}$ , $V_{CM} = 1200 \text{ V}$ , ISO141x, See <a href="#">Fig 38</a> | 85  | 100 |     | $kV/\mu s$ |
| CMTI      | Common-mode transient immunity             | $V_{CC1}=1.71 \text{ V}$ to $5.5 \text{ V}$ , $V_{ID} = 1.5 \text{ V}$ or $-1.5 \text{ V}$ , $V_{CM} = 1200 \text{ V}$ , ISO143x, See <a href="#">Fig 38</a> | 85  | 100 |     | $kV/\mu s$ |
| CMTI      | Common-mode transient immunity             | $V_{CC1}=2.25 \text{ V}$ to $5.5 \text{ V}$ , $V_{ID} = 1.5 \text{ V}$ or $-1.5 \text{ V}$ , $V_{CM} = 1200 \text{ V}$ , ISO145x, See <a href="#">Fig 38</a> | 85  | 100 |     | $kV/\mu s$ |

## 8.11 Supply Current Characteristics: Side 1 ( $I_{CC1}$ )

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| <b>DRIVER ENABLED, RECEIVER DISABLED</b>  |   |     |     |     |      |
| Logic-side supply current                 | $V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$  |     | 2.6 | 4.4 | mA   |
| Logic-side supply current                 | $V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$  |     | 2.6 | 4.4 | mA   |
| Logic-side supply current                 | ISO141x, D = 500-kbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$  |     | 3.2 | 5.1 | mA   |
| Logic-side supply current                 | ISO141x, D = 500-kbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$  |     | 3.2 | 5.1 | mA   |
| Logic-side supply current                 | ISO143x, D = 12-Mbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$   |     | 3.2 | 5.1 | mA   |
| Logic-side supply current                 | ISO143x, D = 12-Mbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$   |     | 3.2 | 5.1 | mA   |
| Logic-side supply current                 | ISO145x, D = 50-Mbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$   |     | 3.6 | 5.3 | mA   |
| Logic-side supply current                 | ISO145x, D = 50-Mbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$   |     | 3.4 | 5.2 | mA   |
| <b>DRIVER ENABLED, RECEIVER ENABLED</b>   |   |     |     |     |      |
| Logic-side supply current                 | $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, $V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$   |     | 2.6 | 4.4 | mA   |
| Logic-side supply current                 | $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, $V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$   |     | 2.6 | 4.4 | mA   |
| Logic-side supply current                 | ISO141x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 500-kbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$   |     | 3.3 | 5.1 | mA   |
| Logic-side supply current                 | ISO141x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 500-kbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$ |     | 3.2 | 5.1 | mA   |
| Logic-side supply current                 | ISO143x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 12-Mbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$    |     | 4.1 | 6   | mA   |
| Logic-side supply current                 | ISO143x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 12-Mbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 3.8 | 5.7 | mA   |
| Logic-side supply current                 | ISO145x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 50-Mbps square wave with 50% duty cycle, $V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$    |     | 6.3 | 8.9 | mA   |
| Logic-side supply current                 | ISO145x, $\overline{V_{RE}} = V_{GND1}$ , loopback if full-duplex device, D = 50-Mbps square wave with 50% duty cycle, $V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 5.3 | 7.8 | mA   |
| <b>DRIVER DISABLED, RECEIVER ENABLED</b>  |   |     |     |     |      |
| Logic-side supply current                 | $V_{(A-B)} \geq 200\text{ mV}, V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$  |     | 1.6 | 3.1 | mA   |
| Logic-side supply current                 | $V_{(A-B)} \geq 200\text{ mV}, V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$  |     | 1.6 | 3.1 | mA   |
| Logic-side supply current                 | ISO141x, (A-B) = 500-kbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$   |     | 1.7 | 3.1 | mA   |
| Logic-side supply current                 | ISO141x, (A-B) = 500-kbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$   |     | 1.6 | 3.1 | mA   |
| Logic-side supply current                 | ISO143x, (A-B) = 12-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 2.6 | 4   | mA   |
| Logic-side supply current                 | ISO143x, (A-B) = 12-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 2.2 | 3.7 | mA   |
| Logic-side supply current                 | ISO145x, (A-B) = 50-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 4.7 | 6.7 | mA   |
| Logic-side supply current                 | ISO145x, (A-B) = 50-Mbps square wave with 50% duty cycle, $V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$ , $C_{L(R)}^{(1)} = 15\text{ pF}$  |     | 3.7 | 5.7 | mA   |
| <b>DRIVER DISABLED, RECEIVER DISABLED</b> |   |     |     |     |      |
| Logic-side supply current                 | $V_{DE} = V_{GND1}, V_D = V_{CC1}, V_{CC1} = 5\text{ V} \pm 10\%$   |     | 1.6 | 3.1 | mA   |
| Logic-side supply current                 | $V_{DE} = V_{GND1}, V_D = V_{CC1}, V_{CC1} = 3.3\text{ V} \pm 10\%$   |     | 1.6 | 3.1 | mA   |

 (1)  $C_{L(R)}$  is the load capacitance on the R pin.

## 8.12 Supply Current Characteristics: Side 2 ( $I_{CC2}$ )

$V_{RE} = V_{GND1}$  or  $V_{RE} = V_{CC1}$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                      | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| <b>DRIVER ENABLED, BUS UNLOADED</b>            |  |     |     |     |      |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$  |     | 4   | 6.1 | mA   |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $V_{CC2} = 5\text{ V} \pm 10\%$  |     | 4.5 | 6.6 | mA   |
| <b>DRIVER ENABLED, BUS LOADED</b>              |  |     |     |     |      |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $R_L = 54\ \Omega$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$   |     | 48  | 58  | mA   |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $R_L = 54\ \Omega$ , $V_{CC2} = 5\text{ V} \pm 10\%$   |     | 74  | 88  | mA   |
| Bus-side supply current                        | ISO141x, D = 500-kbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$ |     | 63  | 95  | mA   |
| Bus-side supply current                        | ISO141x, D = 500-kbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 5\text{ V} \pm 10\%$   |     | 113 | 160 | mA   |
| Bus-side supply current                        | ISO143x, D = 12-Mbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$  |     | 56  | 75  | mA   |
| Bus-side supply current                        | ISO143x, D = 12-Mbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 5\text{ V} \pm 10\%$    |     | 97  | 122 | mA   |
| Bus-side supply current                        | ISO145x, D = 50-Mbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$  |     | 84  | 103 | mA   |
| Bus-side supply current                        | ISO145x, D = 50-Mbps square wave with 50% duty cycle, $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ , $V_{CC2} = 5\text{ V} \pm 10\%$    |     | 134 | 162 | mA   |
| <b>DRIVER DISABLED, BUS LOADED OR UNLOADED</b> |  |     |     |     |      |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $V_{CC2} = 3.3\text{ V} \pm 10\%$  |     | 2.6 | 4.3 | mA   |
| Bus-side supply current                        | $V_D = V_{CC1}$ , $V_{CC2} = 5\text{ V} \pm 10\%$  |     | 2.8 | 4.5 | mA   |

### 8.13 Switching Characteristics: Driver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^{\circ}C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER               | TEST CONDITIONS   | MIN  | TYP | MAX | UNIT |    |
|-------------------------|---|--|-----|-----|------|----|
| <b>500-kbps DEVICES</b> |   |  |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 460 | 680  | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 310 | 570  | ns |
| PWD                     | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 4   | 50   | ns |
| $t_{PHZ}, t_{PLZ}$      | Disable time  | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 125 | 200  | ns |
| $t_{PZH}, t_{PZL}$      | Enable time   | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 160 | 600  | ns |
| <b>12-Mbps DEVICES</b>  |   |  |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $R_L = 54 \Omega, C_L = 50 \text{ pF}, V_{CC2} = 4.5 \text{ V to } 5.5 \text{ V}$ , see <a href="#">图 37</a> |     | 10  | 25   | ns |
|                         |   | $R_L = 54 \Omega, C_L = 50 \text{ pF}, V_{CC2} = 3 \text{ V to } 3.6 \text{ V}$ , see <a href="#">图 37</a>   |     |     | 27.8 | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 68  | 125  | ns |
| PWD                     | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 2   | 10   | ns |
| $t_{PHZ}, t_{PLZ}$      | Disable time  | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 75  | 125  | ns |
| $t_{PZH}, t_{PZL}$      | Enable time   | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 75  | 160  | ns |
| <b>50-Mbps DEVICES</b>  |   |  |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $R_L = 54 \Omega, C_L = 50 \text{ pF}, V_{CC2} = 4.5 \text{ V to } 5.5 \text{ V}$ , see <a href="#">图 37</a> |     | 4.7 | 6    | ns |
|                         |   | $R_L = 54 \Omega, C_L = 50 \text{ pF}, V_{CC2} = 3 \text{ V to } 3.6 \text{ V}$ , see <a href="#">图 37</a>   |     |     | 7.8  | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 19  | 41   | ns |
| PWD                     | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $R_L = 54 \Omega, C_L = 50 \text{ pF}$ , see <a href="#">图 37</a>  |     | 1   | 6    | ns |
| $t_{PHZ}, t_{PLZ}$      | Disable time  | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 25  | 46   | ns |
| $t_{PZH}, t_{PZL}$      | Enable time   | See <a href="#">图 40</a> , and <a href="#">图 41</a>  |     | 32  | 78   | ns |

(1) Also known as pulse skew.

### 8.14 Switching Characteristics: Receiver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^{\circ}C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER               | TEST CONDITIONS   | MIN   | TYP | MAX | UNIT |    |
|-------------------------|---|---|-----|-----|------|----|
| <b>500-kbps DEVICES</b> |   |   |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 1   | 4    | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 92  | 135  | ns |
| PWD                     | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 4.5 | 12.5 | ns |
| $t_{PHZ}, t_{PLZ}$      | Disable time  | See <a href="#">图 43</a> and <a href="#">图 44</a> |     | 9   | 30   | ns |
| $t_{PZH}, t_{PZL}$      | Enable time   | See <a href="#">图 43</a> and <a href="#">图 44</a> |     | 5   | 20   | ns |
| <b>12-Mbps DEVICES</b>  |   |   |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 1   | 4    | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 75  | 120  | ns |
| PWD                     | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 1   | 10   | ns |
| $t_{PHZ}, t_{PLZ}$      | Disable time  | See <a href="#">图 43</a> and <a href="#">图 44</a> |     | 9   | 30   | ns |
| $t_{PZH}, t_{PZL}$      | Enable time   | See <a href="#">图 43</a> and <a href="#">图 44</a> |     | 5   | 20   | ns |
| <b>50-Mbps DEVICES</b>  |   |   |     |     |      |    |
| $t_r, t_f$              | Differential output rise time and fall time                   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 1   | 4    | ns |
| $t_{PHL}, t_{PLH}$      | Propagation delay   | $C_L = 15 \text{ pF}$ , see <a href="#">图 42</a>  |     | 36  | 60   | ns |

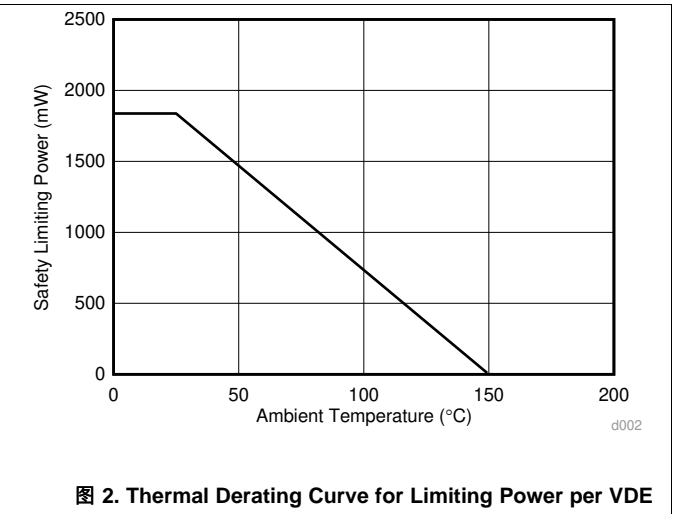
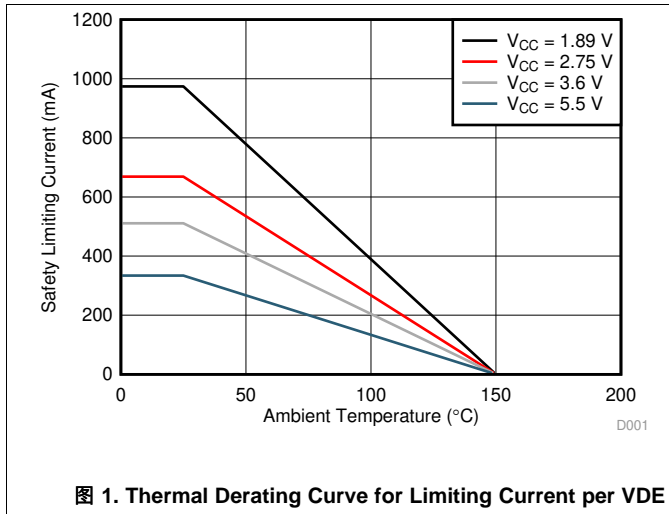
(1) Also known as pulse skew.

## Switching Characteristics: Receiver (continued)

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^{\circ}C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|-----|-----|------|
| PWD                   | Pulse width distortion <sup>(1)</sup> , $ t_{PHL} - t_{PLH} $ | $C_L = 15$ pF, Measured with 50kHz, 50% Duty Clock, see 图 42 |     | 2   | 6   | ns   |
| $t_{PHZ}$ , $t_{PLZ}$ | Disable time  | See 图 43 and 图 44  |     | 9   | 30  | ns   |
| $t_{PZH}$ , $t_{PZL}$ | Enable time   | See 图 43 and 图 44  |     | 5   | 20  | ns   |

## 8.15 Insulation Characteristics Curves





### 8.16 Typical Characteristics

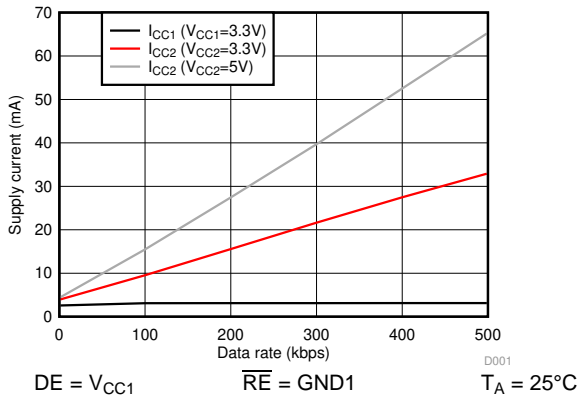


图 3. ISO141x Supply Current Vs Data Rate- No Load

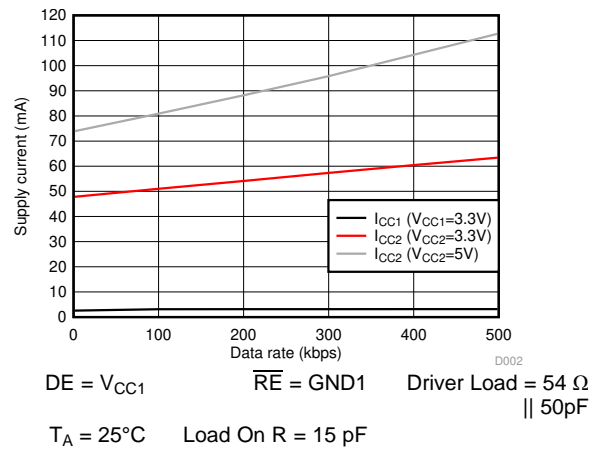


图 4. ISO141x Supply Current Vs Data Rate- With  $54\Omega||50pF$  Load

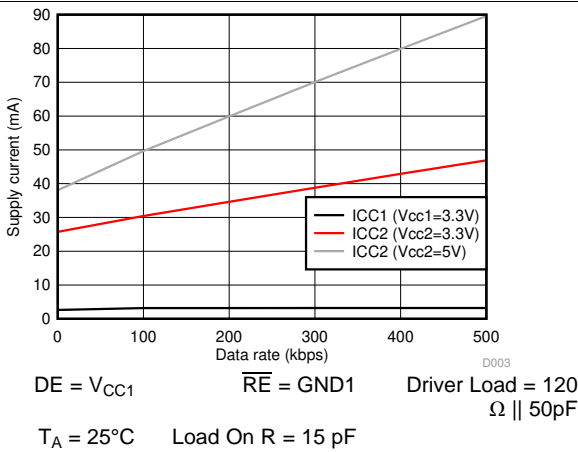


图 5. ISO141x Supply Current Vs Data Rate- With  $120\Omega||50pF$  Load

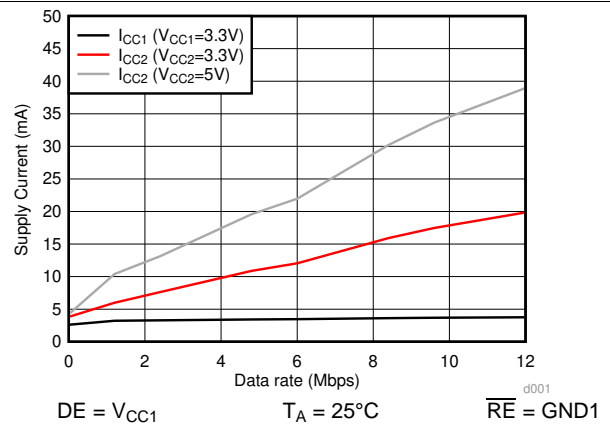


图 6. ISO143x Supply Current Vs. Data Rate - No Load

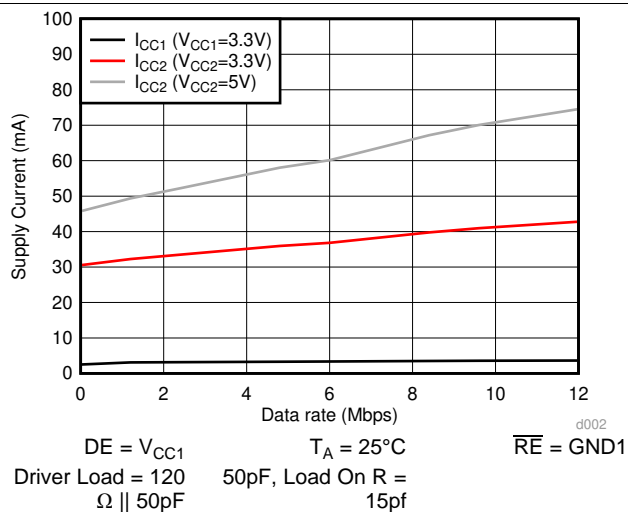


图 7. ISO143x Supply Current Vs. Data Rate -  $120\Omega||50pF$  Load

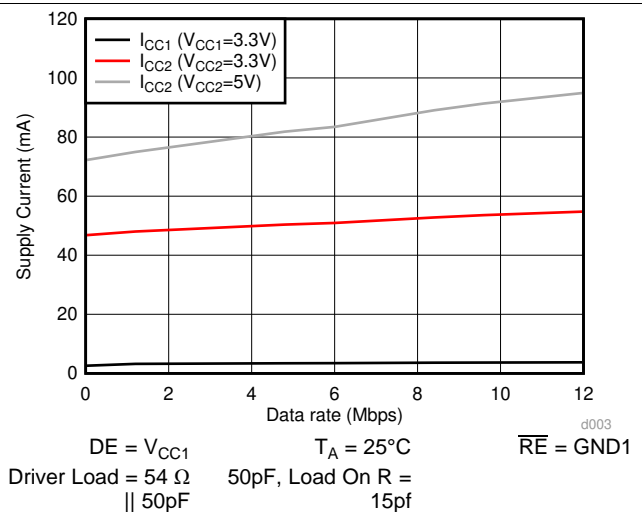


图 8. ISO143x Supply Current Vs Data Rate-  $54\Omega||50pF$  Load

Typical Characteristics (接下页)

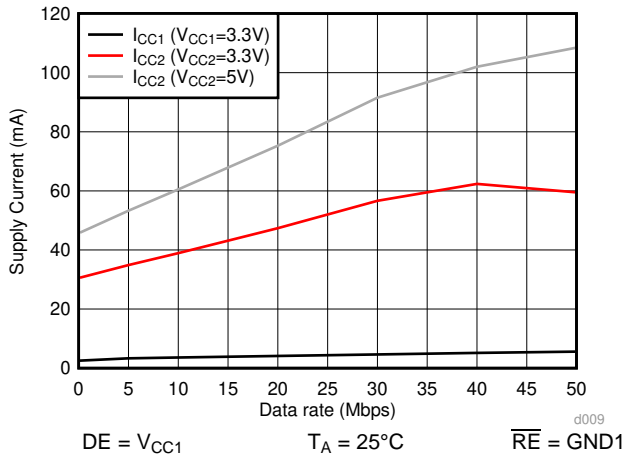


图 9. ISO145x Supply Current Vs Data Rate- No Load

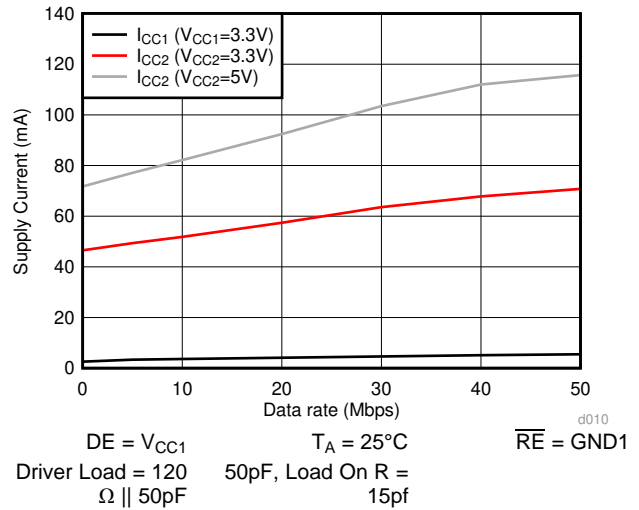


图 10. ISO145x Supply Current Vs Data Rate- 120Ω||50pF Load

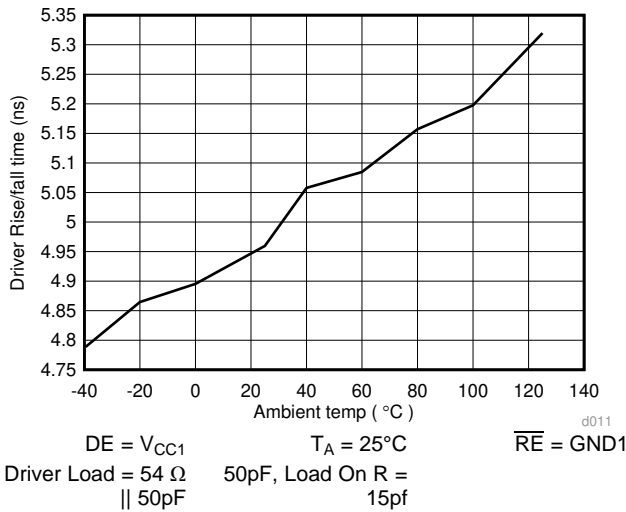


图 11. ISO145x Supply Current Vs Data Rate- 54Ω||50pF Load

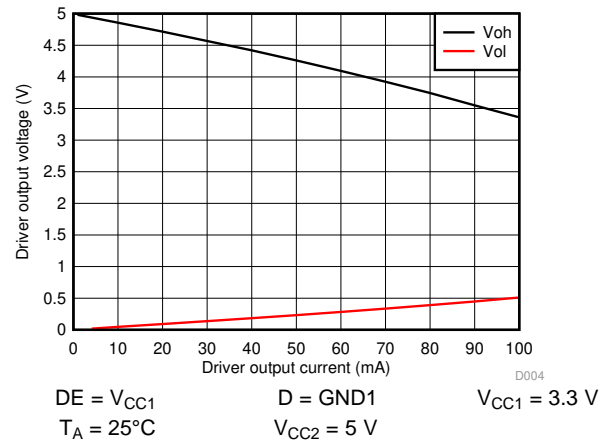


图 12. Driver Output Voltage Vs Driver Output Current

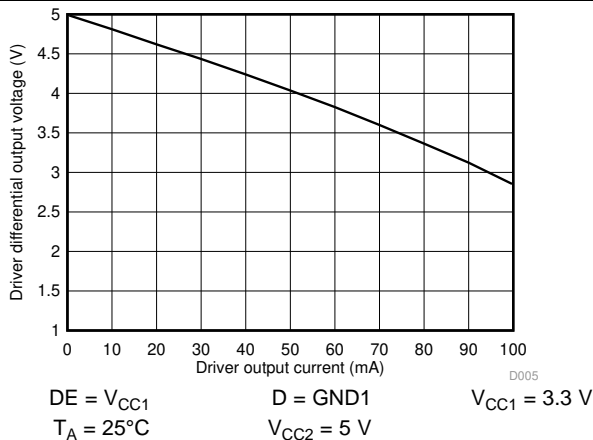


图 13. Driver Differential Output Voltage Vs Driver Output Current

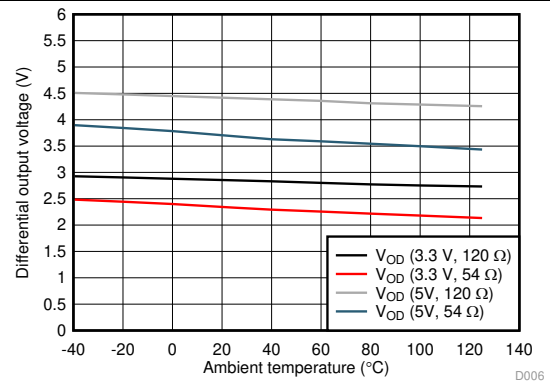


图 14. Driver Differential Output Voltage Vs Temperature

Typical Characteristics (接下页)

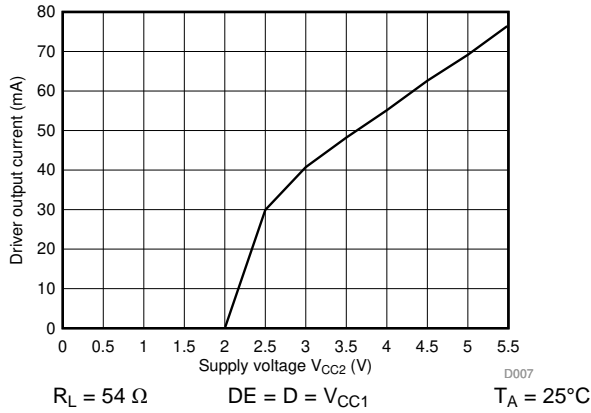


图 15. Driver Output Current Vs Supply Voltage ( $V_{CC2}$ )

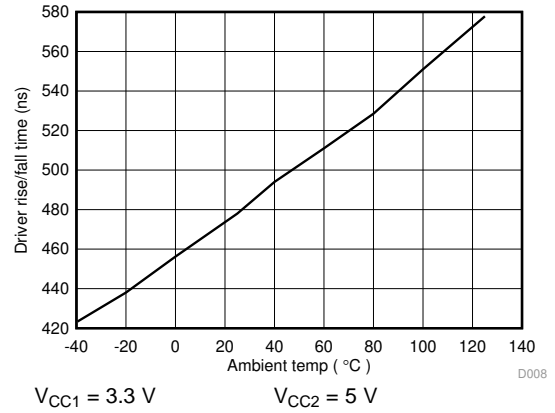


图 16. ISO141x Driver Rise/fall Time (ns) Vs Temperature (c)

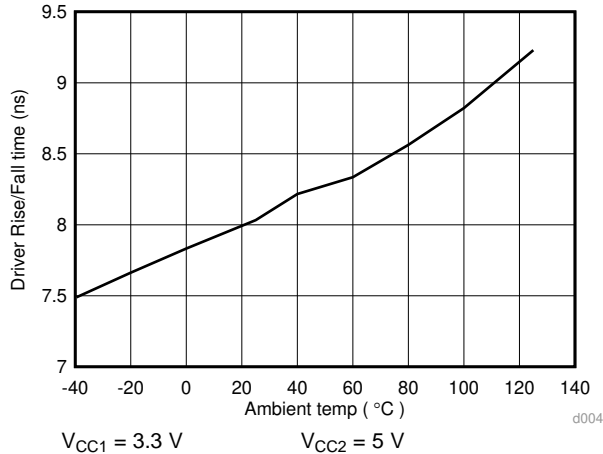


图 17. ISO143x Driver Rise/Fall Time (ns) Vs Temperature (C)

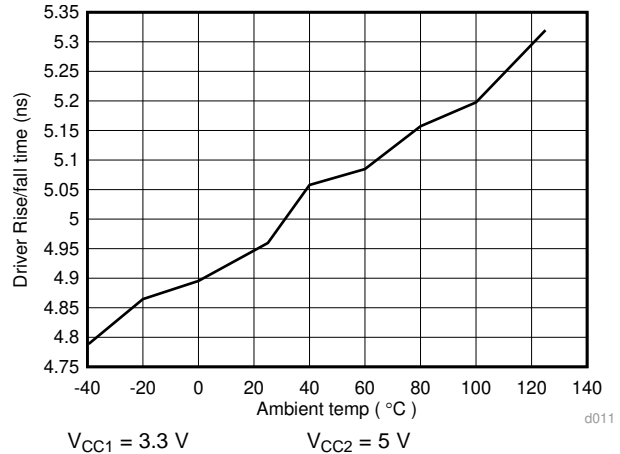


图 18. ISO145x Driver Rise/Fall Time (ns) Vs Temperature (C)

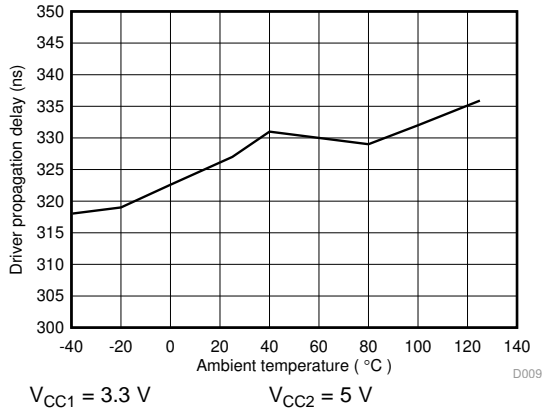


图 19. ISO141x Driver Propagation Delay (ns) Vs Temperature (c)

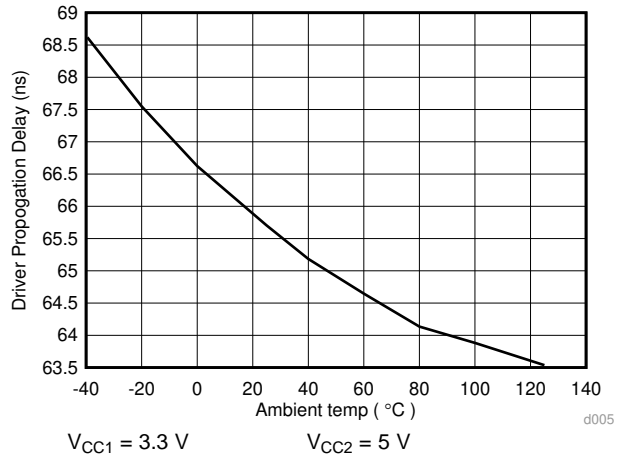


图 20. ISO143x Driver Propagation Delay (ns) Vs Temperature (C)

Typical Characteristics (接下页)

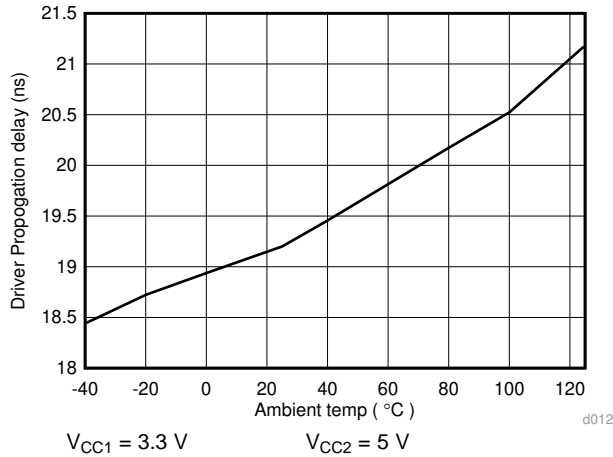


图 21. ISO145x Driver Propagation Delay (ns) Vs Temperature (C)

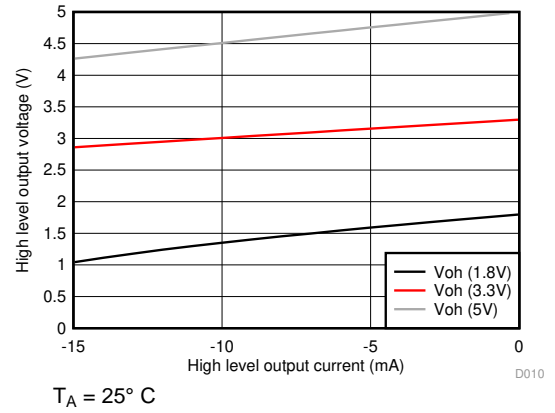


图 22. Receiver Buffer High Level Output Voltage Vs High Level Output Current

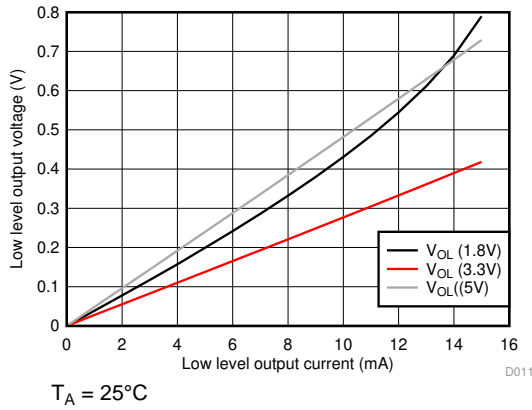


图 23. Receiver Buffer Low Level Output Voltage Vs Low Level Output Current

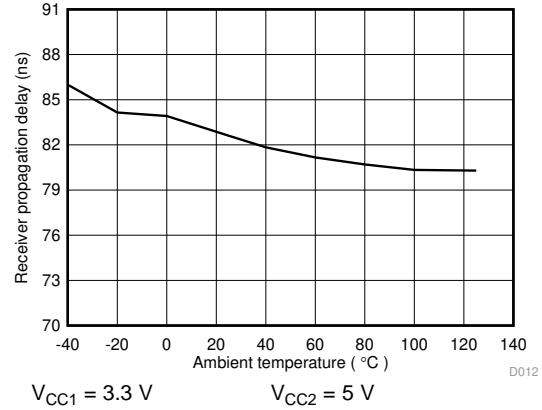


图 24. ISO141x Receiver Propagation Delay (ns) Vs Temperature (c)

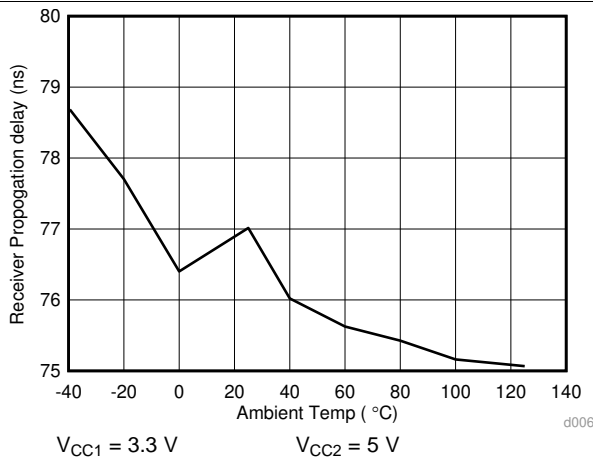


图 25. ISO143x Receiver Propagation Delay (ns) Vs. Temperature (C)

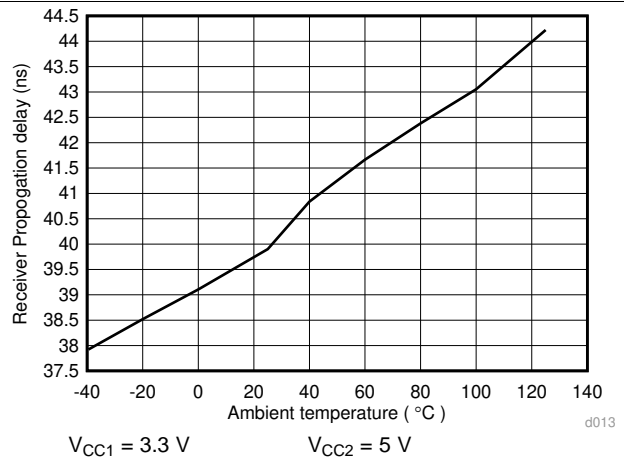


图 26. ISO145x Receiver Propagation Delay (ns) Vs. Temperature (C)

Typical Characteristics (接下页)

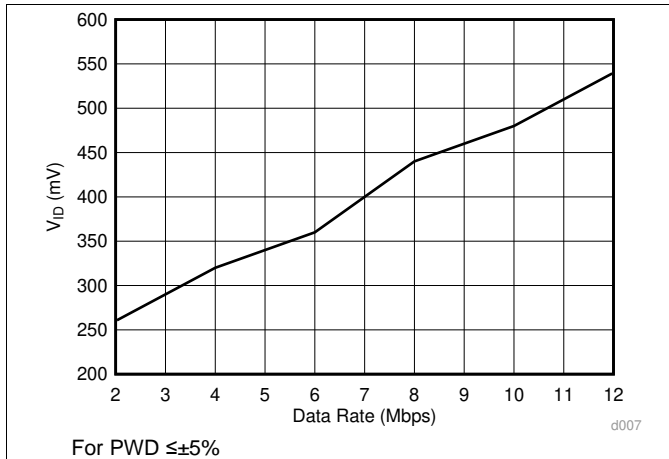


图 27. ISO143x Receiver  $V_{ID}$  vs Signaling Rate

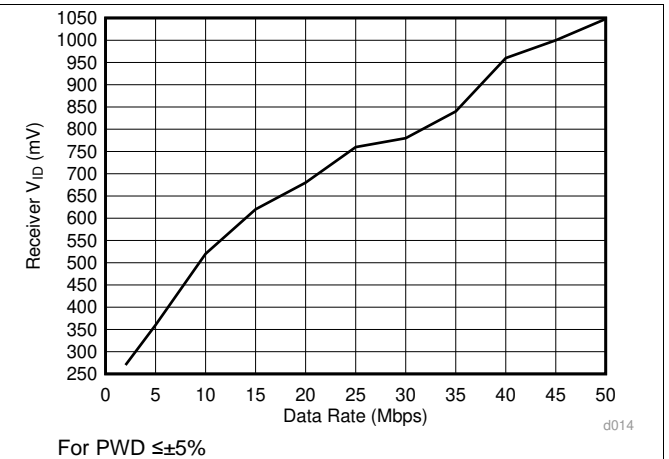


图 28. ISO145x Receiver  $V_{ID}$  vs Signaling Rate

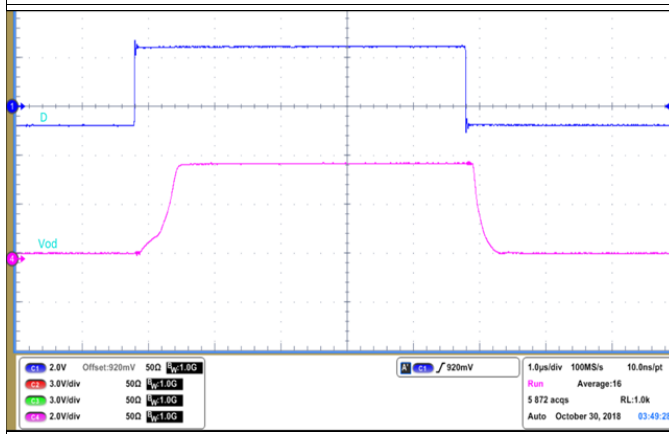


图 29. ISO141x Driver Propagation Delay

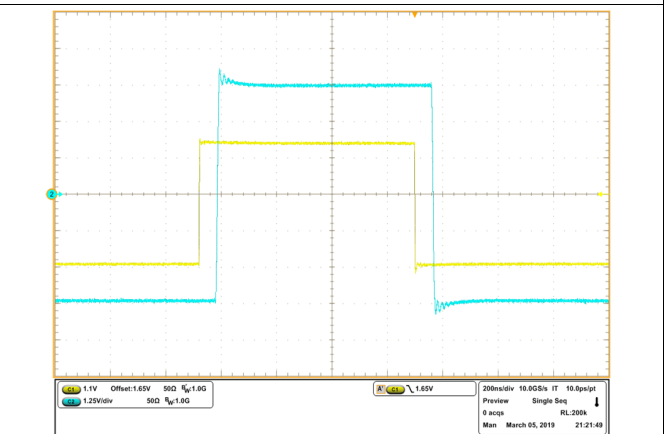


图 30. ISO143x Driver Propagation Delay

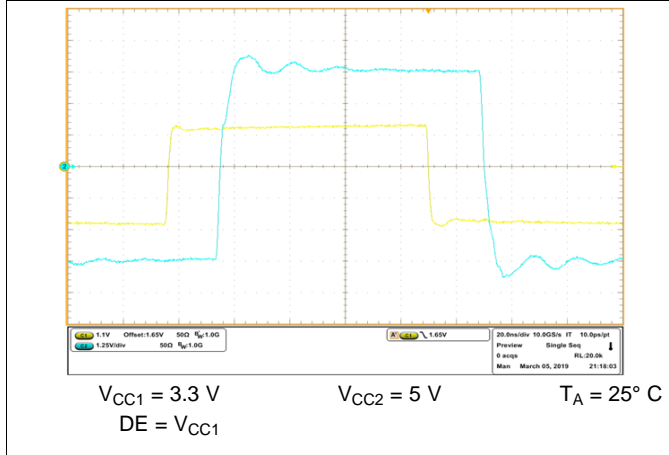


图 31. ISO145x Driver Propagation Delay

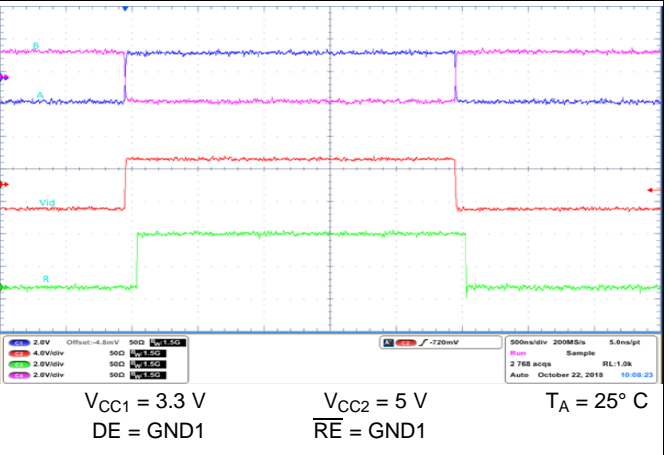


图 32. ISO141x Receiver Propagation Delay

Typical Characteristics (接下页)

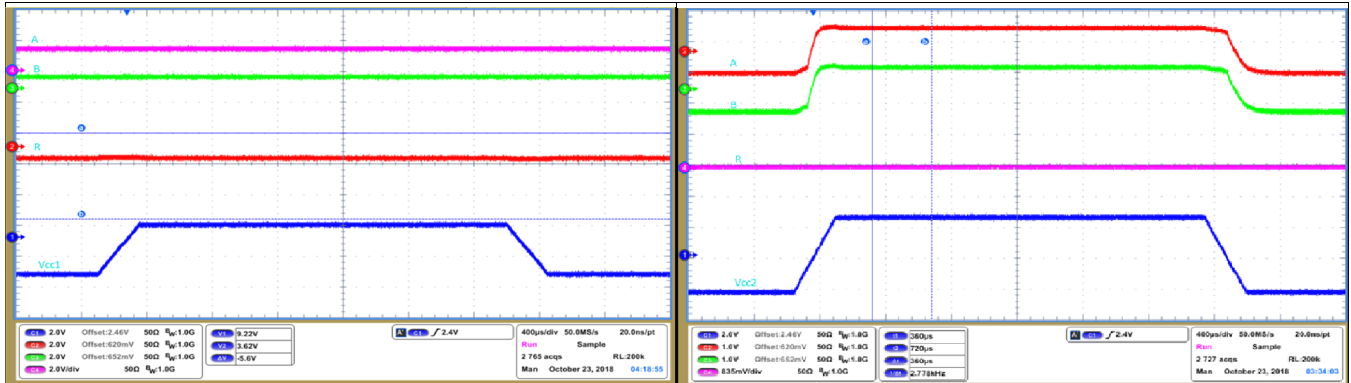


图 33. V<sub>CC1</sub> Power Up/Power Down - Glitch Free Behavior

图 34. V<sub>CC2</sub> Power Up/Power Down - Glitch Free Behavior

## 9 Parameter Measurement Information

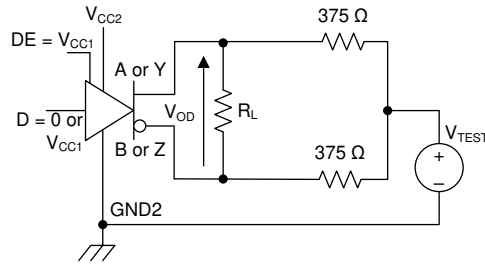
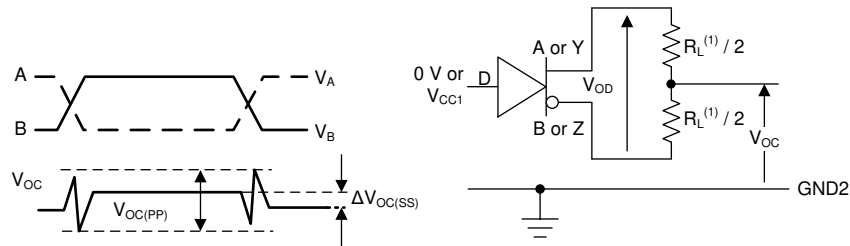
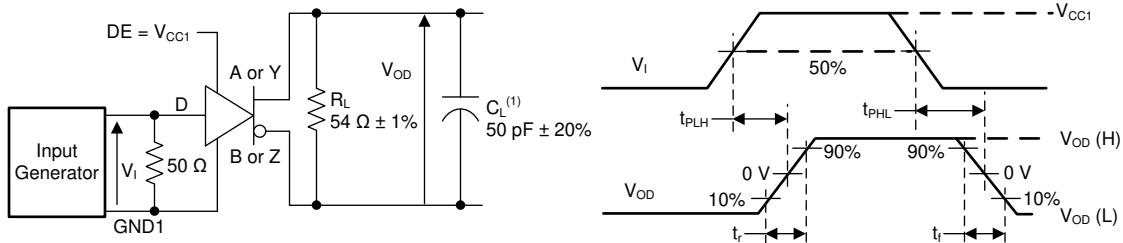


图 35. Driver Voltages



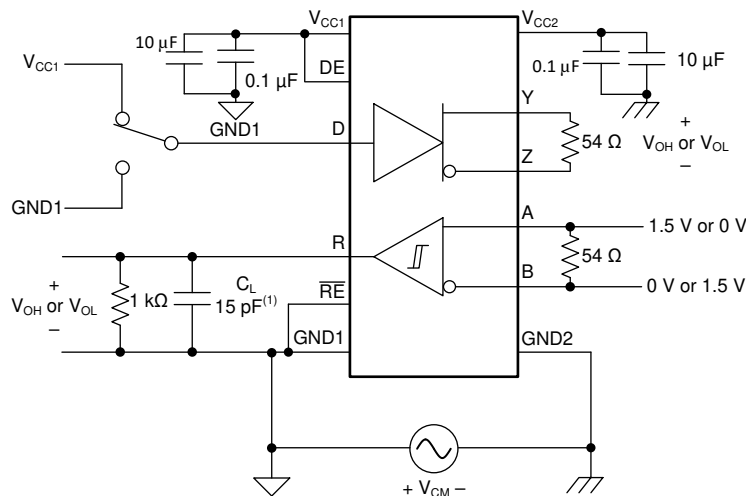
(1)  $R_L = 100 \Omega$  for RS422,  $R_L = 54 \Omega$  for RS-485

图 36. Driver Voltages



(1)  $C_L$  includes fixture and instrumentation capacitance.

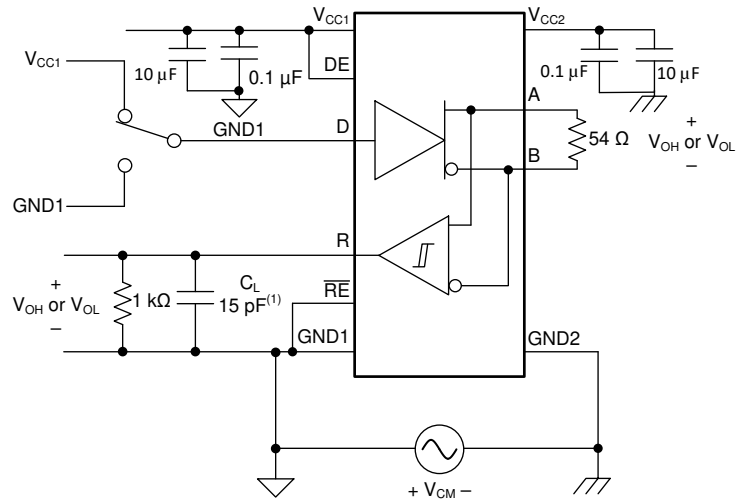
图 37. Driver Switching Specifications



(1) Includes probe and fixture capacitance.

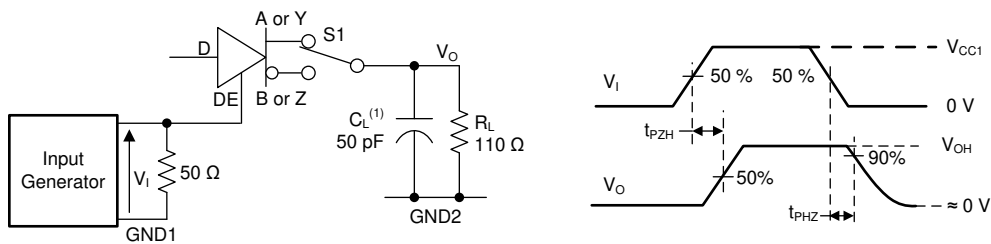
图 38. Common Mode Transient Immunity (CMTI)—Full Duplex

Parameter Measurement Information (接下页)



(1) Includes probe and fixture capacitance.

图 39. Common Mode Transient Immunity (CMTI)—Half Duplex



(1)  $C_L$  includes fixture and instrumentation capacitance

图 40. Driver Enable and Disable Times

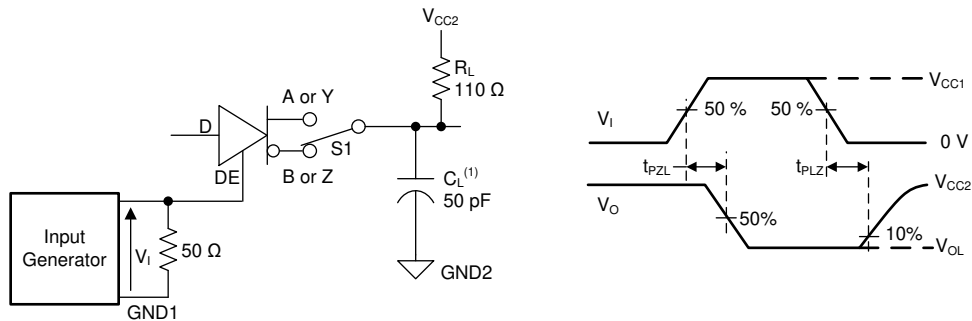
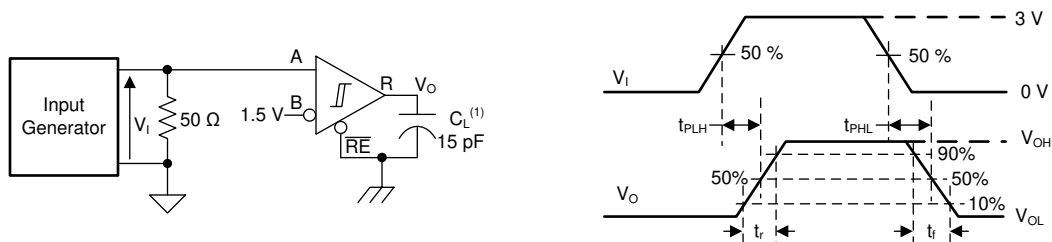


图 41. Driver Enable and Disable Times



Parameter Measurement Information (接下页)



(1)  $C_L$  includes fixture and instrumentation capacitance.

图 42. Receiver Switching Specifications

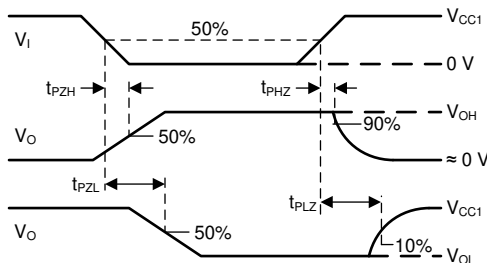


图 43. Receiver Enable and Disable Times

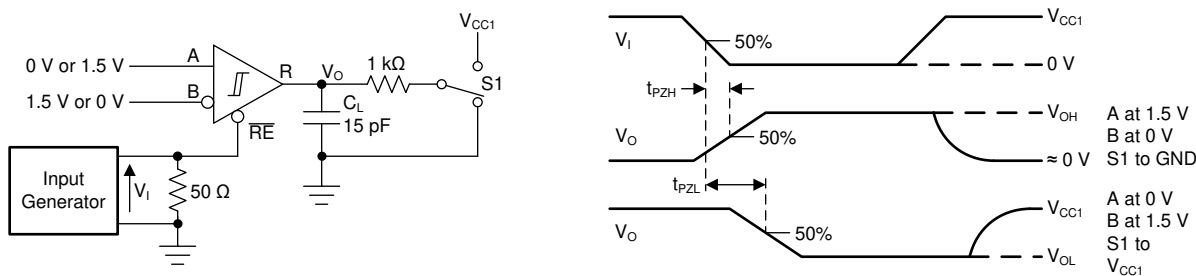
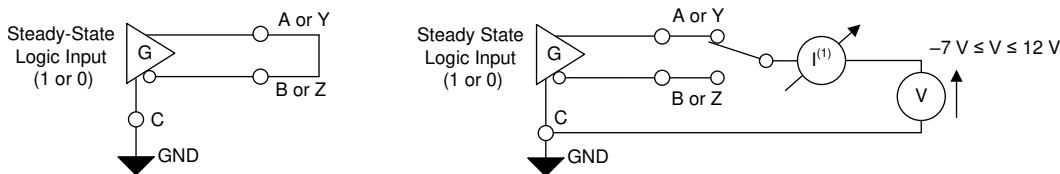


图 44. Receiver Enable and Disable Times



(1) The driver should not sustain any damage with this configuration.

图 45. Short-Circuit Current Limiting

## 10 Detailed Description

### 10.1 Overview

The ISO14xx devices are isolated RS-485/RS-422 transceivers designed to operate in harsh industrial environments. ISO141x, ISO143x and ISO145x devices support up to 500 kbps, 12 Mbps and 50 Mbps signaling rates respectively. This family of devices has a 3-channel digital isolator and an RS-485 transceiver in a 16-pin wide-body SOIC package. The silicon-dioxide based capacitive isolation barrier supports an isolation withstand voltage of 5 kV<sub>RMS</sub> and an isolation working voltage of 1500 V<sub>PK</sub>. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. These devices have a higher typical differential output voltage ( $V_{OD}$ ) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified at a  $V_{CC2}$  voltage of 5 V  $\pm$ 10% which meets the requirements for Profibus applications. The wide logic supply of the device ( $V_{CC1}$ ) supports interfacing with 1.8-V, 2.5-V, 3.3-V, and 5-V control logic. The 3-V to 5.5-V bus side supply ( $V_{CC2}$ ) removes the need of a well-regulated isolated supply in end systems. 图 46 shows the functional block diagram of the full-duplex devices and 图 47 shows the functional block diagram of a half-duplex devices.

### 10.2 Functional Block Diagram

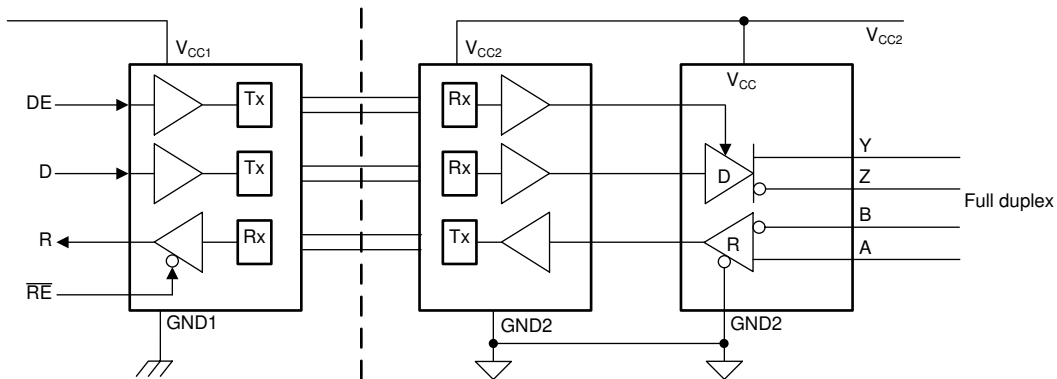


图 46. Full-Duplex Block Diagram

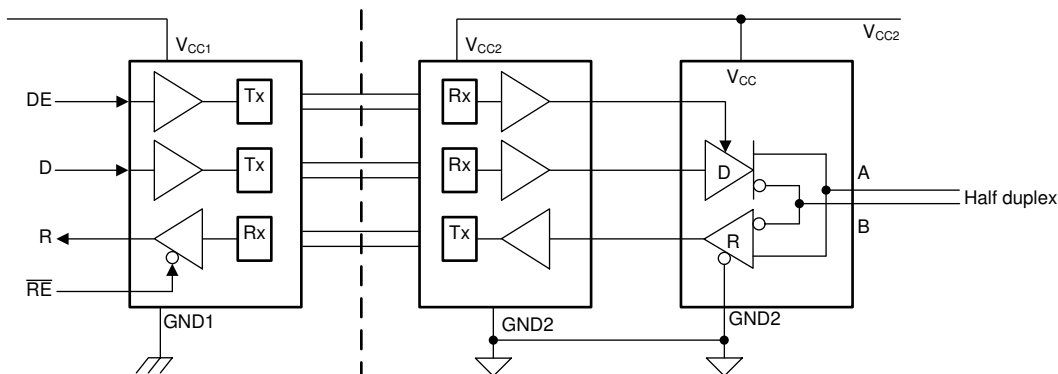


图 47. Half-Duplex Block Diagram

## 10.3 Feature Description

### 10.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO14xx devices incorporate dedicated circuitry to protect the transceiver from  $\pm 16$  kV ESD per IEC61000-4-2 and  $\pm 4$  kV EFT per IEC 61000-4-4. System designers can achieve the  $\pm 4$ -kV EFT Criterion A with careful system design (data communication between nodes in the presence of transient noise with minimum to no data loss).

### 10.3.2 Failsafe Receiver

The differential receiver of the ISO14xx devices has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

The receiver thresholds are offset in the receiver failsafe protection so that the indeterminate range of the does not include a 0 V differential. The receiver output must generate a logic high when the differential input ( $V_{ID}$ ) is greater than 200 mV to comply with the RS-485 standard. The receiver output must also generate a output a logic low when  $V_{ID}$  is less than  $-200$  mV to comply with the RS-485 standard. The receiver parameters that determine the failsafe performance are  $V_{TH+}$ ,  $V_{TH-}$ , and  $V_{HYS}$ . Differential signals less than  $-200$  mV always cause a low receiver output as shown in the *Electrical Characteristics* table. Differential signals greater than 200 mV always cause a high receiver output. A differential input signal that is near zero is still greater than the  $V_{TH+}$  threshold which makes the receiver output logic high. The receiver output goes to a low state only when the differential input decreases by  $V_{HYS}$  to less than  $V_{TH+}$ .

The internal failsafe biasing feature removes the need for the two external resistors that are typically required with traditional isolated RS-485 transceivers as shown in 图 48.

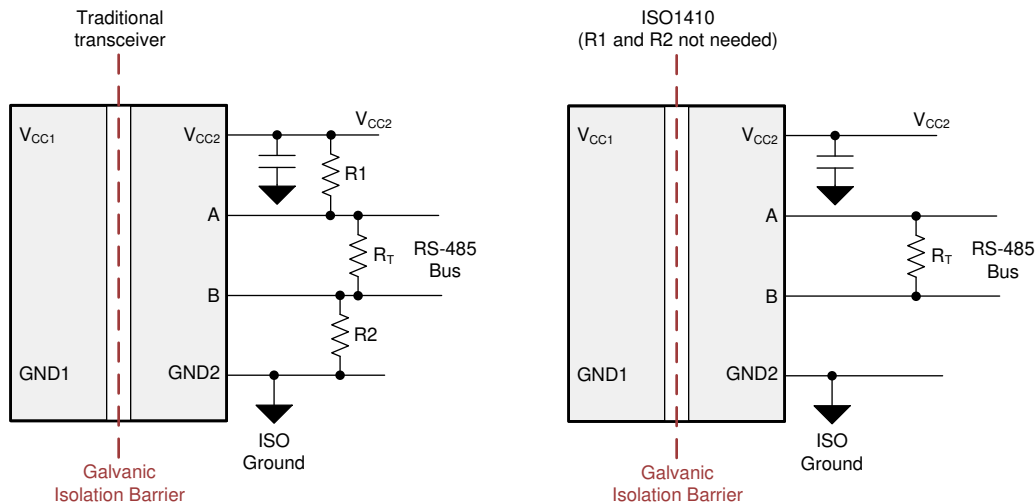


图 48. Failsafe Transceiver

### 10.3.3 Thermal Shutdown

The ISO14xx devices have a thermal shutdown circuit to protect against damage when a fault condition occurs. A driver output short circuit or bus contention condition can cause the driver current to increase significantly which increases the power dissipation inside the device. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 170°C (typical) which lets the device decrease the temperature. The device is enabled when the junction temperature becomes 165°C (typical).

## Feature Description (接下页)

Bus short circuit for an extended duration and/or beyond voltage levels specified in recommended operating condition should be avoided. Repeated or prolonged exposure to bus shorts can result in high junction temperatures and affect device reliability.

### 10.3.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a master node and slave node in an RS485 network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

The ISO14xx devices do not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates from 100  $\mu$ s to 10 ms.

## 10.4 Device Functional Modes

表 2 shows the driver functional modes.

表 2. Driver Functional table<sup>(1)</sup>

| V <sub>CC1</sub>  | V <sub>CC2</sub> | INPUT D | DRIVER ENABLE DE | OUTPUTS <sup>(2)</sup> |      |
|-------------------|------------------|---------|------------------|------------------------|------|
|                   |                  |         |                  | Y, A                   | Z, B |
| PU                | PU               | H       | H                | H                      | L    |
|                   |                  | L       | H                | L                      | H    |
|                   |                  | X       | L                | Hi-Z                   | Hi-Z |
|                   |                  | X       | Open             | Hi-Z                   | Hi-Z |
|                   |                  | Open    | H                | H                      | L    |
| PD <sup>(3)</sup> | PU               | X       | X                | Hi-Z                   | Hi-Z |
| X                 | PD               | X       | X                | Hi-Z                   | Hi-Z |

(1) PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state

(2) The driver outputs are Y and Z for a full-duplex device. The driver outputs are A and B for a half-duplex device.

(3) A strongly driven input signal can weakly power the floating V<sub>CC1</sub> through an internal protection diode and cause an undetermined output.

The description that follows is specific to half-duplex device but the same logic applies to full-duplex device with the outputs being Y and Z.

When the driver enable pin, DE, is logic high, the differential outputs, A and B, follow the logic states at data input, D. A logic high at the D input causes the A output to go high and the B output to go low. Therefore the differential output voltage defined by 公式 1 is positive.

$$V_{OD} = V_A - V_B \quad (1)$$

A logic low at the D input causes the B output to go high and the A output to go low. Therefore the differential output voltage defined by 公式 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The A output goes high and the B output goes low when the D pin is left open while the driver enabled.

表 3 shows the receiver functional modes.

**表 3. Receiver Functional Table<sup>(1)</sup>**

| $V_{CC1}$         | $V_{CC2}$ | DIFFERENTIAL INPUT                       | RECEIVER ENABLE $\overline{RE}$ | OUTPUT R      |
|-------------------|-----------|--|---------------------------------|---------------|
|                   |           | $V_{ID} = V_A - V_B$                     |                                 |               |
| PU                | PU        | $-0.02\text{ V} \leq V_{ID}$             | L                               | H             |
|                   |           | $-0.2\text{ V} < V_{ID} < 0.02\text{ V}$ | L                               | Indeterminate |
|                   |           | $V_{ID} \leq -0.2\text{ V}$              | L                               | L             |
|                   |           | X  | H                               | Hi-Z          |
|                   |           | X  | Open                            | Hi-Z          |
|                   |           | Open, Short, Idle                        | L                               | H             |
| PD <sup>(2)</sup> | PU        | X  | X                               | Hi-Z          |
| PU                | PD        | X  | L                               | H             |
| PD <sup>(2)</sup> | PD        | X  | X                               | Hi-Z          |

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state

(2) A strongly driven input signal can weakly power the floating  $V_{CC1}$  through an internal protection diode and cause an undetermined output.

The receiver is enabled when the receiver enable pin,  $\overline{RE}$ , is logic low. The receiver output, R, goes high when the differential input voltage defined by 公式 2 is greater than the positive input threshold,  $V_{TH+}$ .

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by 公式 2 is less than the negative input threshold,  $V_{TH-}$ . If the  $V_{ID}$  voltage is between the  $V_{TH+}$  and  $V_{TH-}$  thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of  $V_{ID}$  are irrelevant when the  $\overline{RE}$  pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

10.4.1 Device I/O Schematics

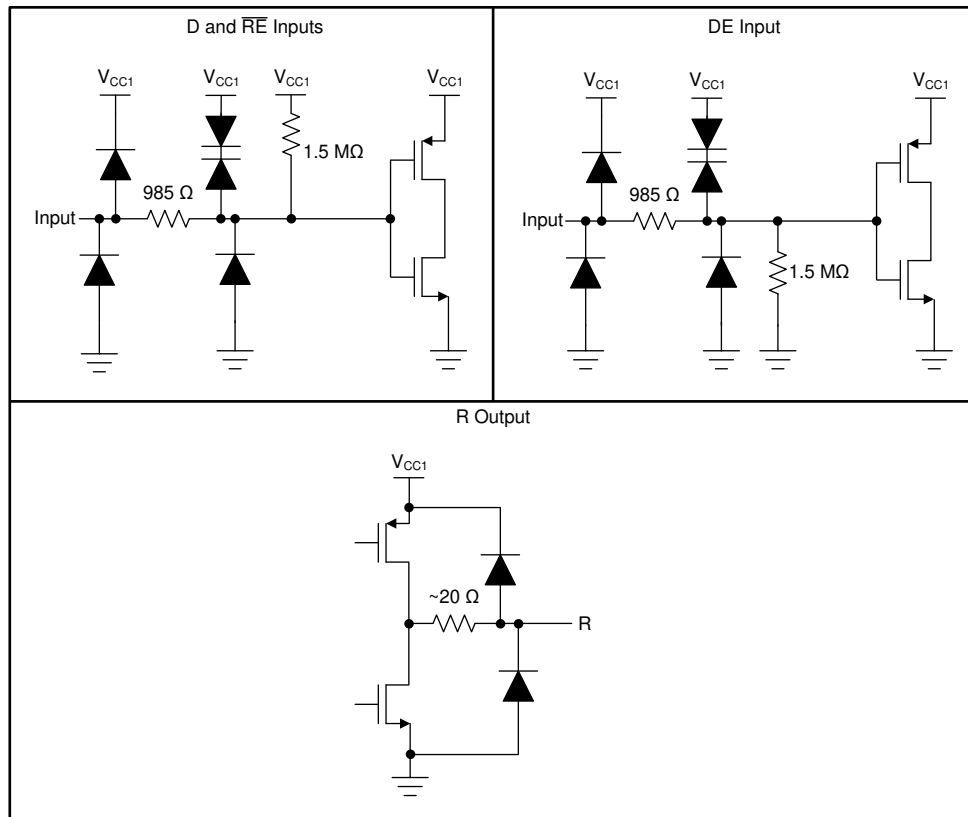


图 49. Device I/O Schematics

## 11 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 11.1 Application Information

The ISO14xx devices are designed for bidirectional data transfer on multipoint RS-485 networks. The design of each RS-485 node in the network requires an ISO14xx device and an isolated power supply as shown in 图 52.

An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor,  $R_T$ , to remove line reflections. The value of  $R_T$  matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

Full-duplex implementation, as shown in 图 50, requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair. In half-duplex implementation, as shown in 图 51, the driver and receiver enable pins let any node at any given moment be configured in either transmit or receive mode which decreases cable requirements.

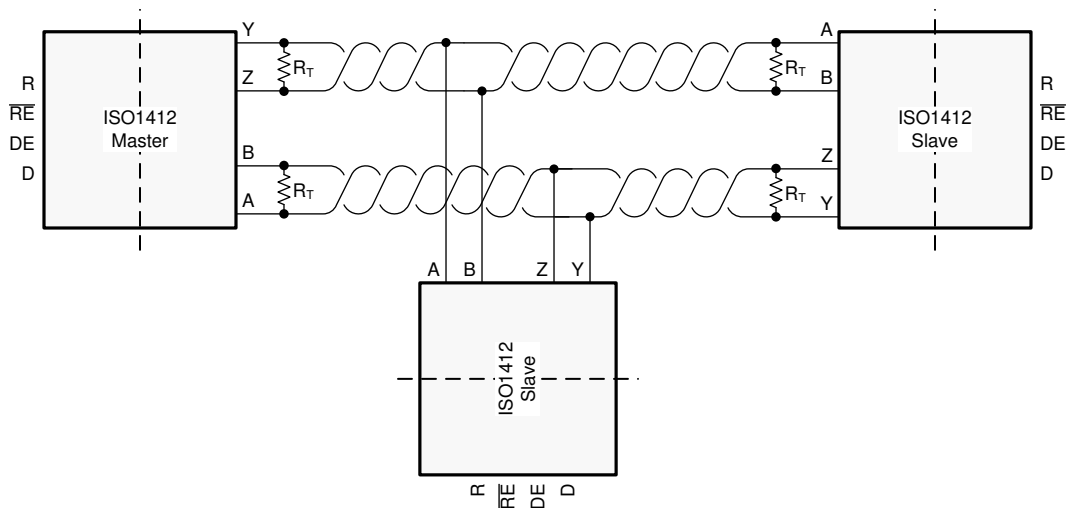


图 50. Typical RS-485 Network With Full-Duplex Isolated Transceivers

## Application Information (接下页)

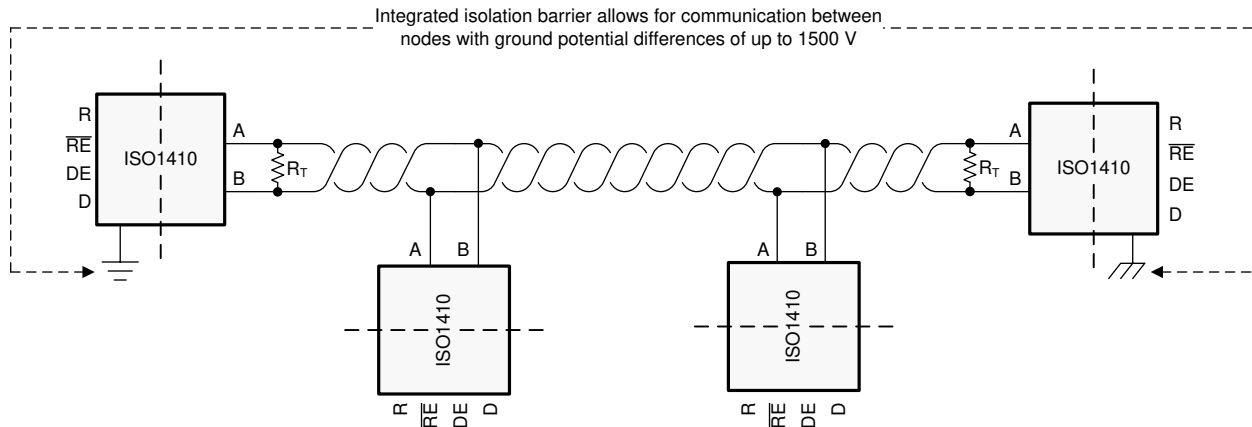


图 51. Typical RS-485 Network With Half-Duplex Isolated Transceivers

## 11.2 Typical Application

图 52 shows the application circuit of the ISO1410 device.

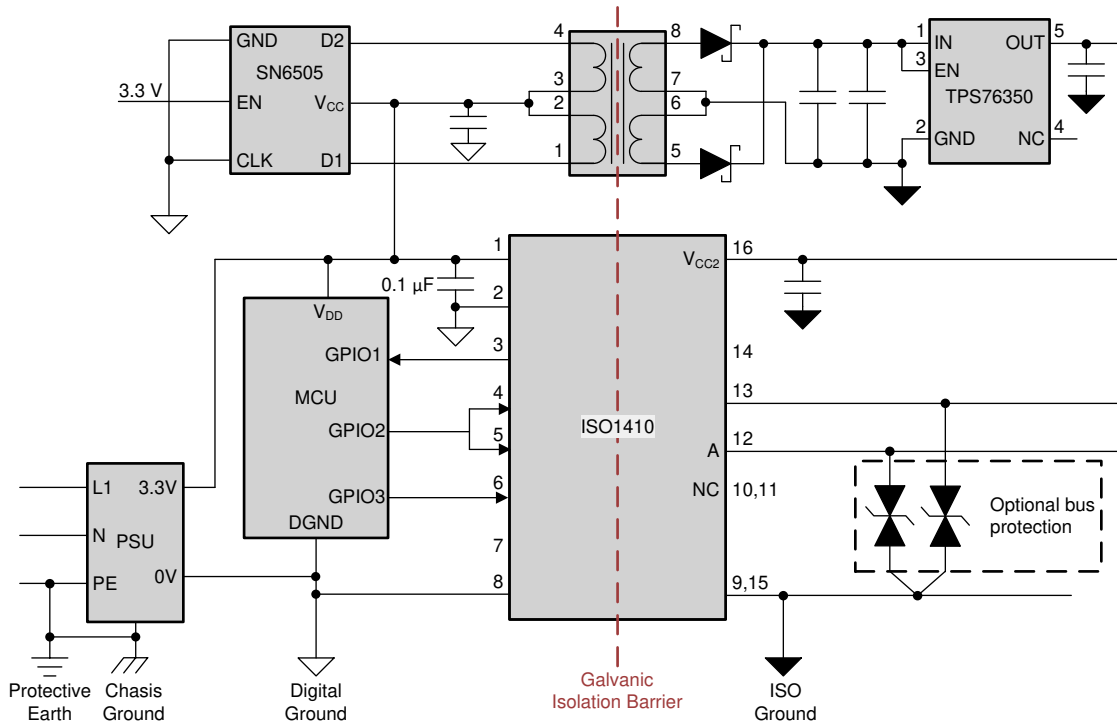


图 52. Application Circuit of ISO1410

### 11.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISO14xx devices only require external bypass capacitors to operate.



## Typical Application (接下页)

### 11.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface suitable for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

#### 11.2.2.1 Data Rate and Bus Length

The RS-485 standard has typical curves similar to those shown in 图 53. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer.

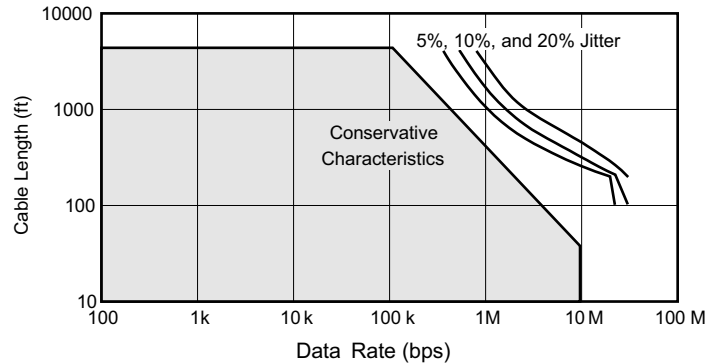


图 53. Cable Length vs Data Rate Characteristics

Use 图 53 as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

#### 11.2.2.2 Stub Length

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the *stub*. The stub should be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length ( $L_{(STUB)}$ ) is calculated as shown in 公式 3.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c$$

where

- $t_r$  is the 10/90 rise time of the driver.
  - $c$  is the speed of light ( $3 \times 10^8$  m/s).
  - $v$  is the signal velocity of the cable or trace as a factor of  $c$ .
- (3)

#### 11.2.2.3 Bus Loading

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12 k $\Omega$ . Standard-compliant drivers must be able to drive 32 of these ULs.

The ISO14xx devices have 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

### 11.2.3 Application Curves

Below eye diagram of ISO145x device indicates low jitter and wide open eye at maximum data rate of 50 Mbps.

Typical Application (接下页)

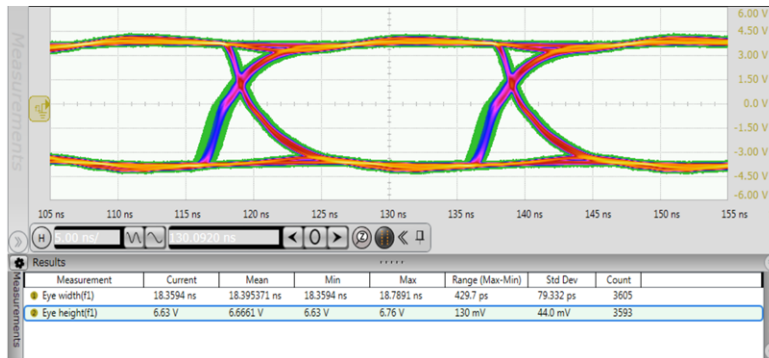


图 54. Eye Diagram at 50 Mbps Clock,  $V_{CC2} = 5\text{ V}$ ,  $25^\circ\text{C}$

11.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 55 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

图 56 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1060  $V_{RMS}$  with a lifetime of 220 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 is specified up to 1060  $V_{RMS}$ . At the lower working voltages, the corresponding insulation lifetime is much longer than 220 years.

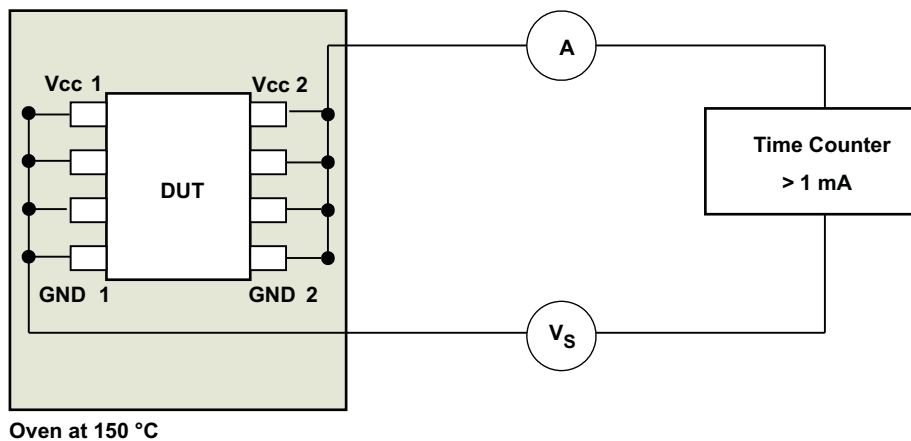
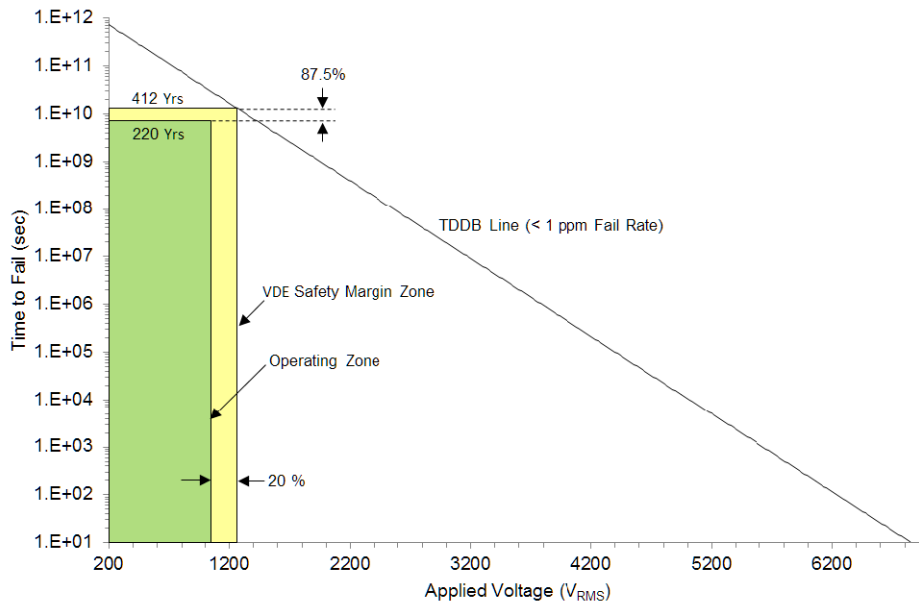


图 55. Test Setup for Insulation Lifetime Measurement

Typical Application (接下页)



Working Isolation Voltage = 1060 V<sub>RMS</sub>  
T<sub>A</sub> up to 150°C

Projected Insulation Lifetime = 220 Years  
Applied Voltage Frequency = 60 Hz

图 56. Insulation Lifetime Projection Data

## 12 Power Supply Recommendations

To make sure device operation is reliable at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the logic and transceiver supply pins (V<sub>CC1</sub> and V<sub>CC2</sub>). The capacitors should be placed as near to the supply pins as possible. Additionally, a 10 μF bulk capacitor on V<sub>CC2</sub> improves transceiver performance during bus transitions in transmit mode. If only one primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's [SN6505B](#) device. For such applications, detailed power supply design and transformer selection recommendations are available in the [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

## 13 Layout

### 13.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 57](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

## Layout Guidelines (continued)

Figure 58 shows the recommended placement and routing of the device bypass capacitors and optional TVS diodes. Put the  $V_{CC2}$  bypass capacitors on the top layer and as near to the device pins as possible. Do not use vias to complete the connection to the  $V_{CC2}$  and GND2 pins. If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the [Digital Isolator Design Guide](#) for detailed layout recommendations.

### 13.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 13.2 Layout Example

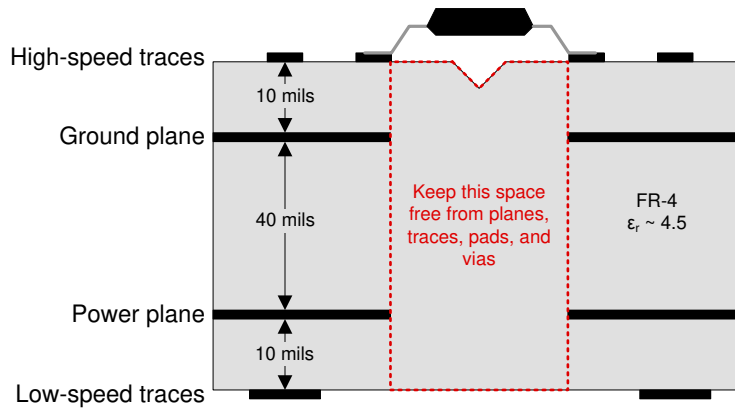


Figure 57. Recommended Layer Stack

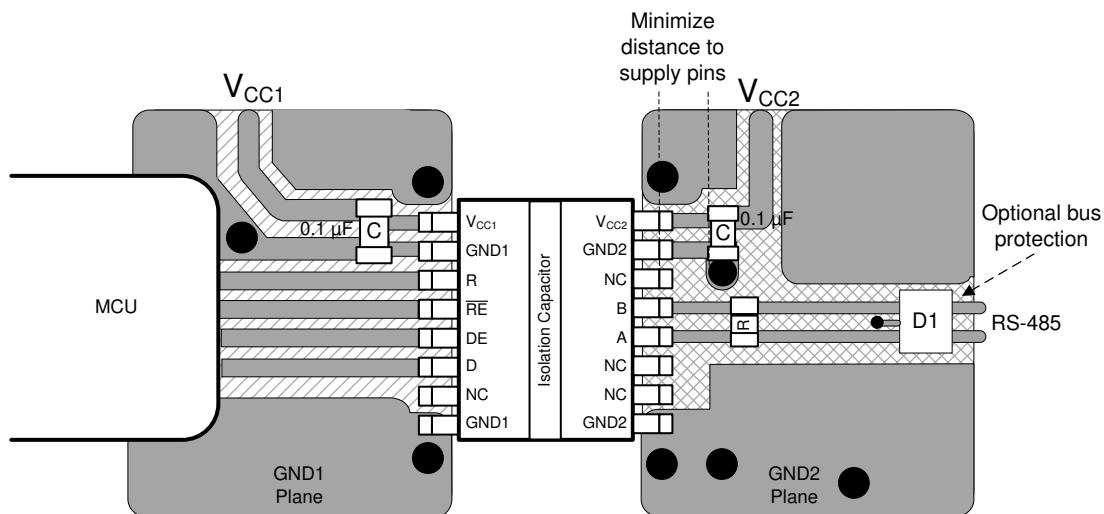


Figure 58. Layout Example

## 14 器件和文档支持

### 14.1 文档支持

#### 14.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI), 《数字隔离器设计指南》
- 德州仪器 (TI), 《隔离相关术语》
- 德州仪器 (TI), 《隔离式 RS-485 半双工评估模块》用户指南
- 德州仪器 (TI), 《如何隔离 RS-485 系统的信号和电源》TI 技术手册
- 德州仪器 (TI) 《适用于工业长途通信的可靠隔离式 RS-485》TI 技术手册

### 14.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 4. 相关链接

| 器件       | 产品文件夹                | 立即订购                 | 技术文档                 | 工具与软件                | 支持和社区                |
|----------|----------------------|----------------------|----------------------|----------------------|----------------------|
| ISO1410  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1412  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1430  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1432  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1450  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1452  | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1410B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1412B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1430B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1432B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1450B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |
| ISO1452B | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> | <a href="#">单击此处</a> |

### 14.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 14.4 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 14.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 15 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ISO1410BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1410B                | <a href="#">Samples</a> |
| ISO1410BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1410B                | <a href="#">Samples</a> |
| ISO1410DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1410                 | <a href="#">Samples</a> |
| ISO1410DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1410                 | <a href="#">Samples</a> |
| ISO1412BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1412B                | <a href="#">Samples</a> |
| ISO1412BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1412B                | <a href="#">Samples</a> |
| ISO1412DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1412                 | <a href="#">Samples</a> |
| ISO1412DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1412                 | <a href="#">Samples</a> |
| ISO1430BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1430B                | <a href="#">Samples</a> |
| ISO1430BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1430B                | <a href="#">Samples</a> |
| ISO1430DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1430                 | <a href="#">Samples</a> |
| ISO1430DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1430                 | <a href="#">Samples</a> |
| ISO1432BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1432B                | <a href="#">Samples</a> |
| ISO1432BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1432B                | <a href="#">Samples</a> |
| ISO1432DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1432                 | <a href="#">Samples</a> |
| ISO1432DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1432                 | <a href="#">Samples</a> |
| ISO1450BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1450B                | <a href="#">Samples</a> |
| ISO1450BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1450B                | <a href="#">Samples</a> |
| ISO1450DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1450                 | <a href="#">Samples</a> |
| ISO1450DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1450                 | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ISO1452BDW       | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1452B                | <a href="#">Samples</a> |
| ISO1452BDWR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1452B                | <a href="#">Samples</a> |
| ISO1452DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1452                 | <a href="#">Samples</a> |
| ISO1452DWR       | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | ISO1452                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO1410BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1410DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1412BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1412DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1430BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1430DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1432BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1432DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1450BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1450DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1452BDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO1452DWR  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO1410BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1410DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1412BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1412DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1430BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1430DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1432BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1432DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1450BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1450DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1452BDWR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| ISO1452DWR  | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device     | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| ISO1410BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1410BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1410DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1410DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1412BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1412BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1412DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1412DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1430BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1430BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1430DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1430DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1432BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1432BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1432DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1432DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1450BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1450BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1450DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1450DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1452BDW | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1452BDW | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |
| ISO1452DW  | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| ISO1452DW  | DW           | SOIC         | 16   | 40  | 506.98 | 12.7   | 4826   | 6.6    |

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



# DW0016B

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

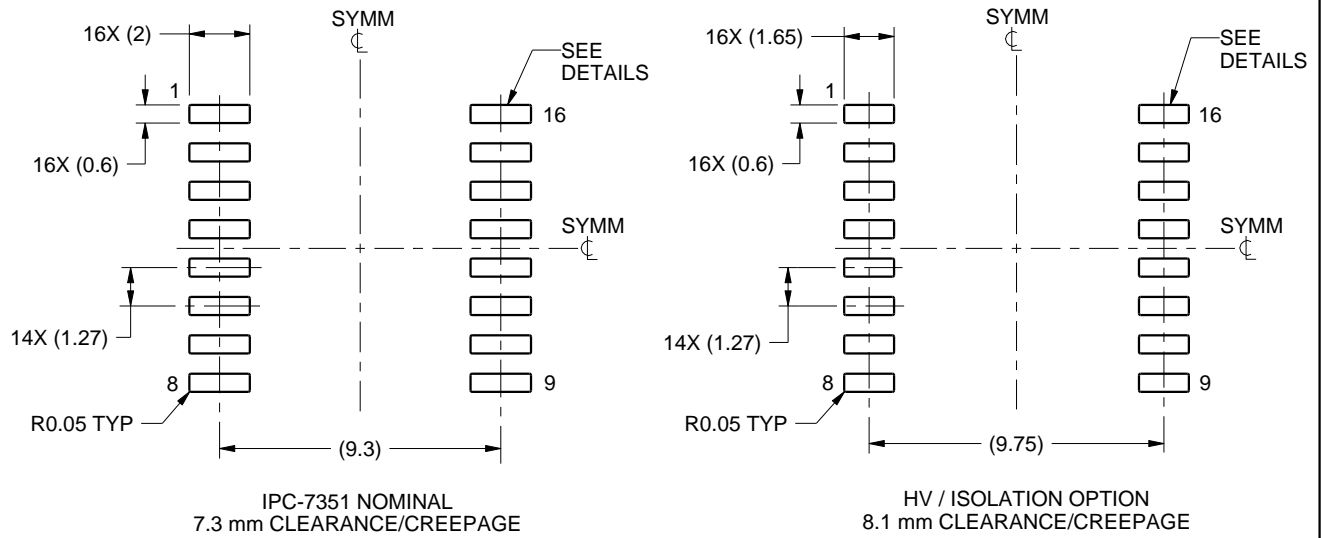
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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