

# INA28x-Q1 汽车级、-14V 至 +80V、双向、高精度、低侧/高侧、电压输出、电流分流监视器

## 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性
  - 器件温度 1 级：-40°C 至 +125°C 环境温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C5
- 功能安全型**
  - 可提供用于功能安全系统设计的文档
- 宽共模范围：-14V 至 +80V
- 失调电压：±20 μV
- CMRR：140dB
- 精度：
  - ±1.4% 增益误差 (最大值)
  - 0.3 μV/°C 温漂
  - 0.005%/°C 增益漂移 (最大值)
- 可用的增益：
  - 50V/V：INA282-Q1
  - 100V/V：INA286-Q1
  - 200V/V：INA283-Q1
  - 500V/V：INA284-Q1
  - 1000V/V：INA285-Q1
- 静态电流：900 μA (最大值)

## 2 应用

- 电动汽车和混合动力汽车电池管理
- EV 和 HEV 充电器
- 电动助力转向 (EPS) 系统
- 车身控制模块
- 刹车系统
- 电子稳定性控制 (ESC) 系统

## 3 说明

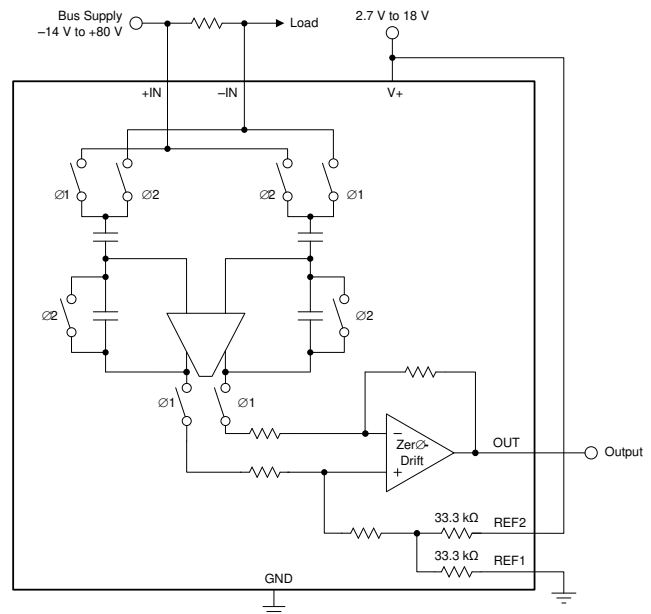
INA28x-Q1 系列包括 INA282-Q1、INA283-Q1、INA284-Q1、INA285-Q1 和 INA286-Q1 器件。这些器件是电压输出分流监控器，能够在 -14V 至 +80V 范围内的共模电压下感测分流器两端的压降，与电源电压无关。零漂移架构的低偏移使得电流检测的分流器两端的最大压降低至 10mV 的满量程。

这些电流检测放大器可由电压为 2.7V 至 18V 的单电源供电，最大电源电流消耗为 900μA。这些器件的额定扩展工作温度范围为 -40°C 至 +125°C，并且采用 SOIC-8 和 VSSOP-8 封装。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
INA28x-Q1	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



详细方框图



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## 4 Revision History

### Changes from Revision B (December 2015) to Revision C (January 2021) Page

• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了“功能安全型”要点.....	1

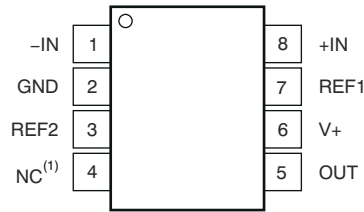
### Changes from Revision A (July 2015) to Revision B (December 2015) Page

• 将 VSSOP 封装从产品预发布更改为量产数据.....	1
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### Changes from Revision \* (March 2012) to Revision A (May 2015) Page

• 将数据表标题从高精度、宽共模范围、双向电流分流监视器零漂移系列更改为 INA28x-Q1 汽车级 -14V 至 80V、双向、高精度、低侧/高侧电压输出电流分流监视器.....	1
• 向数据表添加了 DGK (VSSOP) 封装.....	1
• 更改了应用.....	1
• 更改了首页图.....	1
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.....	3
• Added RVR as symbol for reference rejection ratio.....	5
• Changed order of figures in Typical Characteristics section.....	7
• Changed 图 6-16.....	7
• Changed V <sub>DRIVE</sub> condition in 图 6-20 and 图 6-21.....	7
• Added functional block diagram.....	13
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## 5 Pin Configuration and Functions



A. NC: This pin is not internally connected. The NC pin should either be left floating or connected to GND.

**图 5-1. D and DGK Package 8-Pin SOIC and VSSOP Top View**

**表 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	- IN	Analog input	Connection to negative side of shunt resistor.
2	GND	Analog	Ground
3	REF2	Analog input	Reference voltage, 0 V to V+. See <a href="#">节 7.4.1</a> for connection options.
4	NC	—	This pin is not internally connected. The NC pin should either be left floating or connected to GND.
5	OUT	Analog output	Output voltage
6	V+	Analog	Power supply, 2.7 V to 18 V
7	REF1	Analog input	Reference voltage, 0 V to V+. See <a href="#">节 7.4.1</a> for connection options.
8	+IN	Analog input	Connection to positive side of shunt resistor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, V+			18	V
Analog inputs, V <sub>+IN</sub> , V <sub>-IN</sub> <sup>(2)</sup>	Differential (V <sub>+IN</sub> ) - (V <sub>-IN</sub> ) <sup>(3)</sup>	- 5	5	V
	Common-Mode	- 14	80	V
REF1, REF2, OUT		GND - 0.3	(V+) + 0.3	V
Input current into any pin			5	mA
Junction temperature			150	°C
Storage temperature, T <sub>stg</sub>		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) V<sub>+IN</sub> and V<sub>-IN</sub> are the voltages at the +IN and - IN pins, respectively.
- (3) Input voltages must not exceed common-mode rating.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CM</sub>	Common-mode input voltage		12		V
V+	Operating supply voltage		5		V
T <sub>A</sub>	Operating free-air temperature	- 40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA28x-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	134.9	164.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	72.9	56.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	61.3	85.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.9	6.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	54.3	83.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_{+IN} = 12\text{ V}$ ,  $V_{REF1} = V_{REF2} = 2.048\text{ V}$  referenced to GND, and  $V_{SENSE} = V_{+IN} - V_{-IN}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{OS}$	Offset Voltage, RTI <sup>(1)</sup>	$V_{SENSE} = 0\text{ mV}$		$\pm 20$	$\pm 70$	$\mu\text{ V}$
$dV_{OS}/dT$	vs Temperature	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		$\pm 0.3$	$\pm 1.5$	$\mu\text{ V}/^\circ\text{C}$
PSRR	vs Power Supply	$V_S = 2.7\text{ V}$ to $18\text{ V}$ , $V_{SENSE} = 0\text{ mV}$		3		$\mu\text{ V/V}$
$V_{CM}$	Common-Mode Input Range	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	- 14		+80	V
CMRR	Common-Mode Rejection	$V_{+IN} = -14\text{ V}$ to $80\text{ V}$ , $V_{SENSE} = 0\text{ mV}$ $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	120	140		dB
$I_B$	Input Bias Current per Pin <sup>(2)</sup>	$V_{SENSE} = 0\text{ mV}$		25		$\mu\text{ A}$
$I_{OS}$	Input Offset Current	$V_{SENSE} = 0\text{ mV}$		1		$\mu\text{ A}$
	Differential Input Impedance			6		$\text{k}\Omega$
<b>REFERENCE INPUTS</b>						
	Reference Input Gain			1		V/V
	Reference Input Voltage Range <sup>(3)</sup>		0		$V_{GND} + 9$	V
	Divider Accuracy <sup>(4)</sup>			$\pm 0.2\%$	$\pm 0.5\%$	
RVRR	Reference Voltage Rejection Ratio ( $V_{REF1} = V_{REF2} = 40\text{ mV}$ to $9\text{ V}$ , $V_+ = 18\text{ V}$ )	INA282-Q1		$\pm 25$	$\pm 75$	$\mu\text{ V/V}$
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	0.055		$\mu\text{ V/V}/^\circ\text{C}$
		INA283-Q1		$\pm 13$	$\pm 30$	$\mu\text{ V/V}$
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	0.040		$\mu\text{ V/V}/^\circ\text{C}$
		INA284-Q1		$\pm 6$	$\pm 25$	$\mu\text{ V/V}$
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	0.015		$\mu\text{ V/V}/^\circ\text{C}$
INA285-Q1	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	$\pm 4$	$\pm 10$	$\mu\text{ V/V}$		
INA286-Q1	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	$\pm 17$	$\pm 45$	$\mu\text{ V/V}$		
				0.010		$\mu\text{ V/V}/^\circ\text{C}$
				0.040		$\mu\text{ V/V}/^\circ\text{C}$
<b>GAIN <sup>(6)</sup> (<math>GND + 0.5\text{ V} \leq V_{OUT} \leq (V_+) - 0.5\text{ V}</math>; <math>V_{REF1} = V_{REF2} = (V_+) / 2</math> for all devices)</b>						
G	Gain	INA282-Q1, $V_+ = 5\text{ V}$		50		V/V
		INA283-Q1, $V_+ = 5\text{ V}$		200		V/V
		INA284-Q1, $V_+ = 5\text{ V}$		500		V/V
		INA285-Q1, $V_+ = 5\text{ V}$		1000		V/V
		INA286-Q1, $V_+ = 5\text{ V}$		100		V/V
Gain Error		INA282-Q1, INA283-Q1, INA286-Q1		$\pm 0.4\%$	$\pm 1.4\%$	
		INA284-Q1, INA285-Q1		$\pm 0.4\%$	$\pm 1.6\%$	
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		0.0008	0.005	$\%/^\circ\text{C}$

at  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_{+IN} = 12\text{ V}$ ,  $V_{REF1} = V_{REF2} = 2.048\text{ V}$  referenced to GND, and  $V_{SENSE} = V_{+IN} - V_{-IN}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
Nonlinearity Error				±0.01%		
Output Impedance				1.5		Ω
Maximum Capacitive Load		No sustained oscillation		1		nF
<b>VOLTAGE OUTPUT <sup>(5)</sup></b>						
Swing to V+ Power-Supply Rail		$V_+ = 5\text{ V}$ , $R_{LOAD} = 10\text{ k}\Omega$ to GND $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		$(V_+) - 0.17$	$(V_+) - 0.4$	V
Swing to GND		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		GND+0.015	GND+0.04	V
<b>FREQUENCY RESPONSE</b>						
BW	Effective Bandwidth <sup>(7)</sup>	INA282-Q1		10		kHz
		INA283-Q1		10		
		INA284-Q1		4		
		INA285-Q1		2		
		INA286-Q1		10		
<b>NOISE, RTI <sup>(1)</sup></b>						
Voltage Noise Density		1 kHz		110		nV/√Hz
<b>POWER SUPPLY</b>						
$V_S$	Specified Voltage Range	$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	2.7		18	V
$I_Q$	Quiescent Current			600	900	μA
<b>TEMPERATURE RANGE</b>						
Specified Range			-40		125	°C

- (1) RTI = referred-to-input.
- (2) See typical characteristic graph [图 6-7](#).
- (3) The average of the voltage on pins REF1 and REF2 must be between  $V_{GND}$  and the lesser of  $(V_{GND}+9\text{ V})$  and  $V_+$ .
- (4) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in [图 7-5](#).
- (5) See typical characteristic graphs [图 6-16](#) through [图 6-18](#).
- (6) See typical characteristic graph [图 6-12](#).
- (7) See typical characteristic graph [图 6-1](#) and [节 7.3.2](#) in the Applications Information.

## 6.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_{+IN} = 12\text{ V}$ ,  $V_{REF1} = V_{REF2} = 2.048\text{ V}$  referenced to GND, and  $V_{SENSE} = V_{+IN} - V_{-IN}$ , unless otherwise noted.

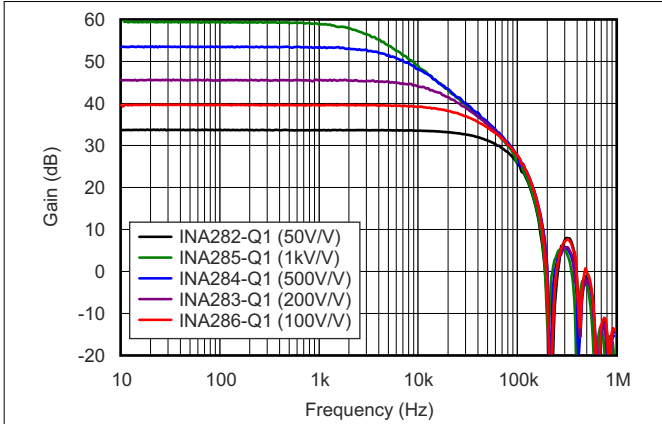


图 6-1. Gain vs Frequency

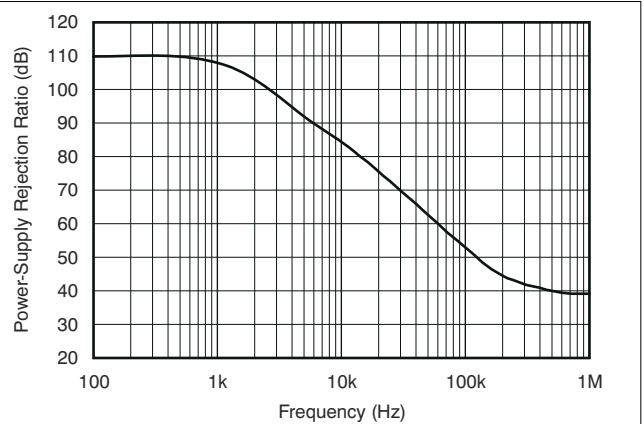


图 6-2. INA282-Q1 PSRR (RTI) vs Frequency

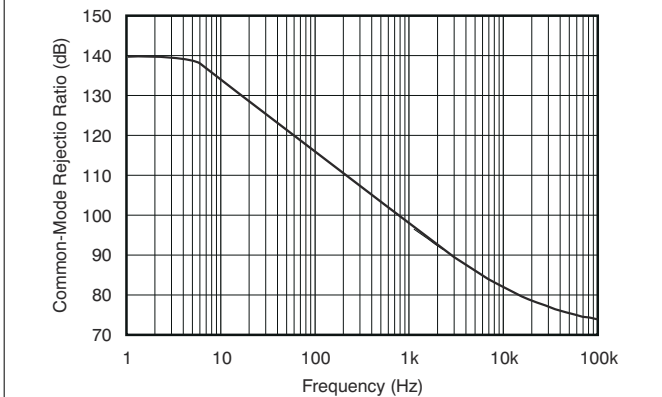


图 6-3. INA284-Q1 Common-Mode Rejection Ratio (RTI)

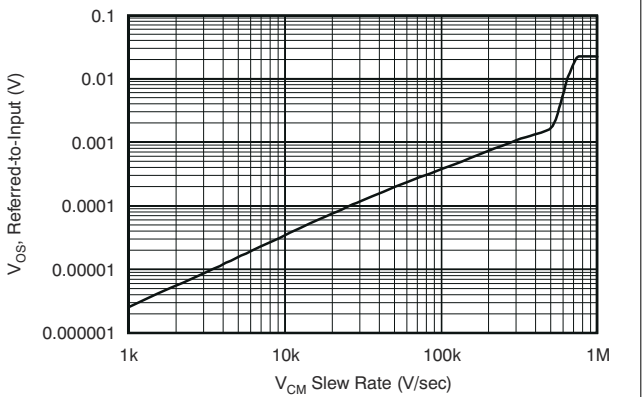


图 6-4. INA282-Q1 Common-Mode Slewing Rate Induced Offset

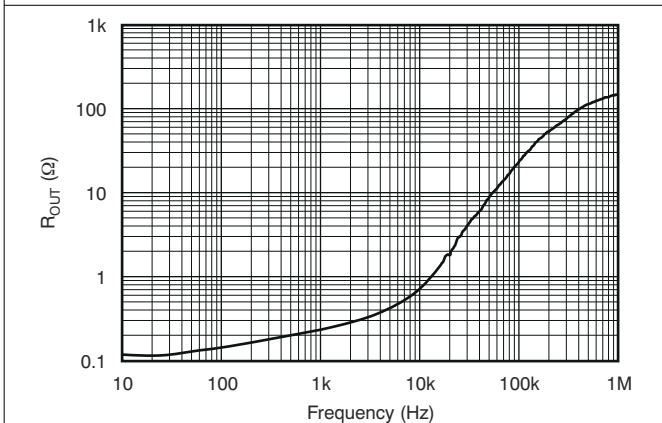


图 6-5. INA286-Q1 Output Impedance vs Frequency

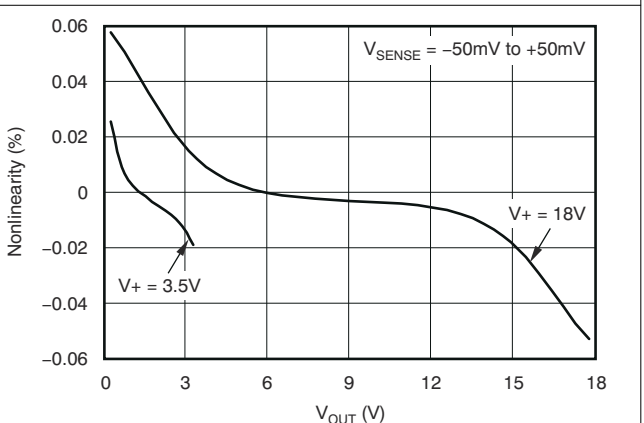
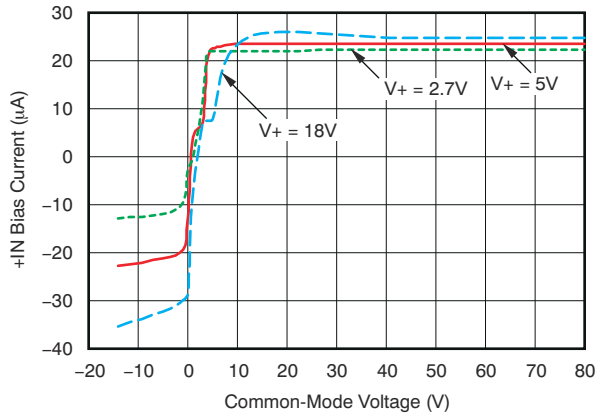
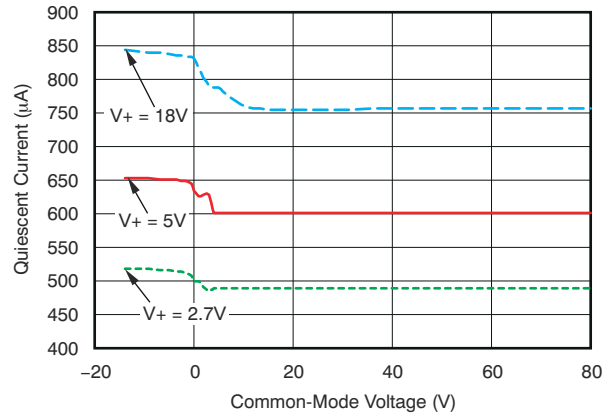


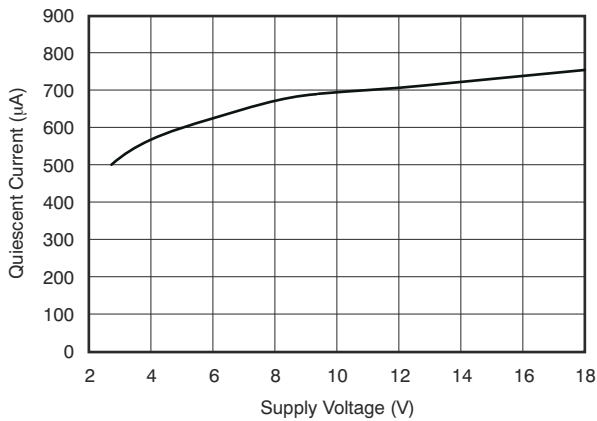
图 6-6. INA282-Q1 Typical Nonlinearity vs Output Voltage



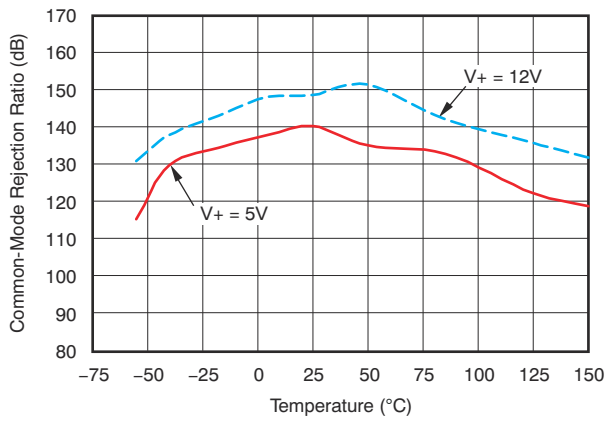
**图 6-7. INA283-Q1 +IN BIAS Current vs Common-Mode Voltage**



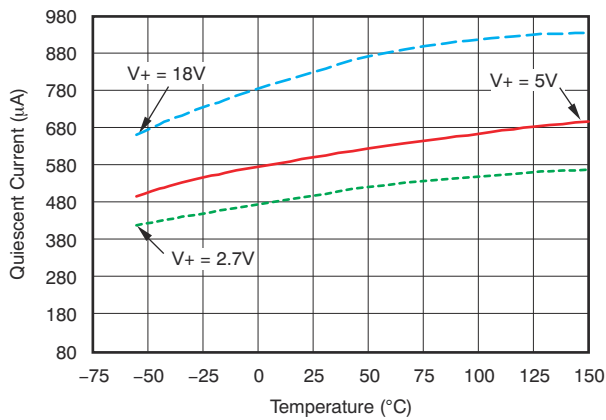
**图 6-8. INA283-Q1 Quiescent Current vs Common-Mode Voltage**



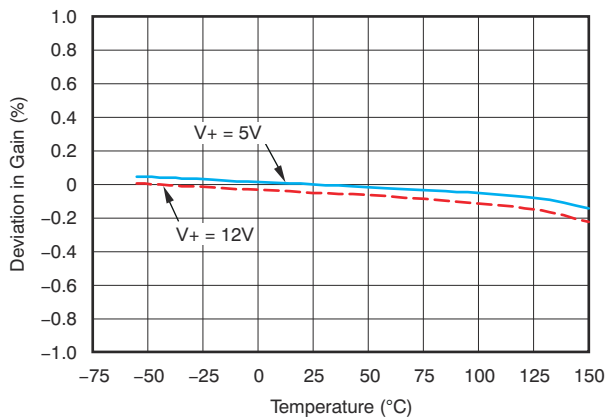
**图 6-9. Quiescent Current vs Supply Voltage**



**图 6-10. Common-Mode Rejection Ratio vs Temperature**

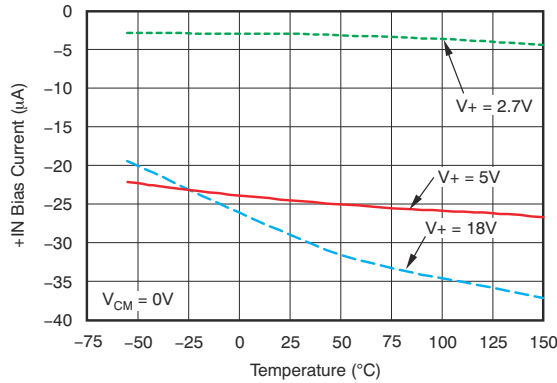


**图 6-11. Quiescent Current vs Temperature**

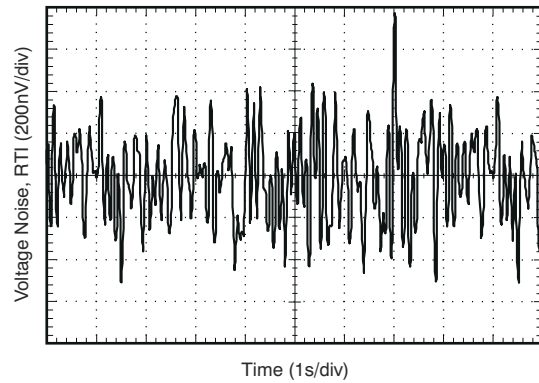


**图 6-12. Deviation in Gain vs Temperature**

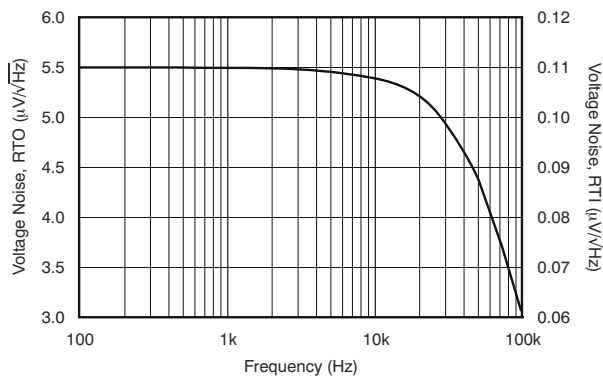




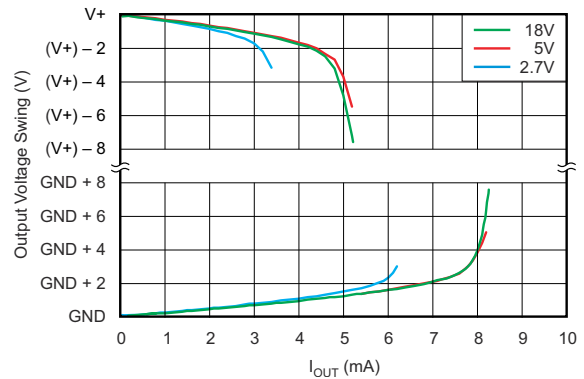
**图 6-13. +IN BIAS Current vs Temperature**



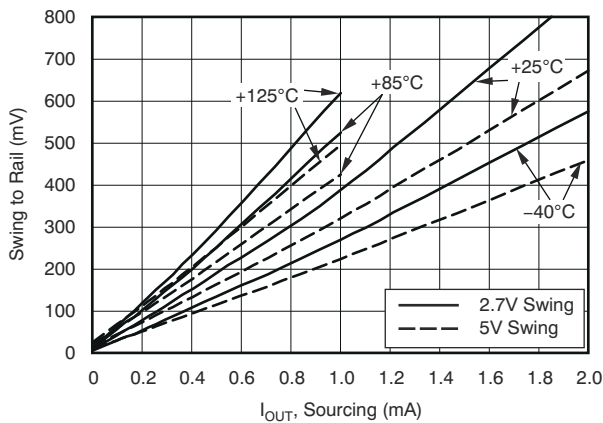
**图 6-14. INA282-Q1 0.1-Hz to 10-Hz Voltage Noise, RTI**



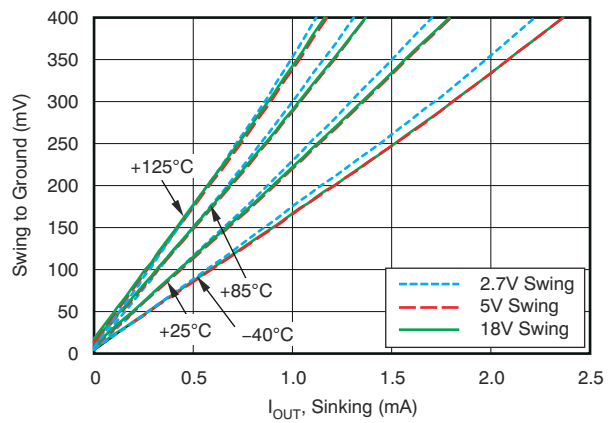
**图 6-15. INA282-Q1 Voltage Noise vs Frequency**



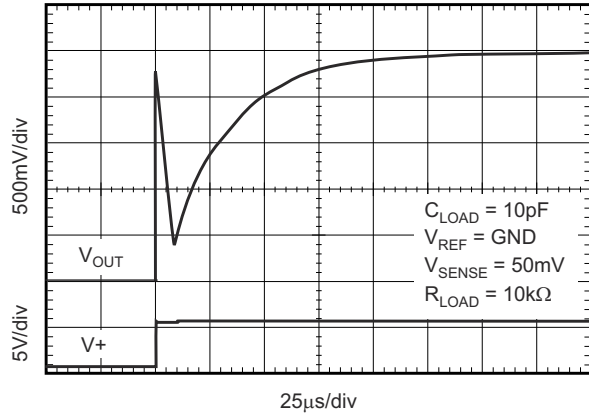
**图 6-16. INA284-Q1 Output Voltage Swing vs Output Current**



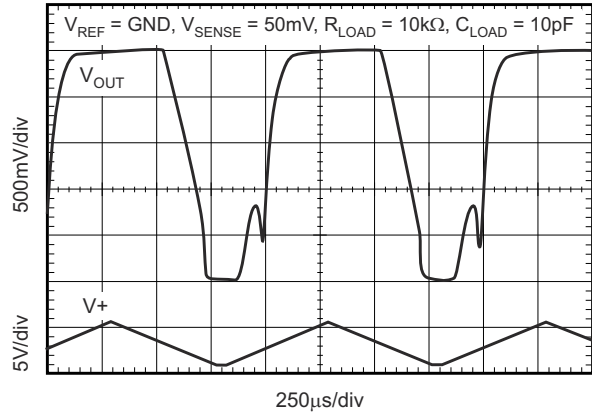
**图 6-17. INA283-Q1 Swing to Rail vs Output Current**



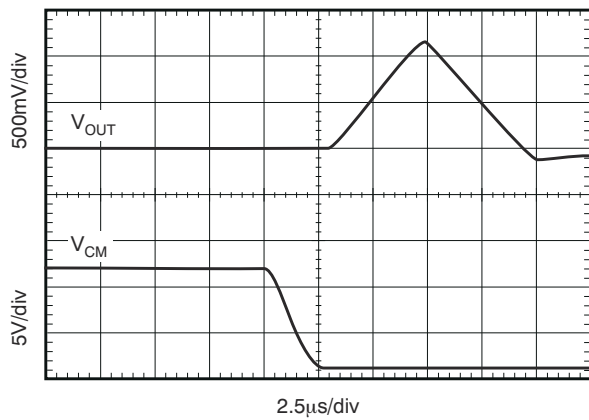
**图 6-18. INA283-Q1 Swing to Ground vs Output Current**



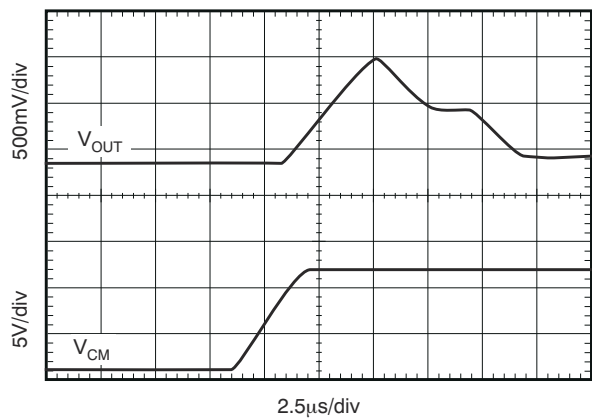
**图 6-19. Start-Up Transient Response**



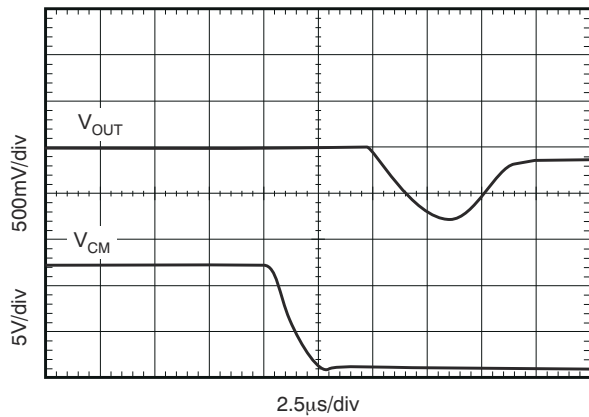
**图 6-20. Start-Up Transient Response**



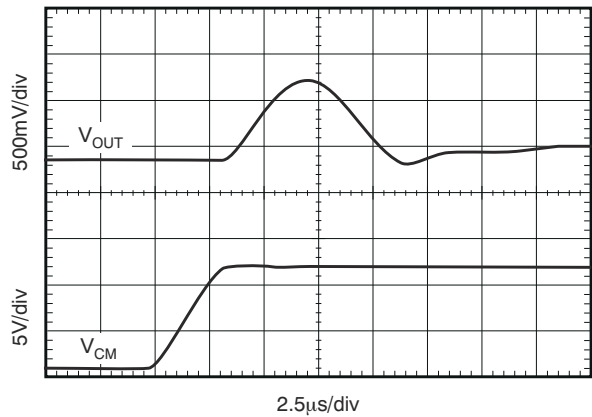
**图 6-21. 12-V Common-Mode Step Response**



**图 6-22. 12-V Common-Mode Step Response**



**图 6-23. 12-V Common-Mode Step Response**



**图 6-24. 12-V Common-Mode Step Response**

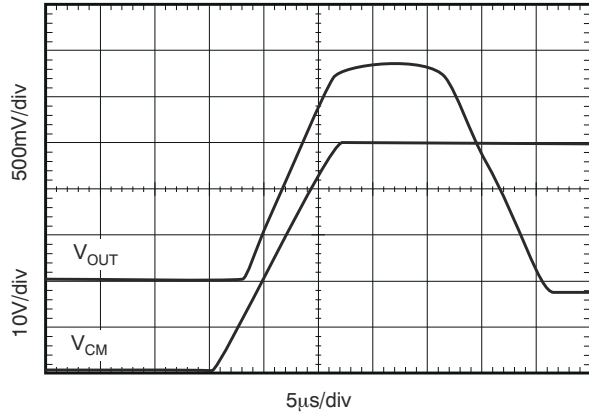


图 6-25. 50-V Common-Mode Step Response

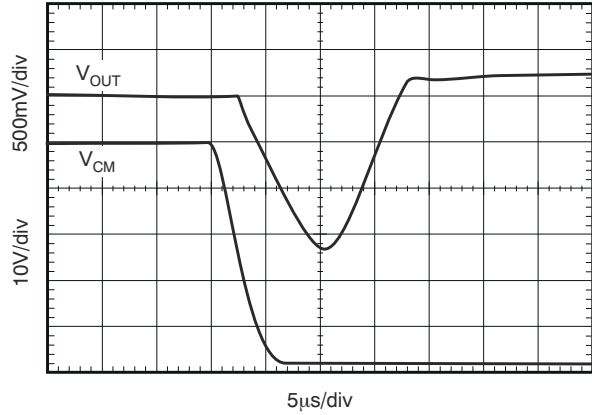


图 6-26. 50-V Common-Mode Step Response

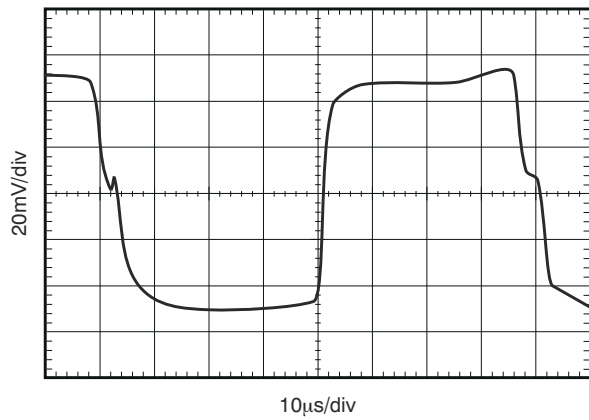


图 6-27. 100-mV Step Response

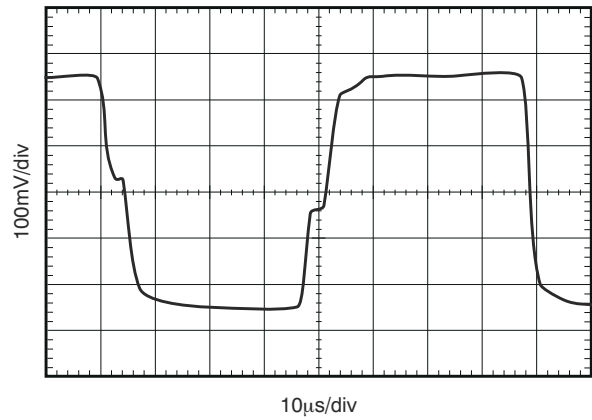


图 6-28. 500-mV Step Response

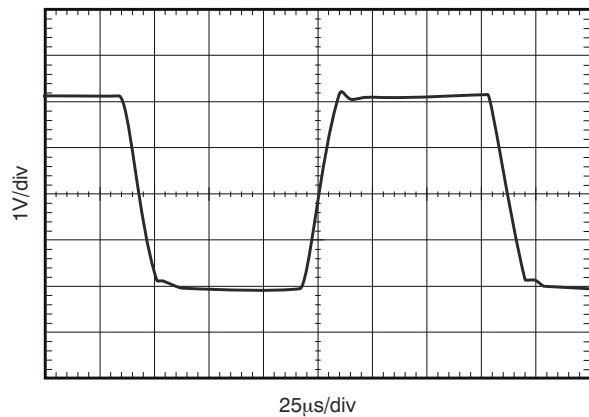


图 6-29. 4-V Step Response

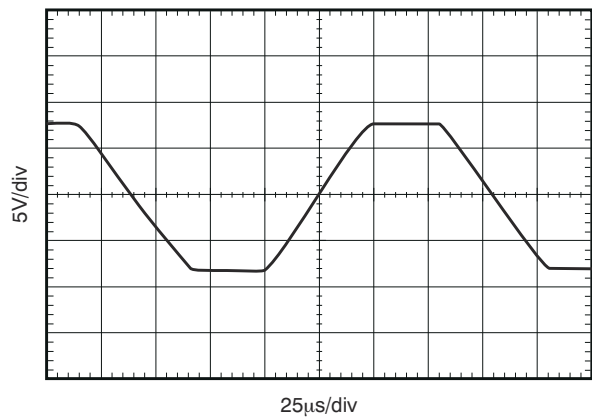


图 6-30. 17-V Step Response

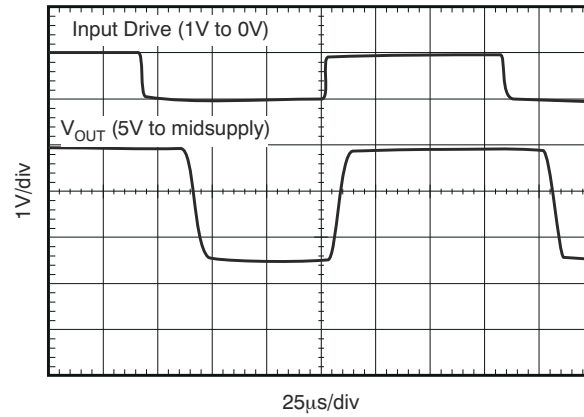


图 6-31. Input Overload

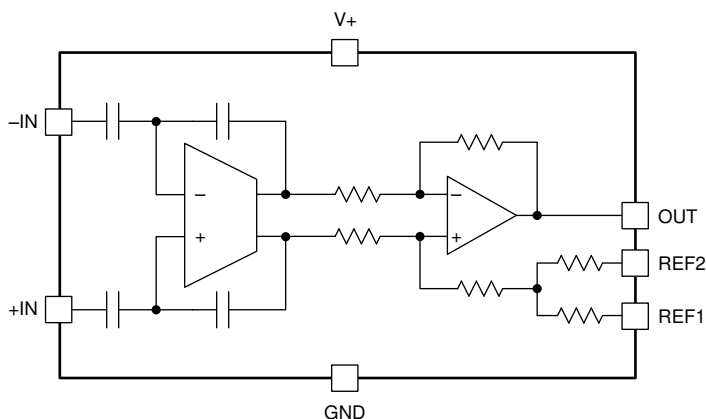
## 7 Detailed Description

### 7.1 Overview

The INA28x-Q1 family of voltage output current-sensing amplifiers are specifically designed to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the devices. This family features a common-mode range that extends 14 V less than the negative supply rail, as well as up to 80 V, allowing for either low-side or high-side current sensing while the device is powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 70  $\mu\text{V}$  with a maximum temperature contribution of 1.5  $\mu\text{V}/^\circ\text{C}$  over the full temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Selecting $R_S$

The zero-drift offset performance of the INA28x-Q1 family offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, nonzero-drift, current-shunt monitors typically require a full-scale range of 100 mV. The INA28x-Q1 family gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude, with many additional benefits. Alternatively, applications that must measure current over a wide dynamic range can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gains of the INA282-Q1, INA286-Q1, or INA283-Q1 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA282-Q1 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 55 mV, with only 70  $\mu$ V of offset.

### 7.3.2 Effective Bandwidth

The extremely high DC CMRR of the INA28x-Q1 results from the switched capacitor input structure. Because of this architecture, the INA28x-Q1 exhibits discrete time system behaviors as illustrated in the gain versus frequency graph of [Figure 6-3](#) and the step response curves of [Figure 6-21](#) through [Figure 6-28](#). The response to a step input depends somewhat on the phase of the internal INA28x-Q1 clock when the input step occurs. It is possible to overload the input amplifier with a rapid change in input common-mode voltage (see [Figure 6-4](#)). Errors as a result of common-mode voltage steps and/or overload situations typically disappear within 15  $\mu$ s after the disturbance is removed.

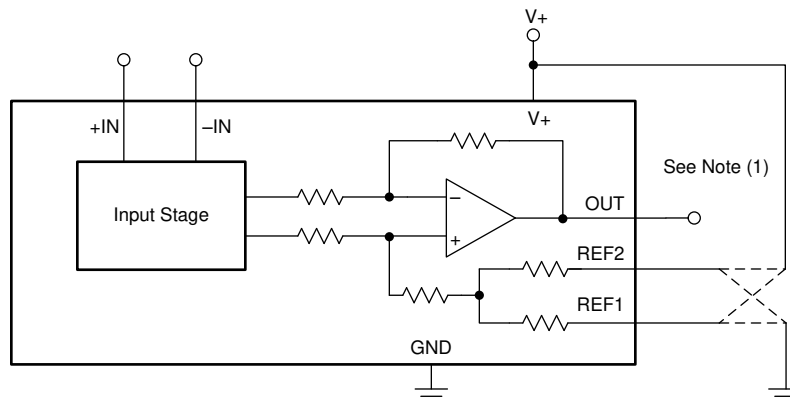
### 7.3.3 Transient Protection

The -14-V to 80-V common-mode range of the INA28x-Q1 is ideal for withstanding automotive fault conditions that range from 12-V battery reversal up to 80-V transients; no additional protective components are needed up to those levels. In the event that the INA28x-Q1 is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (Zener or *Transzorbs*) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it cannot allow the INA28x-Q1 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage as a result of transient absorber dynamic impedance). Despite the use of internal zener-type electrostatic discharge (ESD) protection, the INA28x-Q1 does not lend itself to using external resistors in series with the inputs without degrading gain accuracy.

## 7.4 Device Functional Modes

### 7.4.1 Reference Pin Connection Options

图 7-1 illustrates a test circuit for reference divider accuracy. The output of the INA28x-Q1 can be connected for unidirectional or bidirectional operation. Neither the REF1 pin nor the REF2 pin may be connected to any voltage source lower than GND or higher than V+, and that the effective reference voltage  $(REF1 + REF2)/2$  must be 9 V or less. This parameter means that the V+ reference output connection shown in 图 7-3 is not allowed for V+ greater than 9 V. However, the split-supply reference connection shown in 图 7-5 is allowed for all values of V+ up to 18 V.



- A. Reference divider accuracy is determined by measuring the output with the reference voltage applied to alternate reference resistors, and calculating a result such that the amplifier offset is cancelled in the final measurement.

图 7-1. Test Circuit for Reference Divider Accuracy

#### 7.4.1.1 Unidirectional Operation

Unidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in one direction. In the case of unidirectional operation, the output could be set at the negative rail (near ground, and the most common connection) or at the positive rail (near V+) when the differential input is 0V. The output moves to the opposite rail when a correct polarity differential input voltage is applied.

The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to move the output down. If the output is set at ground, the polarity is positive to move the output up.

The following sections describe how to configure the output for unidirectional operation.

##### 7.4.1.1.1 Ground Referenced Output

When using the INA28x-Q1 in this mode, both reference inputs are connected to ground; this configuration takes the output to the negative rail when there is 0V differential at the input (as 图 7-2 shows).

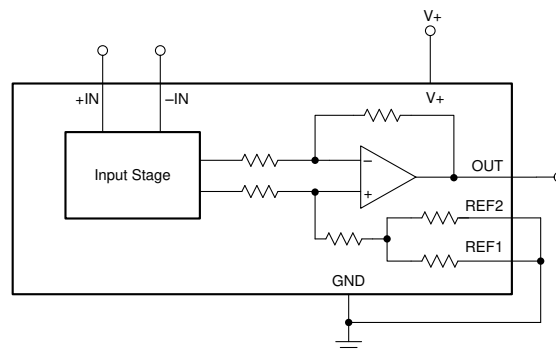


图 7-2. Ground Referenced Output

### 7.4.1.1.2 V+ Referenced Output

This mode is set when both reference pins are connected to the positive supply. It is typically used when a diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (as shown in 图 7-3).

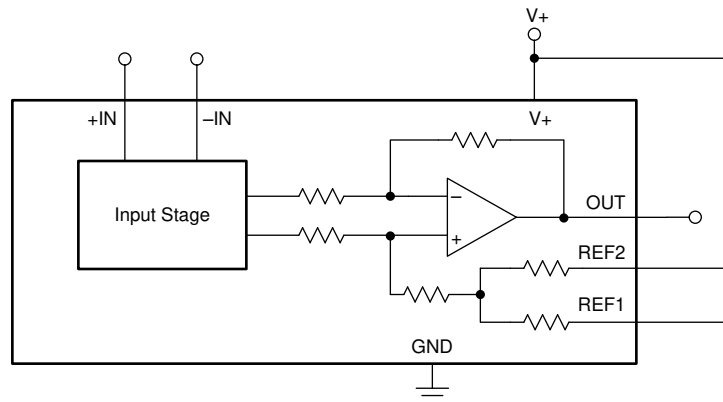


图 7-3. V+ Referenced Output

### 7.4.1.2 Bidirectional Operation

Bidirectional operation allows the INA28x-Q1 to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, from 0 V to 9 V, but never to exceed the supply voltage). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage(s) to the reference inputs. REF1 and REF2 are connected to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

#### 7.4.1.2.1 External Reference Output

Connecting both pins together and to a reference produces an output at the reference voltage when there is no differential input; this configuration is illustrated in 图 7-4. The output moves down from the reference voltage when the input is negative relative to the - IN pin and up when the input is positive relative to the - IN pin. This technique is the most accurate way to bias the output to a precise voltage.

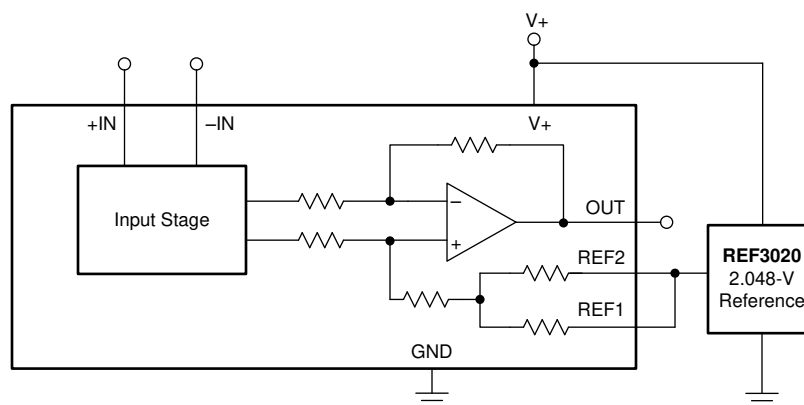


图 7-4. External Reference Output



#### 7.4.1.2.2 Splitting the Supply

By connecting one reference pin to V+ and the other to the ground pin, the output is set at half of the supply when there is no differential input, as shown in 图 7-5. This method creates a midscale offset that is ratiometric to the supply voltage; thus, if the supply increases or decreases, the output remains at half the supply.

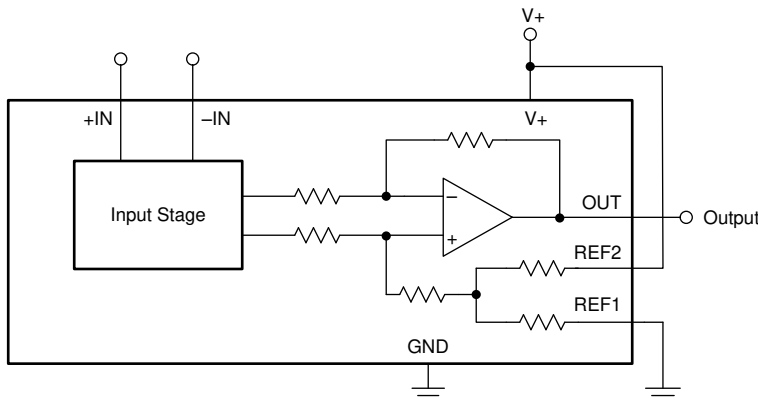


图 7-5. Split-Supply Output

#### 7.4.1.2.3 Splitting an External Reference

In this case, an external reference is divided by 2 with an accuracy of approximately 0.5% by connecting one REF pin to ground and the other REF pin to the reference (as 图 7-6 illustrates).

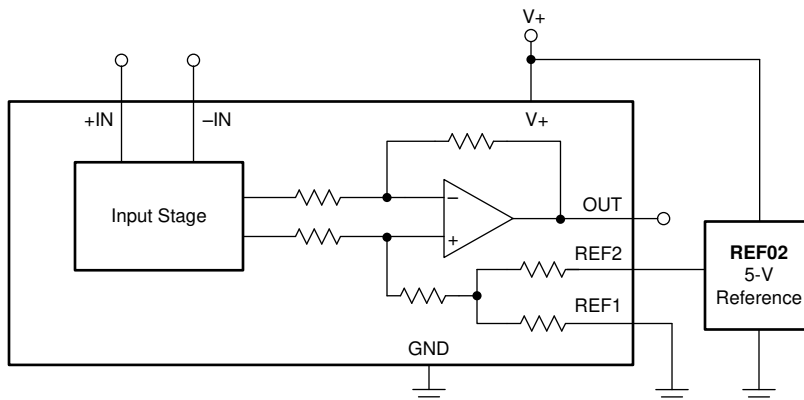


图 7-6. Split Reference Output

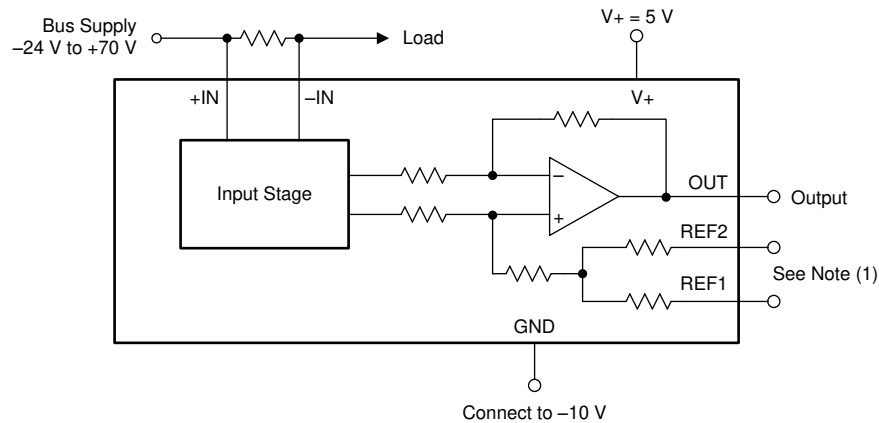
### 7.4.2 Shutdown

While the INA28x-Q1 family does not provide a shutdown pin, the quiescent current of 600  $\mu$ A enables the device to be powered from the output of a logic gate. Take the gate low to shut down the INA28x-Q1 family devices.

### 7.4.3 Extended Negative Common-Mode Range

Using a negative power supply can extend the common-mode range 14 V more negative than the supply used. For instance, a -10 V supply allows up to -24-V negative common-mode. Remember to keep the total voltage between the GND pin and V+ pin to less than 18 V. The positive common-mode decreases by the same amount.

The reference input simplifies this type of operation because the output quiescent bias point is always based on the reference connections. 图 7-7 shows a circuit configuration for common-mode ranges from -24 V to 70 V.



A. Connect the REF pins as desired; however, they cannot exceed 9 V greater than the GND pin voltage.

图 7-7. Circuit Configuration for Common-Mode Ranges from -24 V to 70 V

#### 7.4.4 Calculating Total Error

The electrical specifications for the INA28x-Q1 family of devices include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in 节 6.5. To accurately calculate the expected error of the device, the operating conditions of the device must first be known. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them to calculate the total error value for the device under any normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode rejection ratio, gain error, and nonlinearity error. For the INA28x-Q1, an additional error source referred to as *reference voltage rejection ratio* is also included in the total error value.

The nonlinearity error of the INA28x-Q1 is relatively low compared to the gain error specification. This low error results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA28x-Q1 decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal resulting in an increase in error in the measurement. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The relatively low input offset voltages present in the INA28x-Q1 devices limit the amount of contribution the offset voltage has on the total error term.

The term *reference voltage rejection ratio* refers to the amount of error induced by applying a reference voltage to the INA28x-Q1 device that deviates from the inherent bias voltage present at the output of the first stage of the device. The output of the switched-capacitor network and first-stage amplifier has an inherent bias voltage of approximately 2.048 V. Applying a reference voltage of 2.048 V to the INA28x-Q1 reference pins results in no additional error term contribution. Applying a voltage to the reference pins that differs from 2.048 V creates a voltage potential in the internal difference amplifier, resulting in additional current flowing through the resistor network. As a result of resistor tolerances, this additional current flow causes additional error at the output because of resistor mismatches. Additionally, as a result of resistor tolerances, this additional current flow causes additional error at the output based on the common-mode rejection ratio of the output stage amplifier. This error term is referred back to the input of the device as additional input offset voltage. Increasing the difference between the 2.048-V internal bias and the external reference voltage results in a higher input offset voltage. Also, as the error at the output is referred back to the input, there is a larger impact on the input-referred offset,  $V_{OS}$ , for the lower-gain versions of the device.

Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well, to provide the user more information on how much error variance is present from device to device.

#### 7.4.4.1 Example 1 INA282-Q1

表 7-1.  $V_+ = 5\text{ V}$ ;  $V_{CM} = 12\text{ V}$ ;  $V_{REF1} = V_{REF2} = 2.048\text{ V}$ ;  $V_{SENSE} = 10\text{ mV}$

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	$V_{OS}$	—	20 $\mu\text{V}$	70 $\mu\text{V}$
Added input offset voltage because of common-mode voltage	$V_{OS\_CM}$	$\frac{1}{10^{\left(\frac{CMRR_{dB}}{20}\right)}} \times (V_{CM} - 12\text{V})$	0 $\mu\text{V}$	0 $\mu\text{V}$
Added input offset voltage because of reference voltage	$V_{OS\_REF}$	$RVRR \times (2.048\text{ V} - V_{REF})$	0 $\mu\text{V}$	0 $\mu\text{V}$
Total input offset voltage	$V_{OS\_Total}$	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	20 $\mu\text{V}$	70 $\mu\text{V}$
Error from input offset voltage	Error_ $V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.20%	0.70%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
<b>Total error</b>	—	$\sqrt{(\text{Error\_}V_{OS})^2 + (\text{Error\_Gain})^2 + (\text{Error\_Lin})^2}$	0.45%	1.56%

#### 7.4.4.2 Example 2 INA286-Q1

表 7-2.  $V_+ = 5\text{ V}$ ;  $V_{CM} = 24\text{ V}$ ;  $V_{REF1} = V_{REF2} = 0\text{ V}$ ;  $V_{SENSE} = 10\text{ mV}$

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial input offset voltage	$V_{OS}$	—	20 $\mu\text{V}$	70 $\mu\text{V}$
Added input offset voltage because of common-mode voltage	$V_{OS\_CM}$	$\frac{1}{10^{\left(\frac{CMRR_{dB}}{20}\right)}} \times (V_{CM} - 12\text{V})$	1.2 $\mu\text{V}$	12 $\mu\text{V}$
Added input offset voltage because of reference voltage	$V_{OS\_REF}$	$RVRR \times (2.048\text{ V} - V_{REF})$	34.8 $\mu\text{V}$	92.2 $\mu\text{V}$
Total input offset voltage	$V_{OS\_Total}$	$\sqrt{(V_{OS})^2 + (V_{OS\_CM})^2 + (V_{OS\_REF})^2}$	40.2 $\mu\text{V}$	116.4 $\mu\text{V}$
Error from input offset voltage	Error_ $V_{OS}$	$\frac{V_{OS\_Total}}{V_{SENSE}} \times 100$	0.40%	1.16%
Gain error	Error_Gain	—	0.40%	1.40%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
<b>Total error</b>	—	$\sqrt{(\text{Error\_}V_{OS})^2 + (\text{Error\_Gain})^2 + (\text{Error\_Lin})^2}$	0.57%	1.82%

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The INA28x-Q1 family of devices measure the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pins to adjust the functionality of the output signal is shown in multiple configurations.

#### 8.1.1 Basic Connections

图 8-1 shows the basic connection of an INA28x-Q1 family device. Connect the input pins, +IN and -IN, as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

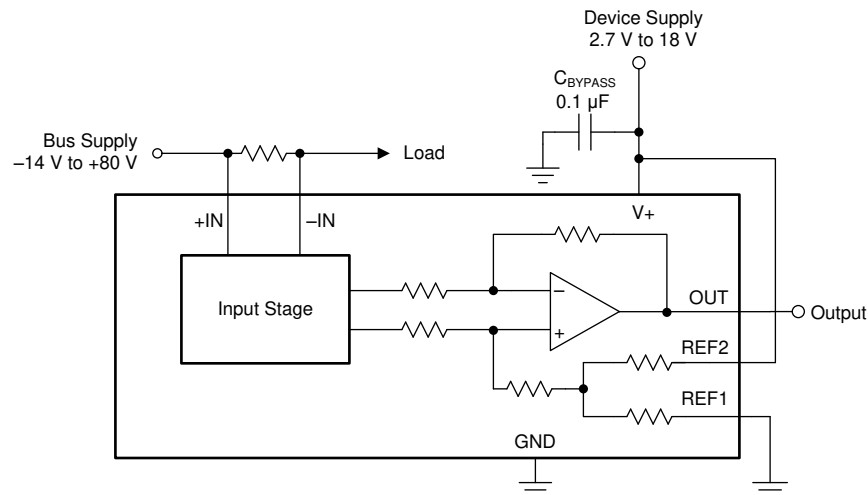


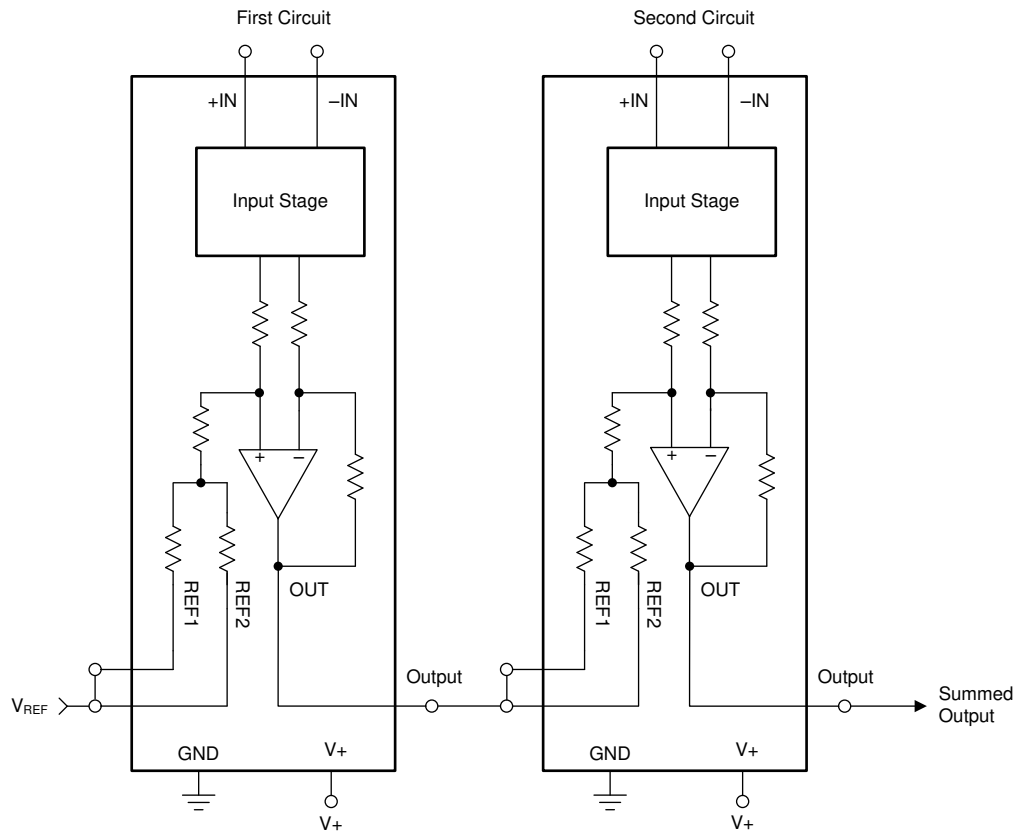
图 8-1. Basic Connections

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

## 8.2 Typical Applications

### 8.2.1 Current Summing

The outputs of multiple INA28x-Q1 family devices are easily summed by connecting the output of one INA28x-Q1 family device to the reference input of a second INA28x-Q1 family device. The circuit configuration shown in [Figure 8-1](#) is an easy way to achieve current summing.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

**图 8-2. Summing the Outputs of Multiple INA28x-Q1 Family Devices**

### 8.2.1.1 Design Requirements

In order to sum multiple load currents, multiple INA28x-Q1 devices must be connected. 图 8-2 shows summing for two devices. Summing beyond two devices is possible by repeating this connection. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

### 8.2.1.2 Detailed Design Procedures

Connect the output of one INA28x-Q1 family device to the reference input of the next INA28x-Q1 family device in the chain. Use the reference input of the first circuit to set the reference of the final summed output. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

### 8.2.1.3 Application Curve

图 8-3 shows an example output response of a summing configuration. The reference pins of the first circuit are connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.

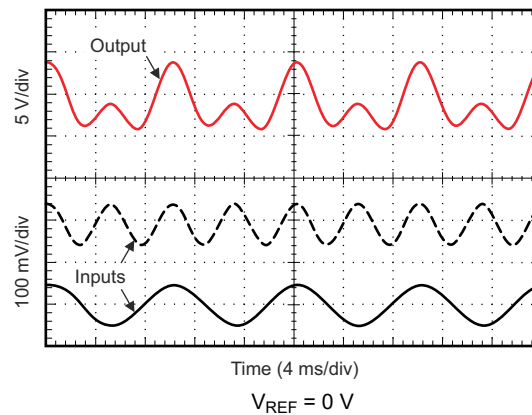
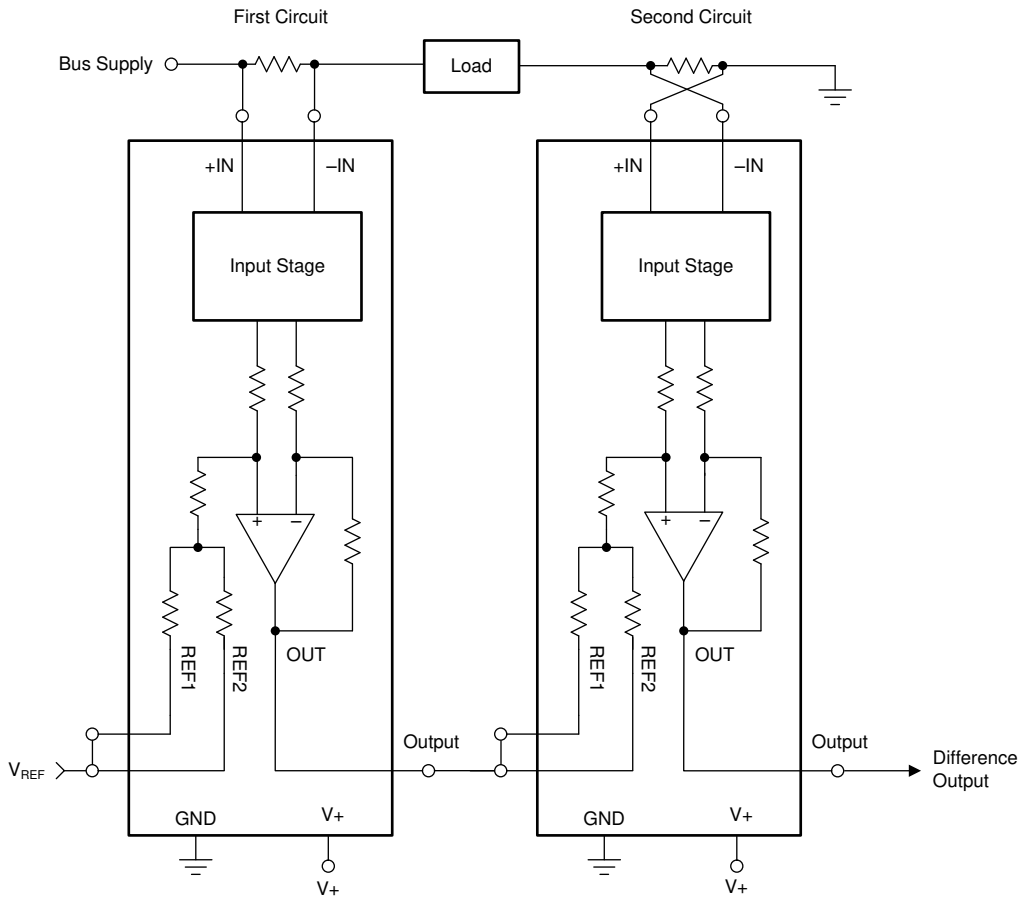


图 8-3. Current Summing Application Output Response

### 8.2.2 Current Differencing

Occasionally, the need arises to confirm that the current into a load is identical to the current out of a load, usually as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing except that the two amplifiers have the inputs connected opposite of each other.



NOTE: The voltage applied to the reference inputs must not exceed 9 V.

**图 8-4. Current Differencing Using an INA28x-Q1 Device**

### 8.2.2.1 Design Requirements

For current differencing, connect two INA28x-Q1 devices, and connect the inputs opposite to each other, as shown in 图 8-4. The reference input of the first INA28x-Q1 family device sets the output quiescent level for all the devices in the string.

### 8.2.2.2 Detailed Design Procedure

Connect the output of one INA28x-Q1 family device to the reference input of the second INA28x-Q1 family device. The reference input of the first circuit sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current into and out of a load do not match.

### 8.2.2.3 Application Curve

图 8-5 shows an example output response of a difference configuration. The reference pins of the first circuit are connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out of phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.

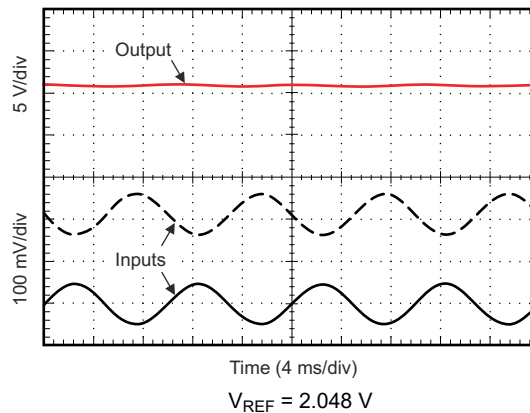


图 8-5. Current Differencing Application Output Response



## 9 Power Supply Recommendations

The INA28x-Q1 can make accurate measurements well outside of its own power-supply voltage,  $V+$ , because its inputs (+IN and -IN) may operate anywhere from -14 V to 80 V independent of  $V+$ . For example, the  $V+$  power supply can be 5 V while the common-mode voltage being monitored by the shunt may be as high as 80 V. Of course, the output voltage range of the INA28x-Q1 is constrained by the supply voltage that powers it on  $V+$ . When the power to the INA28x-Q1 is off (that is, no voltage is supplied to the  $V+$  pin), the input pins (+IN and -IN) are high impedance with respect to ground and typically leak less than  $\pm 1 \mu\text{A}$  over the full common-mode range of -14 V to 80 V.

## 10 Layout

### 10.1 Layout Guidelines

Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. TI recommends a bypass capacitor with a value of 0.1  $\mu\text{F}$ . Add additional decoupling capacitance to compensate for noisy or high-impedance power supplies.

### 10.2 Layout Example

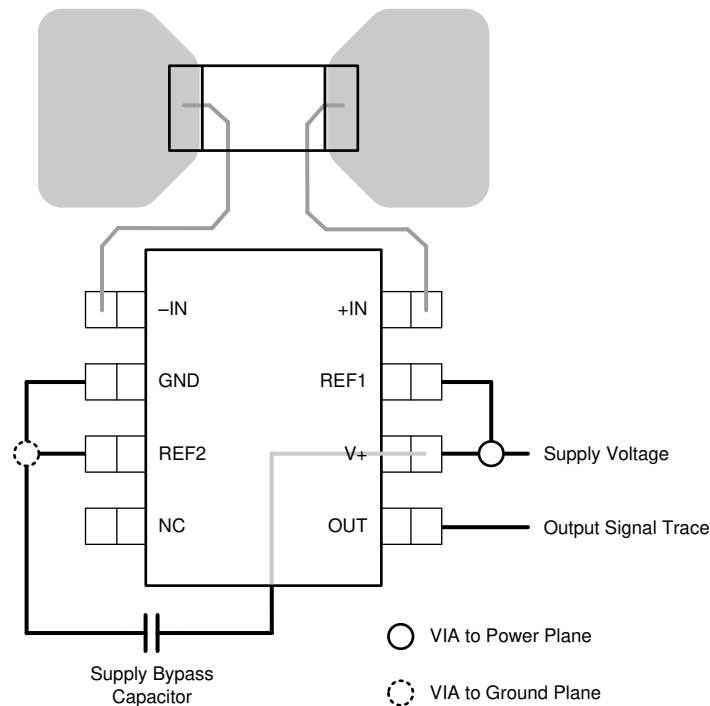


图 10-1. Layout Example

## 11 Device and Documentation Support

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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### 11.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">INA282AQDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11GF
<a href="#">INA282AQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	282Q1
<a href="#">INA283AQDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11FF
<a href="#">INA283AQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	283Q1
<a href="#">INA284AQDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11HF
<a href="#">INA284AQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	284Q1
<a href="#">INA285AQDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11IF
<a href="#">INA285AQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	285Q1
<a href="#">INA286AQDGKRQ1</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	11JF
<a href="#">INA286AQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	286Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA282-Q1, INA283-Q1, INA284-Q1, INA285-Q1, INA286-Q1 :**

- Catalog : [INA282](#), [INA283](#), [INA284](#), [INA285](#), [INA286](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA282AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA282AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA283AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA283AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA284AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA284AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA285AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA285AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA286AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA286AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA282AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA282AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
INA283AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA283AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
INA284AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA284AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
INA285AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA285AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
INA286AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA286AQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

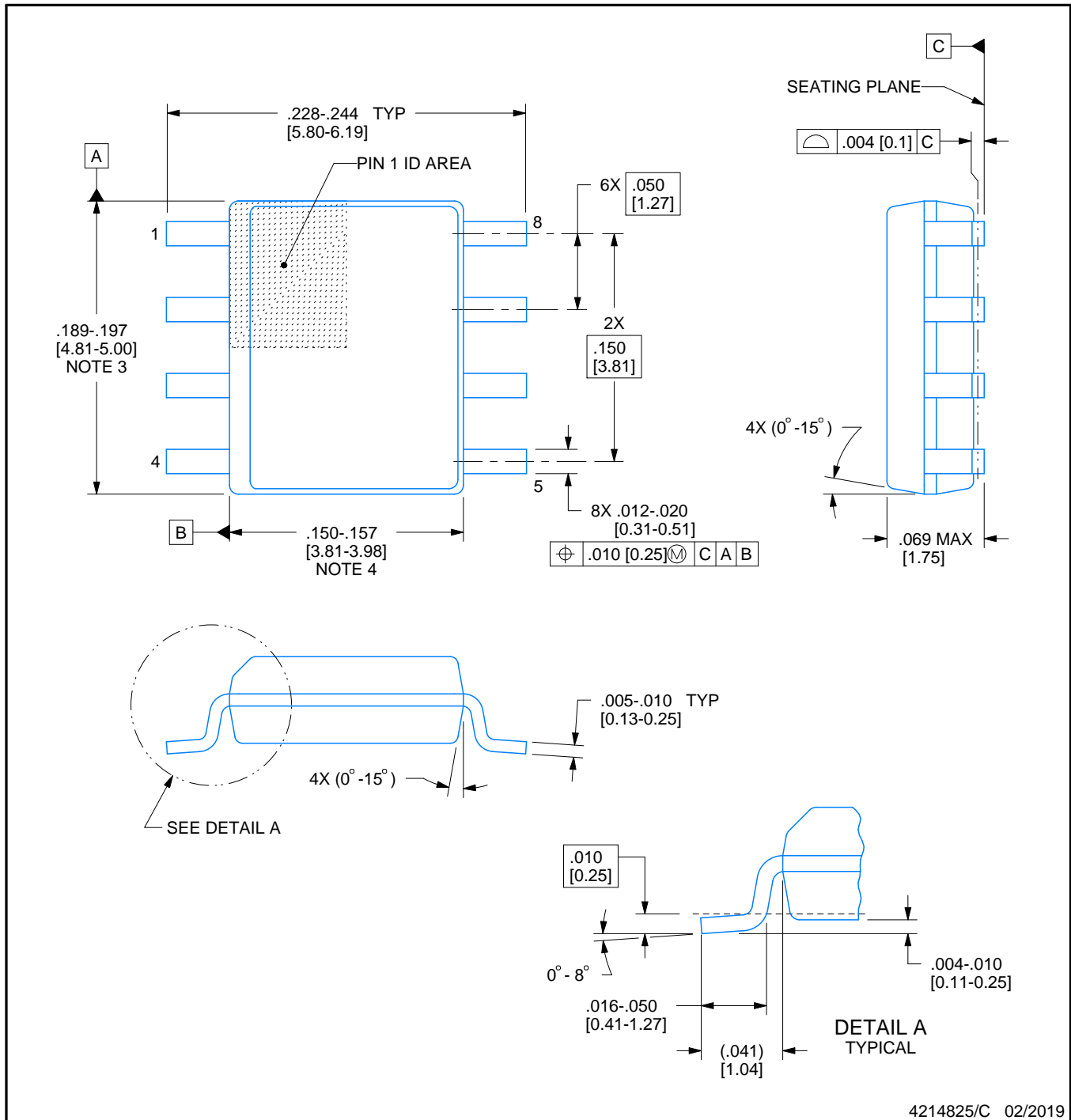


# D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

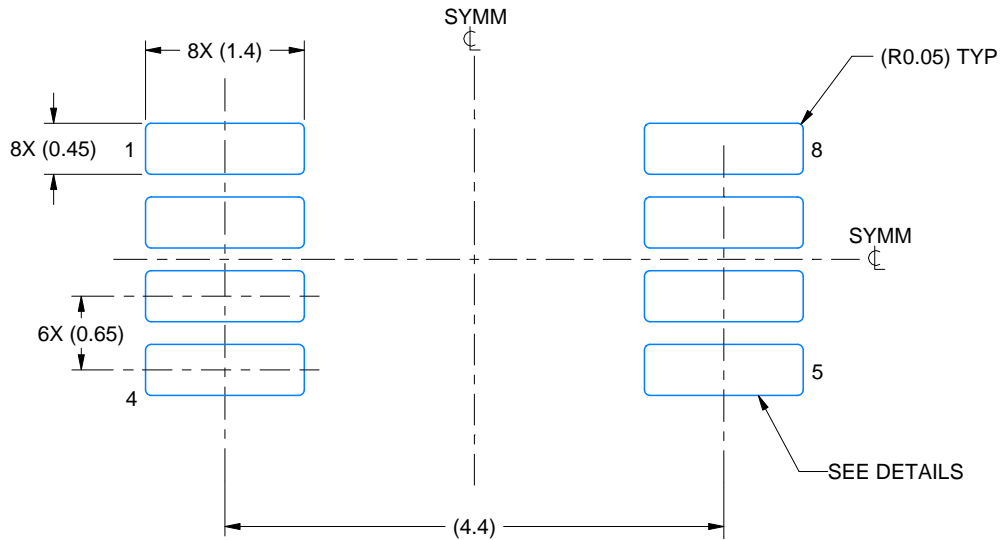
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

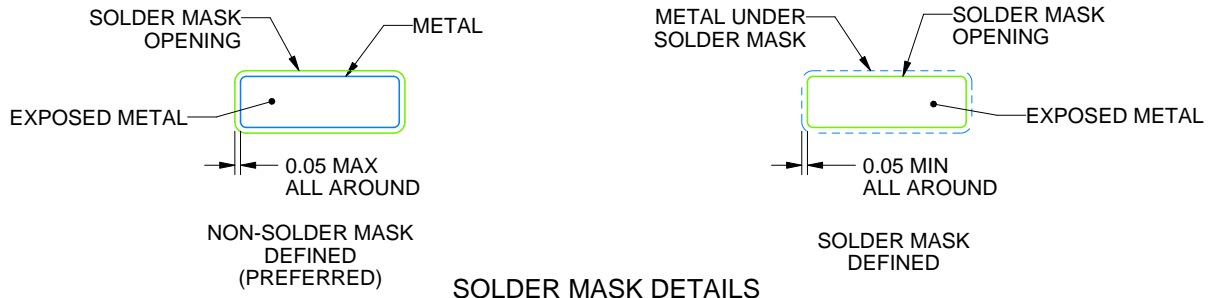
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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