

# ESDS452 采用 SOT-23 封装的 5.5V 双向 TVS 二极管

## 1 特性

- IEC 61000-4-5 浪涌保护：
  - 18A (8/20  $\mu$ s)
- IEC 61000-4-2 ESD 保护：
  - $\pm 30$ kV 接触放电
  - $\pm 30$ kV 气隙放电
- 5.5V 工作电压
- 超低漏电流：
  - 1nA (典型值)
- I/O 电容：
  - 3pF (典型值)
- 双向极性，支持正负电压摆幅
- 双通道器件通过单个元件提供全面的 ESD/浪涌保护
- 小型引线式 SOT-23 可实现低成本的自动光学检测 (AOI)

## 2 应用

- 终端设备：
  - 工厂自动化和控制
  - 楼宇自动化
  - 电网基础设施
  - HVAC 系统
  - 储能系统

## 3 说明

ESDS452 是一款双向 ESD 和 TVS 二极管。ESDS452 的额定 ESD 冲击消散值超出了 IEC 61000-4-2 国际标准所规定的最高水平 ( $\pm 30$ kV 接触放电,  $\pm 30$ kV 气隙放电)。根据 IEC 61000-4-5 标准, 该器件可以钳制峰值脉冲电流高达 18A 的 8/20  $\mu$ s 浪涌。此外, 二极管的正负低钳位电压有助于防止下游电路在 ESD 或浪涌事件期间暴露于高电压和大电流中。这种保护对于对稳健性和可靠性要求很高的工业系统至关重要。

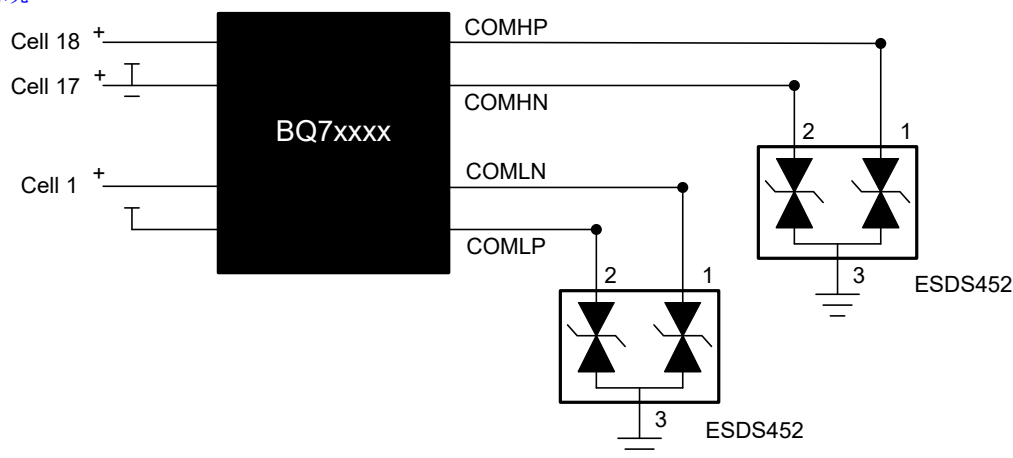
ESDS452 采用小型引线式 SOT-23 (DBZ) 封装。

封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
ESDS452	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) 有关更多信息, 请参阅节 9。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。



BMS 的典型应用

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## 4 Pin Configuration and Functions

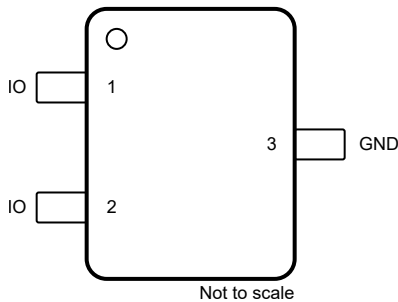


图 4-1. ESDS452 DBZ Package, 3-Pin SOT-23 (Top View)

表 4-1. Pin Functions for ESDS452

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Parameter		MIN	MAX	UNIT
P <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20μs) Peak Pulse Power at 25 °C		172	W
I <sub>PPM</sub>	IEC 61000-4-5 Surge (t <sub>p</sub> = 8/20μs) Peak Pulse Current at 25 °C		18	A
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C
T <sub>stg</sub>	Storage temperature	- 65	155	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings -JEDEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 ESD Ratings - IEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

### 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	- 5.5		5.5	V
T <sub>A</sub>	Operating Free Air Temperature	- 40		125	°C

### 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ESDS452	UNIT
		DBZ (SOT-23)	
		3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	309.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	162.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	149.0	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	41.0	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	147.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

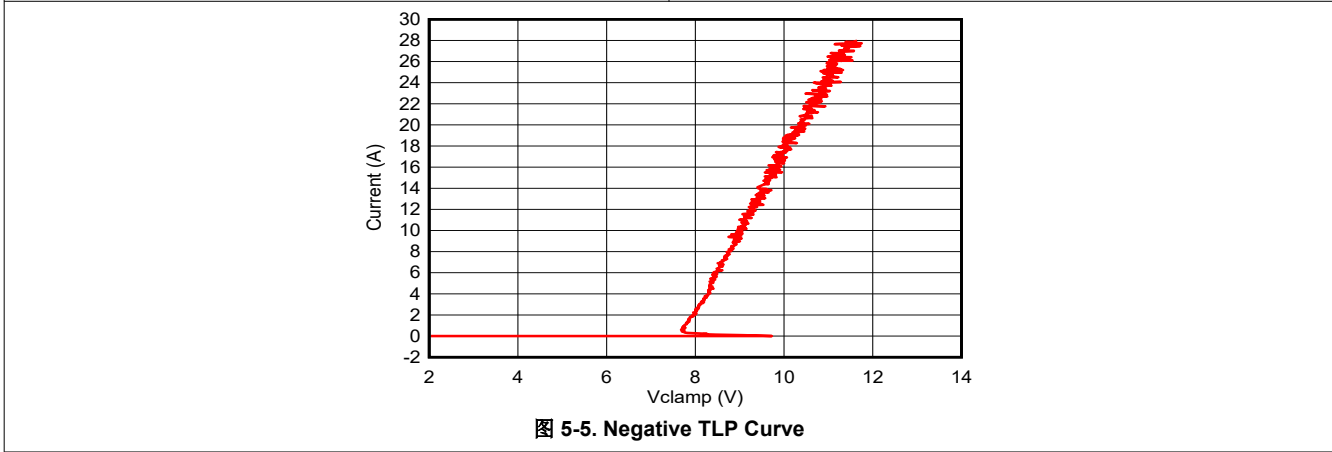
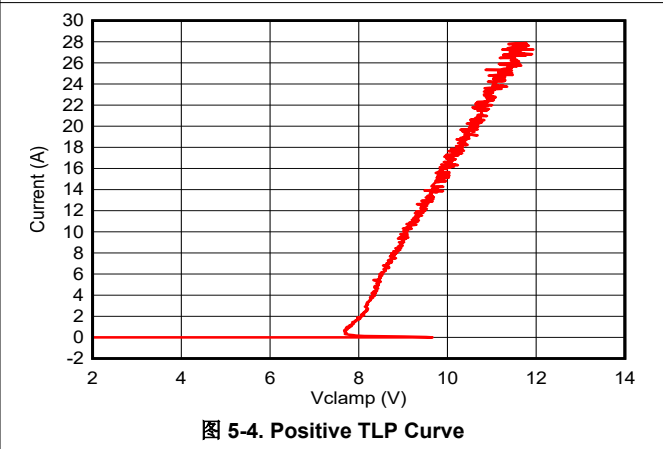
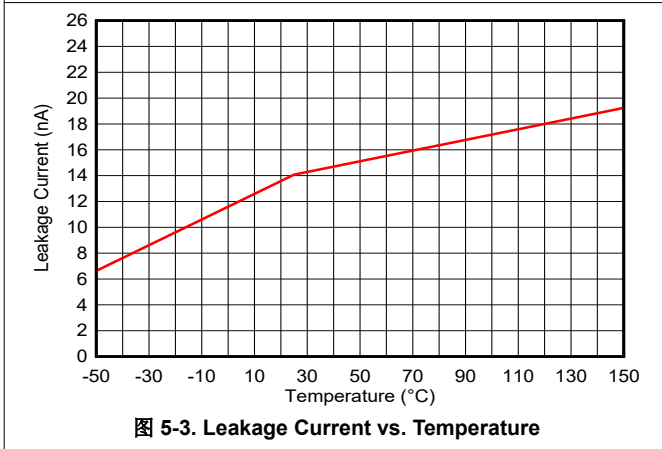
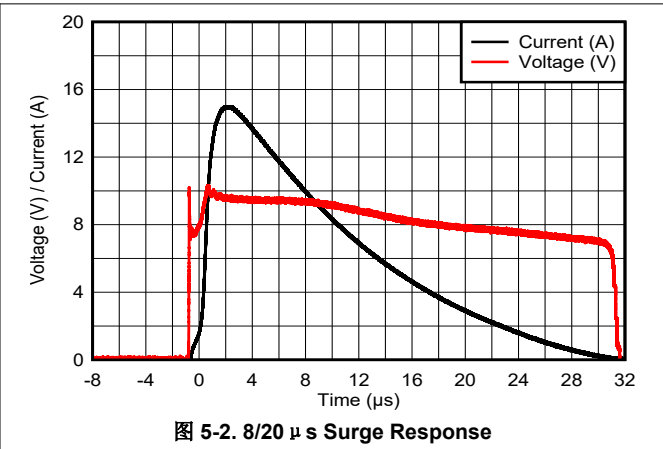
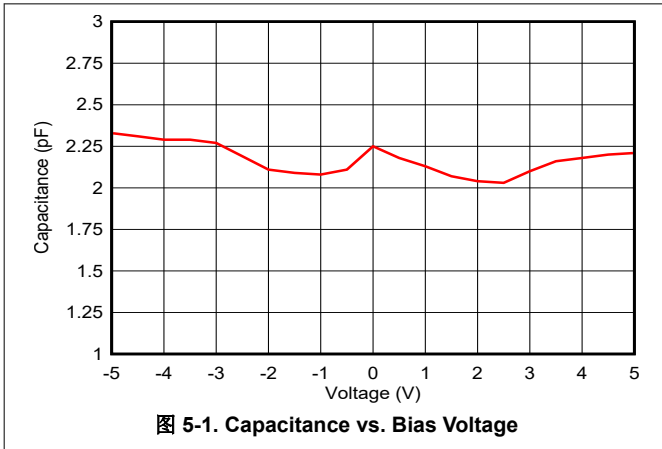
## 5.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>RWM</sub>	Reverse stand-off voltage	I <sub>IO</sub> < 50nA	-5.5		5.5	V
I <sub>LEAK</sub>	Leakage current at V <sub>RWM</sub>	V <sub>IO</sub> = ±5.5 V, I/O to GND and GND to I/O		1	50	nA
V <sub>BR</sub>	Breakdown voltage, I/O to GND <sup>(1)</sup>	I <sub>IO</sub> = ±1mA	7	8	9	V
V <sub>CLAMP</sub>	Surge clamping voltage, t <sub>p</sub> = 8/20 μs <sup>(2)</sup>	I <sub>PP</sub> = ±1 A, I/O to GND		7.5	10	V
V <sub>CLAMP</sub>	Surge clamping voltage, t <sub>p</sub> = 8/20 μs <sup>(2)</sup>	I <sub>PP</sub> = ±15 A, I/O to GND		11.5	14	V
V <sub>CLAMP</sub>	TLP clamping voltage, t <sub>p</sub> = 100ns <sup>(3)</sup>	I <sub>PP</sub> = ±16 A, I/O to GND		9.6		V
R <sub>DYN</sub>	Dynamic resistance <sup>(4)</sup>	I/O to GND		0.29		Ω
		GND to I/O		0.29		
C <sub>LINE</sub>	Line capacitance, IO to GND	V <sub>IO</sub> = 0 V, f = 1 MHz		3	5	pF

- (1) V<sub>BR</sub> is defined as the voltage when ±1mA is applied in the positive or negative direction respectively.  
(2) Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5  
(3) Non-repetitive square wave current pulse, Transmission Line Pulse (TLP); ANSI / ESD STM5.5.1-2008  
(4) 8/20 μs (IEC 61000-4-5) dynamic resistance

### 5.7 Typical Characteristics



## 6 Application and Implementation

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### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 6.1 Application Information

The ESDS452 is a diode type TVS which provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#).

## 7 Device and Documentation Support

### 7.1 Documentation Support

#### 7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Packaging and Layout Guide](#)
- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

### 7.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 7.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 7.4 Trademarks

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### 7.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 7.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial Release

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESDS452DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	3BO8	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS452DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS452DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

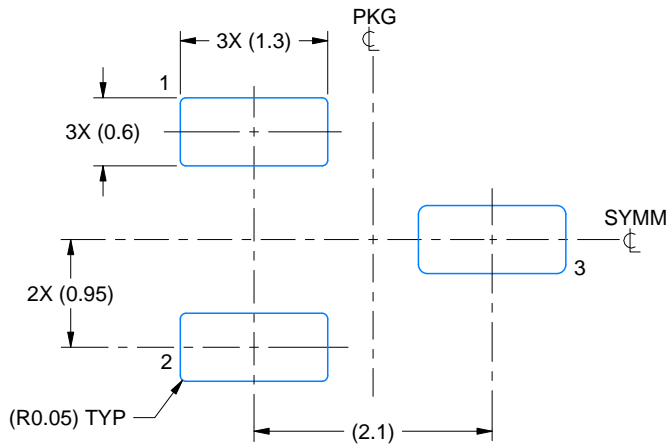


# EXAMPLE BOARD LAYOUT

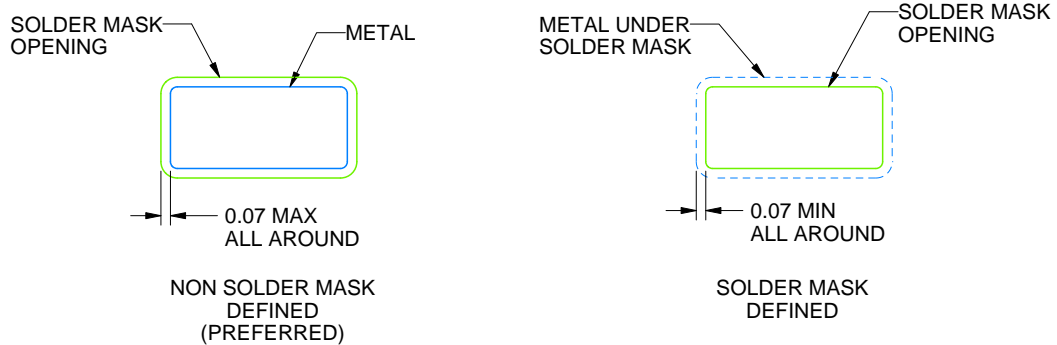
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

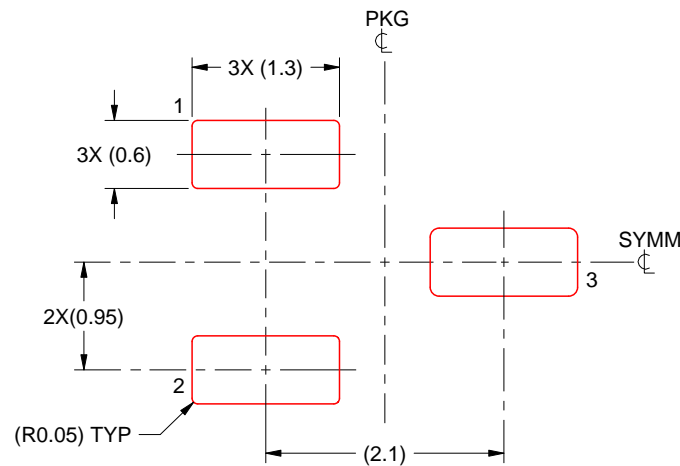
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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