

ESD2CANxx36-Q1 适用于车载网络的 汽车类双通道 36V ESD 保护二极管

1 特性

- 36V 工作电压
- IEC 61000-4-2 ESD 保护：
 - $\pm 25\text{kV}$ 接触放电和 $\pm 25\text{kV}$ 气隙放电 (ESD2CAN36-Q1)
 - $\pm 18\text{kV}$ 接触放电和 $\pm 18\text{kV}$ 气隙放电 (ESD2CANFD36-Q1)
- ISO 10605 (330pF , 330 Ω) ESD 保护：
 - $\pm 25\text{kV}$ 接触放电和 $\pm 25\text{kV}$ 气隙放电 (ESD2CAN36-Q1)
 - $\pm 18\text{kV}$ 接触放电和 $\pm 18\text{kV}$ 气隙放电 (ESD2CANFD36-Q1)
- IEC 61000-4-5 浪涌保护 (8/20 μs) :
 - 4.3A (ESD2CAN36-Q1)
 - 3.1A (ESD2CANFD36-Q1)
- 双向 ESD 保护
- I/O 电容 = 2.8pF 典型值 (ESD2CAN36-Q1)
- I/O 电容 = 2.6pF 典型值 (ESD2CANFD36-Q1)
- 低钳位电压可保护下游元件
- 符合 AEC-Q101 标准
- SOT-23 (DBZ) 小型、标准封装
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- **汽车车载网络：**
 - 控制器局域网 (CAN)
 - 控制器局域网灵活数据速率 (CAN-FD)
 - 低速容错 CAN
 - 高速 CAN
- **工业控制网络：**
 - DeviceNet IEC 62026-3
 - CANopen - CiA 301/302-2 和 EN 50325-4

3 说明

ESD2CANxx36-Q1 是一款提供控制器局域网 (CAN) 接口保护的双向 ESD 保护二极管。ESD2CANxx36-Q1 的额定消散接触 ESD 冲击能力符合 ISO 10605 汽车标准。低动态电阻和低钳位电压支持针对瞬态事件提供系统级保护。这种保护很关键，因为汽车系统对安全应用的稳健性和可靠性要求很高。

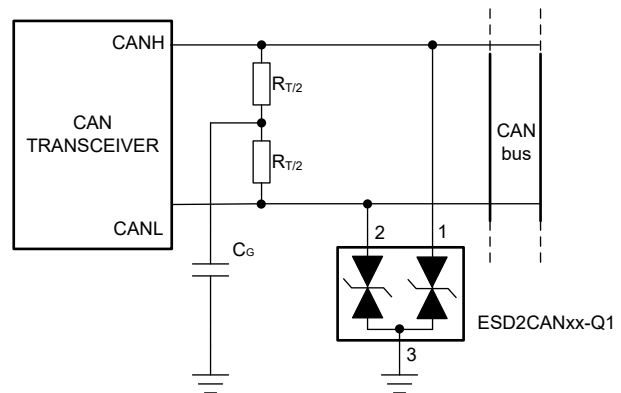
该器件的低 IO 电容 (每通道) 和引脚排列适合两条汽车 CAN 总线 (CANH 和 CANL)，可防止总线因静电放电 (ESD) 和其他瞬态而损坏。此外，ESD2CANxx36-Q1 具有 2.8pF (典型值) 或更低的线路电容，是 CAN、CAN-FD 和 CAN SiC 应用的理想选择。

ESD2CANxx36-Q1 采用 3 引脚 SOT-23 引线式封装，可轻松实现直通式布线。

器件信息

器件型号	通道数	封装 ⁽¹⁾
ESD2CAN36-Q1	2 通道	DBZ (SOT-23 , 3)
ESD2CANFD36-Q1		

(1) 有关详细信息，请参阅节 9



ESD2CANxx36-Q1 典型应用



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4 Pin Configuration and Functions

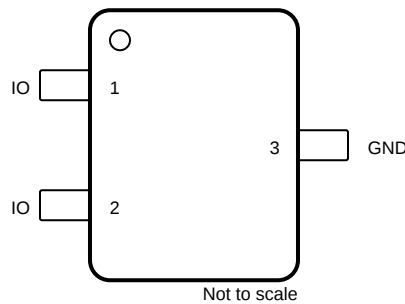


图 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I/O = Input or Output, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		DEVICE	MIN	MAX	UNIT
P _{PP}	IEC 61000-4-5 Power (t _p = 8/20 μs) at 25°C	ESD2CAN36-Q1		233	W
		ESD2CANFD36-Q1		175	
I _{PP}	IEC 61000-4-5 current (t _p = 8/20 μs) at 25°C	ESD2CAN36-Q1		4.3	A
		ESD2CANFD36-Q1		3.1	
T _A	Operating free-air temperature		-55	150	°C
T _J	Junction temperature		-55	150	
T _{stg}	Storage temperature		-65	155	

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

PARAMETER	TEST CONDITION	VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 ⁽¹⁾	± 2500	V
		Charged device model (CDM), per AEC Q101-005 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	DEVICE	VALUE	UNIT
V _(ESD)	IEC 61000-4-2 Contact Discharge, all pins	ESD2CAN36-Q1	±25000	V
		ESD2CANFD36-Q1	±18000	
	IEC 61000-4-2 Air-gap Discharge, all pins	ESD2CAN36-Q1	±25000	
		ESD2CANFD36-Q1	±18000	

5.4 ESD Ratings - ISO Specification

over TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	DEVICE	VALUE	UNIT	
V _(ESD)	Contact discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN36-Q1	±25000	V
			ESD2CANFD36-Q1	±18000	
		ISO 10605, 330pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
			ESD2CANFD36-Q1	±18000	
	Air-gap discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
			ESD2CANFD36-Q1	±18000	
		ISO 10605, 330pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
			ESD2CANFD36-Q1	±18000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-36		36	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC ⁽¹⁾		ESD2CAN36-Q1	ESD2CANFD36-Q1	UNIT
		DBZ (SOT-23)	DBZ (SOT-23)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.4	313.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.9	162.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.0	151.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.9	43.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	132.0	150.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.7 Electrical Characteristics

over $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			-36		36	V
V_{BRF}	Breakdown voltage ⁽²⁾	$I_{IO} = 10\text{mA}$, IO to GND		37.8	40	44.2	V
V_{BRR}		$I_{IO} = -10\text{mA}$, IO to GND		-37.8	-40	-44.2	V
V_{CLAMP}	Clamping voltage ⁽³⁾	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CAN36-Q1		43		V
V_{CLAMP}		$I_{PP} = 4.3\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CAN36-Q1		61		V
V_{CLAMP}		$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CANFD36-Q1		47		V
V_{CLAMP}		$I_{PP} = 3.1\text{A}$, $t_p = 8/20\mu\text{s}$, IO to GND	ESD2CANFD36-Q1		61		V
V_{CLAMP}	Clamping voltage ⁽⁴⁾	$I_{PP} = 16\text{A}$, TLP, IO to GND or GND to IO	ESD2CAN36-Q1		63		V
V_{CLAMP}			ESD2CANFD36-Q1		64		V
I_{LEAK}	Leakage current	$V_{IO} = \pm 24\text{V}$, IO to GND		-50	5	50	nA
R_{DYN}	Dynamic resistance ⁽⁴⁾	IO to GND and GND to IO	ESD2CAN36-Q1		0.49		Ω
			ESD2CANFD36-Q1		0.49		Ω
C_L	Line capacitance ⁽⁵⁾	$V_{IO} = 0\text{V}$, $f = 1\text{MHz}$, $V_{pp} = 30\text{mV}$	ESD2CAN36-Q1		2.8	3.5	pF
			ESD2CANFD36-Q1		2.6	2.9	

(1) Measurements made on each IO channel

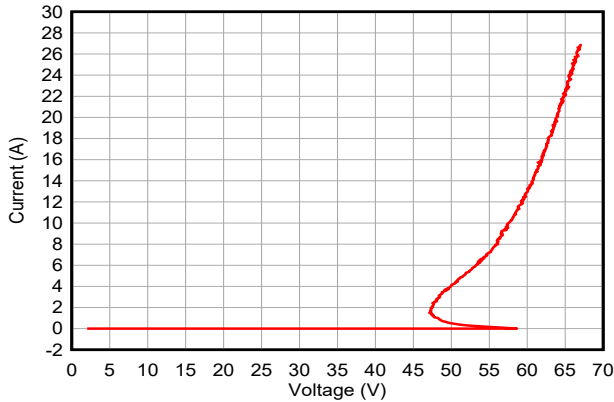
(2) V_{BRF} and V_{BRR} are defined as the voltage when $\pm 10\text{mA}$ is applied in the positive and negative going direction respectively, before the device latches into the snapback state

(3) Device stressed with $8/20\mu\text{s}$ exponential decay waveform according to IEC 61000-4-5

(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

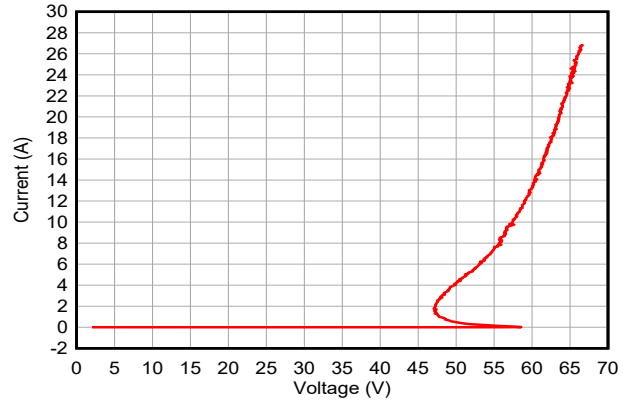
(5) Measured from IO to GND on each channel

5.8 Typical Characteristics - ESD2CAN36-Q1



tp = 100 ns, Transmission Line Pulse (TLP)

图 5-1. Positive TLP Curve



tp = 100 ns, Transmission Line Pulse (TLP)

图 5-2. Negative TLP Curve

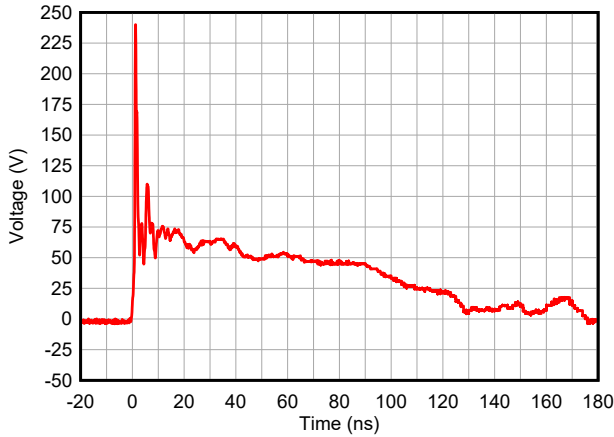


图 5-3. +8kV Clamped IEC Waveform

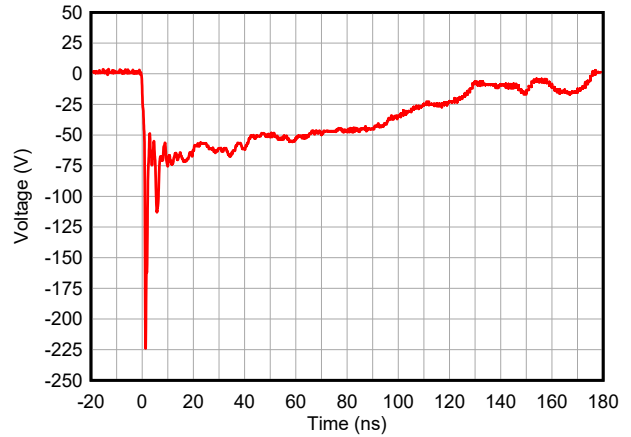


图 5-4. -8kV Clamped IEC Waveform

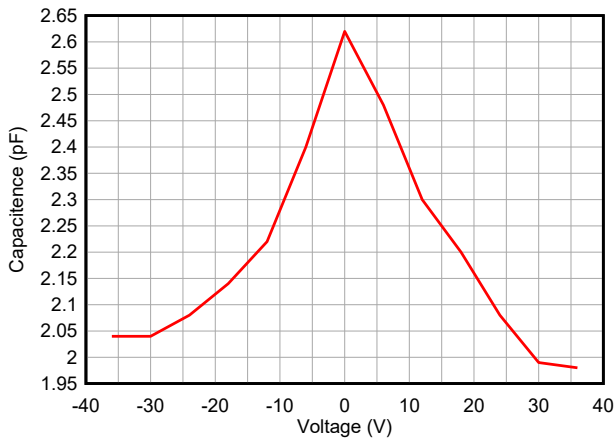


图 5-5. Capacitance vs. Bias Voltage

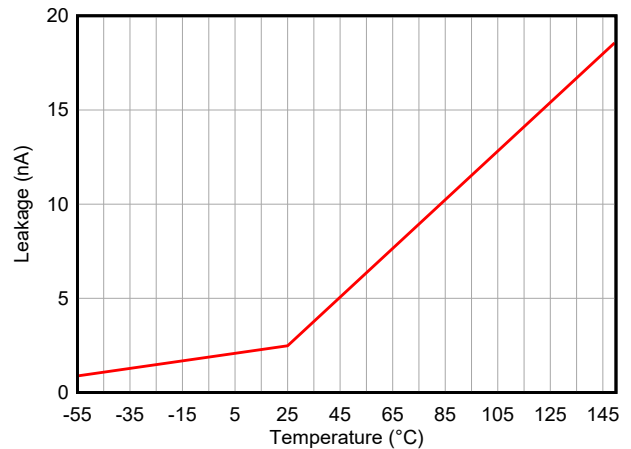
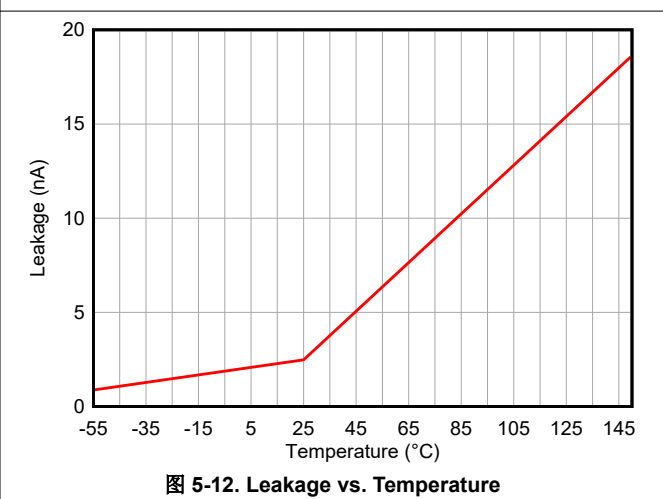
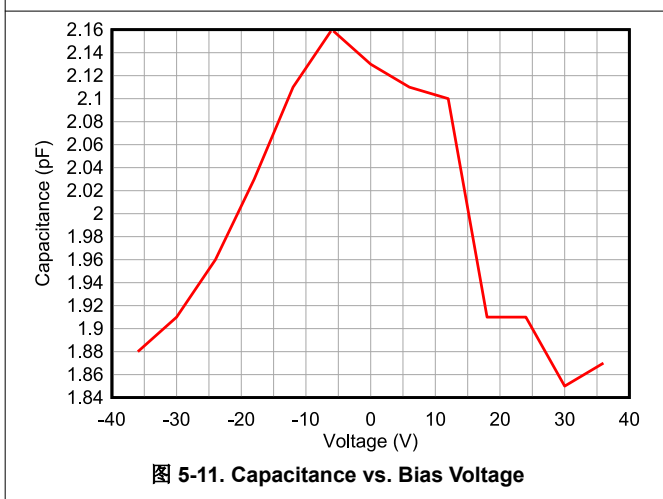
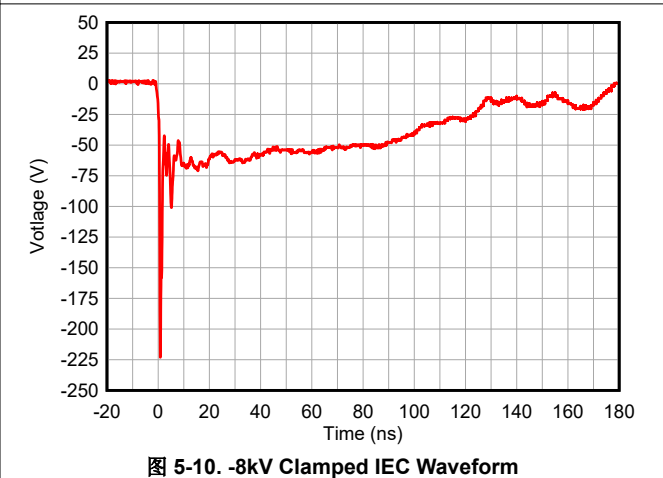
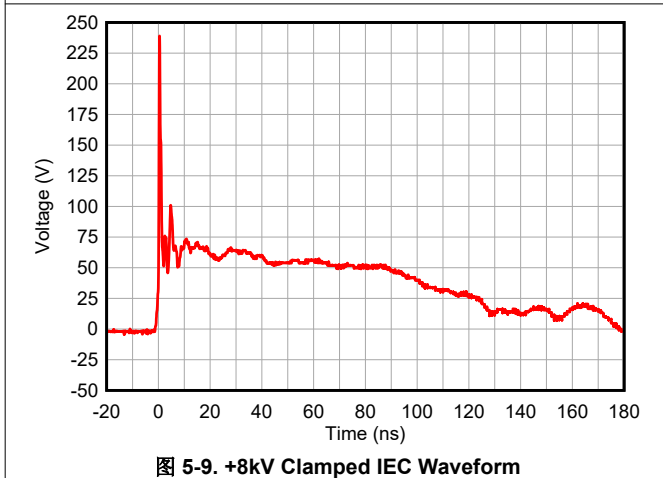
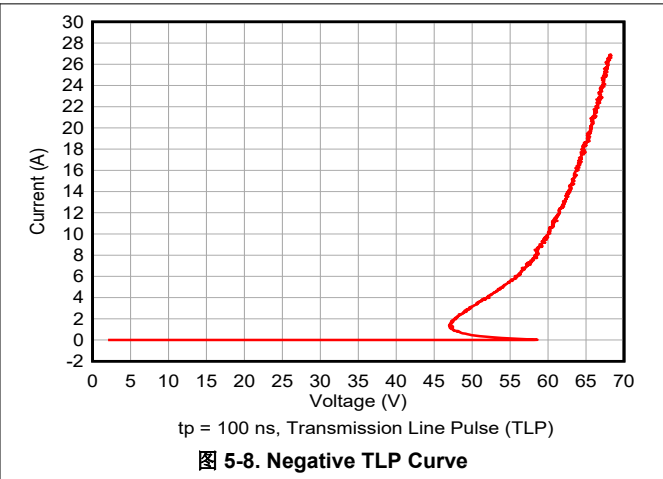
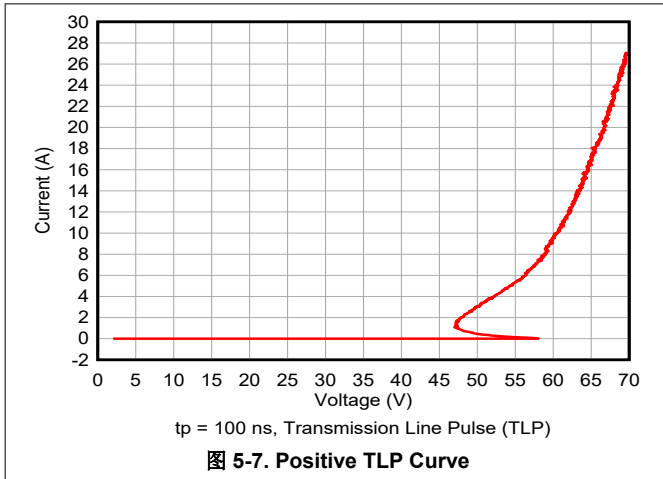


图 5-6. Leakage Current vs. Bias Voltage Across Temperature

5.9 Typical Characteristics- ESD2CANFD36-Q1



6 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD2CANxx36-Q1 is a dual channel TVS diode that provides a path to ground for dissipating ESD events on differential CAN signal lines. The CAN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

7.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

7.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (February 2024) to Revision A (March 2024)	Page
• 将数据表状态从 预告信息 更改为 “量产数据”	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD2CAN36DBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z18
ESD2CAN36DBZRQ1.Z	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z18
ESD2CANFD36DBZRQ1	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z58
ESD2CANFD36DBZRQ1.Z	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z58

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CAN36DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD2CANFD36DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

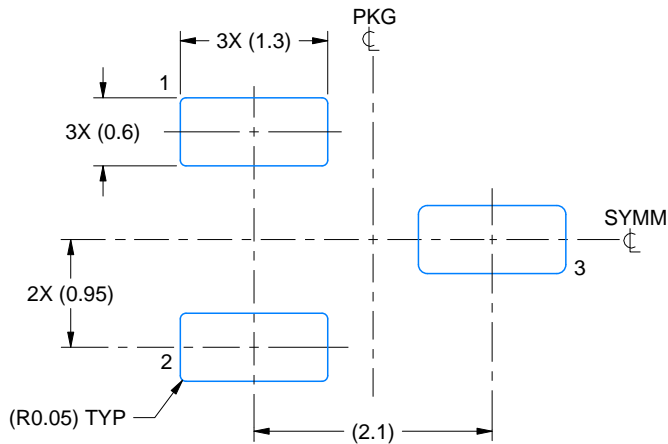
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CAN36DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD2CANFD36DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

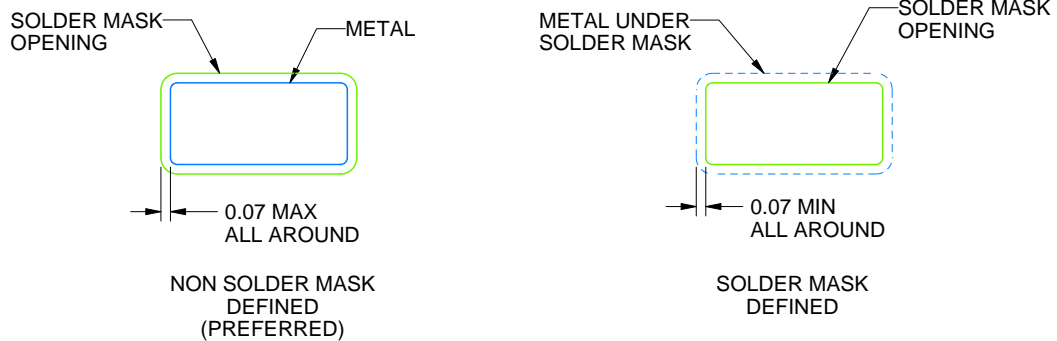
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

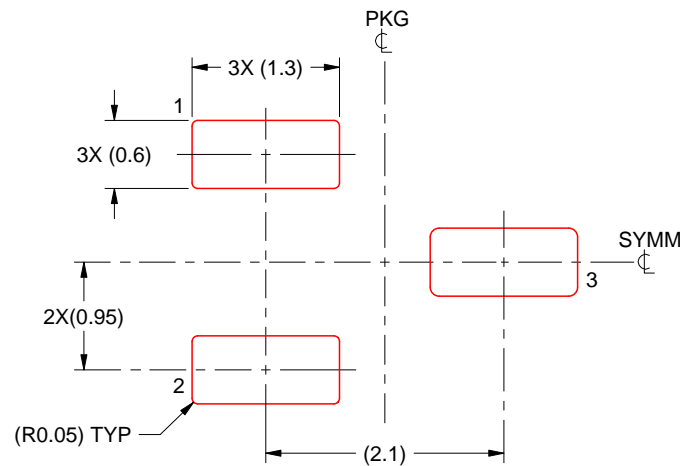
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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