

DS90CF384AQ +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link - 65 MHz

Check for Samples: [DS90CF384AQ](#)

FEATURES

- Automotive Grade Device, AEC-Q100 Grade 3 Qualified
- Operating Temperature Range: -40°C to $+85^{\circ}\text{C}$
- 20 to 65 MHz Shift Clock Support
- 50% Duty Cycle on Receiver Output Clock
- Best-in-Class Set & Hold Times on RxOUTPUTs
- Rx Power Consumption <142 mW (typ) @65MHz Grayscale
- Rx Power-down Mode <200 μW (max)
- ESD Rating >7 kV (HBM), >700V (EIAJ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- PLL Requires No External Components
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 56-Lead TSSOP Package

DESCRIPTION

The DS90CF384AQ receiver converts the four LVDS data streams at up to 1.8 Gbps throughput (227 Megabytes/sec bandwidth) back into parallel 28 bits of LVCMOS/LVTTL data. In a Display application, the 28 bits include: 24 bits of RGB data and up to 4 bits of video control (Hsync, Vsync, DE and CNTL).

The DS90CF384AQ device is enhanced over prior generation FPD-Link receivers, provides a wider data valid time on the receiver output and is offered as an AEC-Q100 grade 3 device.

FPD-Link is an ideal means to solve EMI and cable size problems associated with wide, high speed LVCMOS/LVTTL interfaces.

Block Diagram

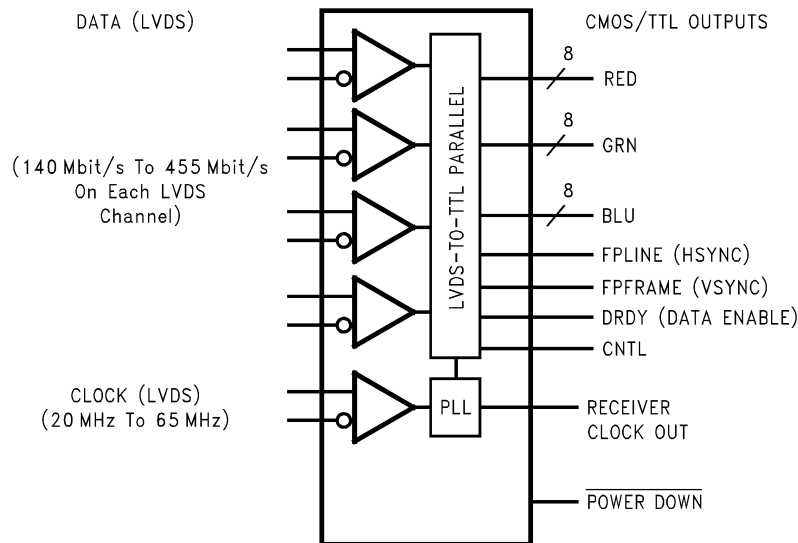


Figure 1. DS90CF384AQ Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.3V to +4V
LVCMOS/LVTTL Input Voltage		-0.3V to ($V_{CC} + 0.3V$)
LVCMOS/LVTTL Output Voltage		-0.3V to ($V_{CC} + 0.3V$)
LVDS Receiver Input Voltage		-0.3V to ($V_{CC} + 0.3V$)
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
For soldering specifications: see http://www.ti.com/lit/SNOA549		
Maximum Package Power Dissipation Capacity @ 25°C		
DGG Package:		1.61 W
DGG Package Derating:		12.4 mW/°C above +25°C
ESD Rating	(HBM, 1.5 kΩ, 100 pF)	> 7 kV
	(EIAJ, 0Ω, 200 pF)	> 700V

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

(2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	-40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV _{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (For Power Down Pin)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V
I_{IN}	Input Current	$V_{IN} = 0.4V, 2.5V$ or V_{CC}		+1.8	+10	μA
		$V_{IN} = GND$	-10	0		μA
LVCMOS/LVTTL DC SPECIFICATIONS						
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4$ mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA		0.06	0.3	V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$		-60	-120	mA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	$V_{CM} = +1.2V$			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	$V_{IN} = +2.4V, V_{CC} = 3.6V$			±10	μA
		$V_{IN} = 0V, V_{CC} = 3.6V$			±10	μA

(1) Typical values are given for $V_{CC} = 3.3V$ and $T_A = +25°C$.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Units	
RECEIVER SUPPLY CURRENT⁽²⁾							
ICCRW	Receiver Supply Current Worst Case	$C_L = 8$ pF, Worst Case Pattern (Figure 2 and Figure 4)	f = 32.5 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 65 MHz		81	105	mA
ICCRG	Receiver Supply Current, 16 Grayscale	$C_L = 8$ pF, 16 Grayscale Pattern (Figure 3 and Figure 4)	f = 32.5 MHz		28		mA
			f = 37.5 MHz		30		mA
			f = 65 MHz		43		mA
ICCRZ	Receiver Supply Current Power Down	Power Down = Low, Receiver Outputs Stay Low during Power Down Mode		10	55	μA	

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4)			2	5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4)			1.8	5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 10)	f = 25 MHz	1.20	1.96	2.82	ns
RSPos1	Receiver Input Strobe Position for Bit 1		6.91	7.67	8.53	ns
RSPos2	Receiver Input Strobe Position for Bit 2		12.62	13.38	14.24	ns
RSPos3	Receiver Input Strobe Position for Bit 3		18.33	19.09	19.95	ns
RSPos4	Receiver Input Strobe Position for Bit 4		24.04	24.80	25.66	ns
RSPos5	Receiver Input Strobe Position for Bit 5		29.75	30.51	31.37	ns
RSPos6	Receiver Input Strobe Position for Bit 6		35.46	36.22	37.08	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 10)	f = 65 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin ⁽¹⁾ (Figure 11)	f = 25 MHz	750			ps
		f = 65 MHz	500			ps
RCOP	RxCLK OUT Period (Figure 5)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 5)	f = 65 MHz	5.0	7.6	9.0	ns
RCOL	RxCLK OUT Low Time (Figure 5)		5.0	6.3	9.0	ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 5)		4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 5)		4.0	6.3		ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, $V_{CC} = 3.3V$ (Figure 6)		3.5	5.0	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 7)			10	ms	
RPDD	Receiver Power Down Delay (Figure 9)			1	μs	

(1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the DS90C383B transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). The RSKM will change when different transmitters are used. This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

AC Timing Diagrams

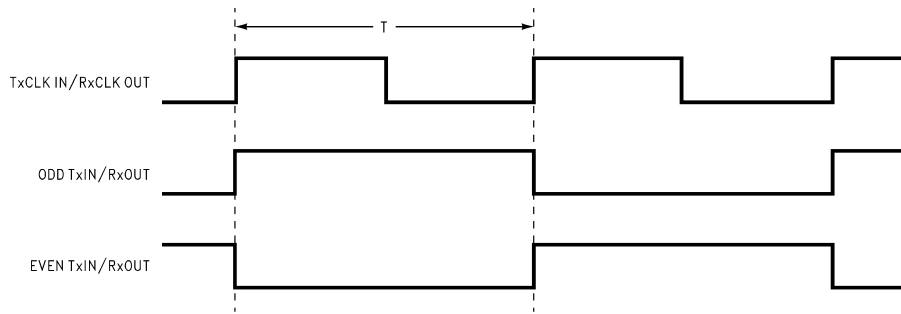


Figure 2. "Worst Case" Test Pattern

Device Pin Name	Signal	Signal Pattern	Signal Frequency
TxCLK IN/RxCLK OUT	Dot Clk	[Square Wave]	f
TxIN0/RxOUT0	R0	[Pattern]	f/16
TxIN1/RxOUT1	R1	[Pattern]	f/8
TxIN2/RxOUT2	R2	[Pattern]	f/4
TxIN3/RxOUT3	R3	[Pattern]	f/2
TxIN4/RxOUT4	R4	[Steady State, Low]	Steady State, Low
TxIN5/RxOUT5	R7	[Steady State, Low]	Steady State, Low
TxIN6/RxOUT6	R5	[Steady State, Low]	Steady State, Low
TxIN7/RxOUT7	G0	[Steady State, Low]	Steady State, Low
TxIN8/RxOUT8	G1	[Pattern]	f/16
TxIN9/RxOUT9	G2	[Pattern]	f/8
TxIN10/RxOUT10	G6	[Pattern]	f/4
TxIN11/RxOUT11	G7	[Pattern]	f/2
TxIN12/RxOUT12	G3	[Steady State, Low]	Steady State, Low
TxIN13/RxOUT13	G4	[Steady State, Low]	Steady State, Low
TxIN14/RxOUT14	G5	[Steady State, Low]	Steady State, Low
TxIN15/RxOUT15	B0	[Steady State, Low]	Steady State, Low
TxIN16/RxOUT16	B6	[Pattern]	f/16
TxIN17/RxOUT17	B7	[Pattern]	f/8
TxIN18/RxOUT18	B1	[Pattern]	f/4
TxIN19/RxOUT19	B2	[Pattern]	f/2
TxIN20/RxOUT20	B3	[Steady State, Low]	Steady State, Low
TxIN21/RxOUT21	B4	[Steady State, Low]	Steady State, Low
TxIN22/RxOUT22	B5	[Steady State, Low]	Steady State, Low
TxIN23/RxOUT23	RES	[Steady State, Low]	Steady State, Low
TxIN24/RxOUT24	HSYNC	[Steady State, High]	Steady State, High
TxIN25/RxOUT25	VSYNC	[Steady State, High]	Steady State, High
TxIN26/RxOUT26	EN	[Steady State, High]	Steady State, High
TxIN27/RxOUT27	R6	[Steady State, High]	Steady State, High

The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN / RxCLK OUT).

Recommended pin to signal mapping. Application may choose to define differently, check compatibility with source.

Figure 3. "16 Grayscale" Test Pattern

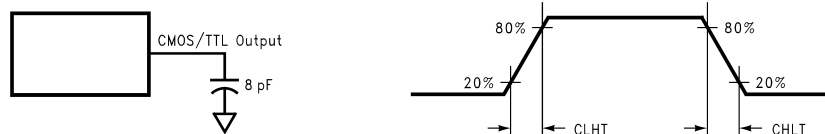


Figure 4. Receiver CMOS/TTL Output Load and Transition Times

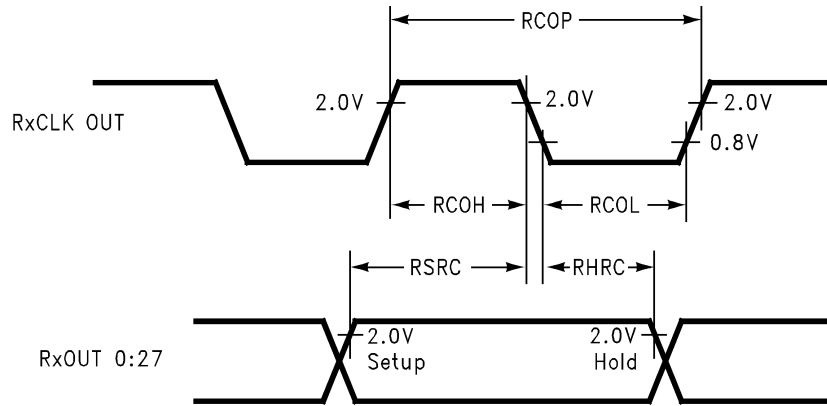


Figure 5. Receiver Output Setup/Hold and High/Low Times

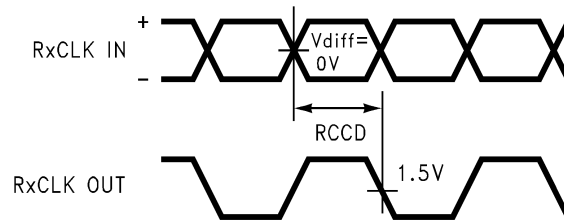


Figure 6. Receiver Clock In to Clock Out Delay

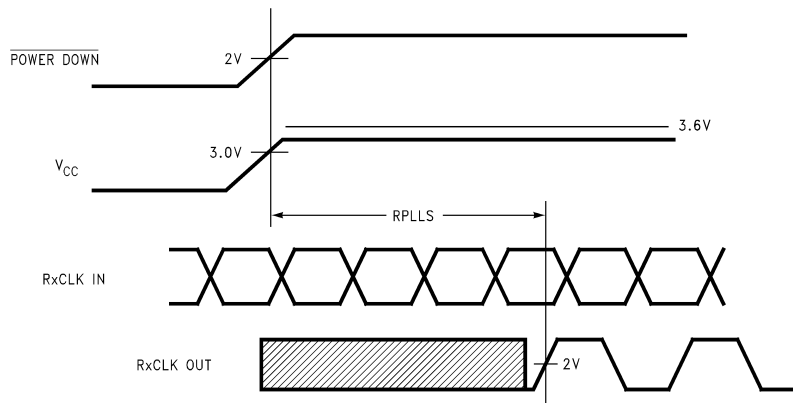


Figure 7. Receiver Phase Lock Loop Set Time

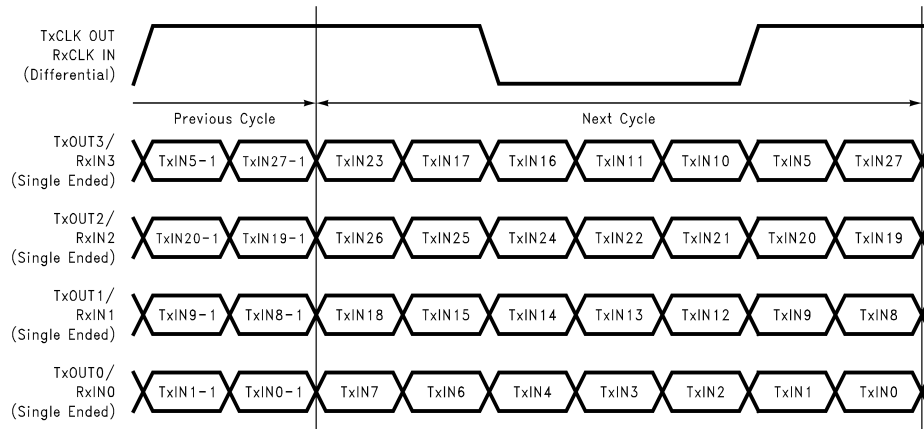


Figure 8. 28 Parallel TTL Data Inputs/Outputs Mapped to LVDS Bits (TxINn / RxOUTn)

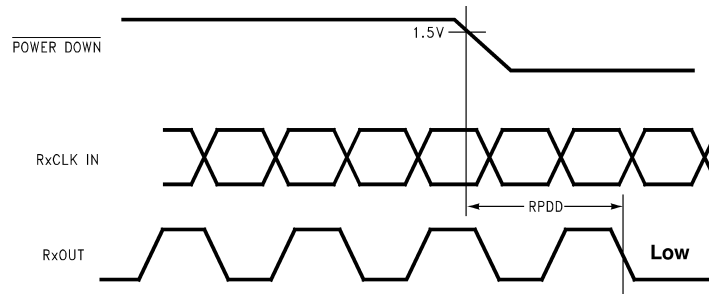


Figure 9. Receiver Power Down Delay

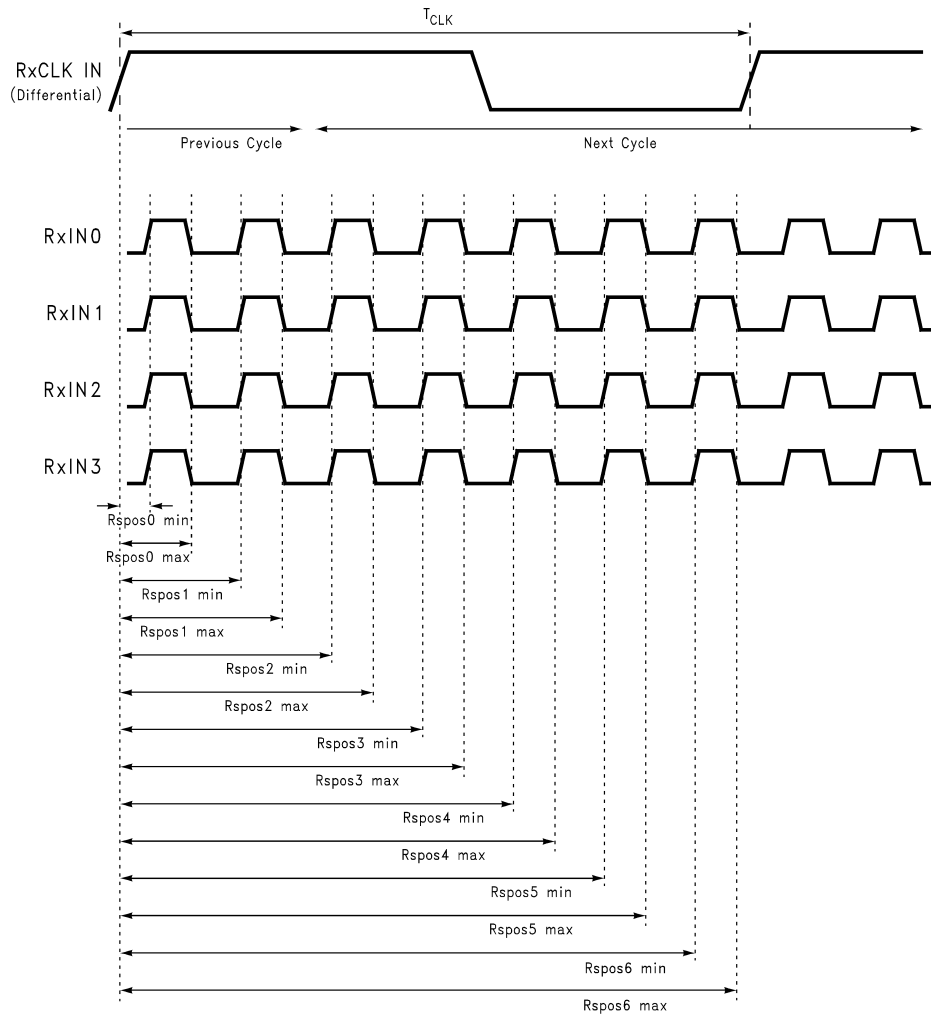
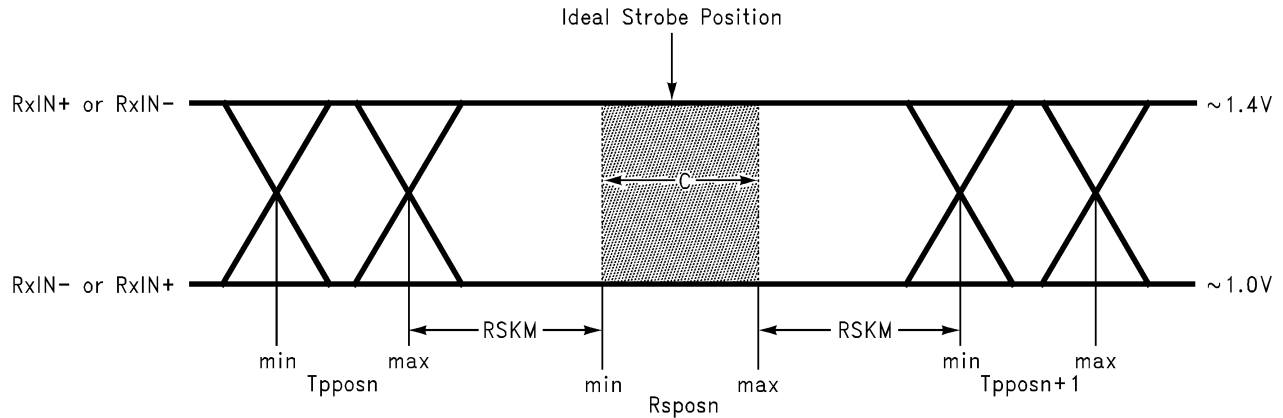


Figure 10. Receiver LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
 Tppos—Transmitter output pulse position (min and max)
 RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
 Cable Skew—typically 10 ps–40 ps per foot, media dependent
 Cycle-to-cycle jitter is less than 250 ps at 65 MHz.
 ISI is dependent on interconnect length; may be zero.

Figure 11. Receiver LVDS Input Skew Margin

DS90CF384AQ Pin Descriptions — 56L TSSOP Package

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN-	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN-	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
PWR DOWN	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V _{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V _{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V _{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Pin Diagram for TSSOP Package

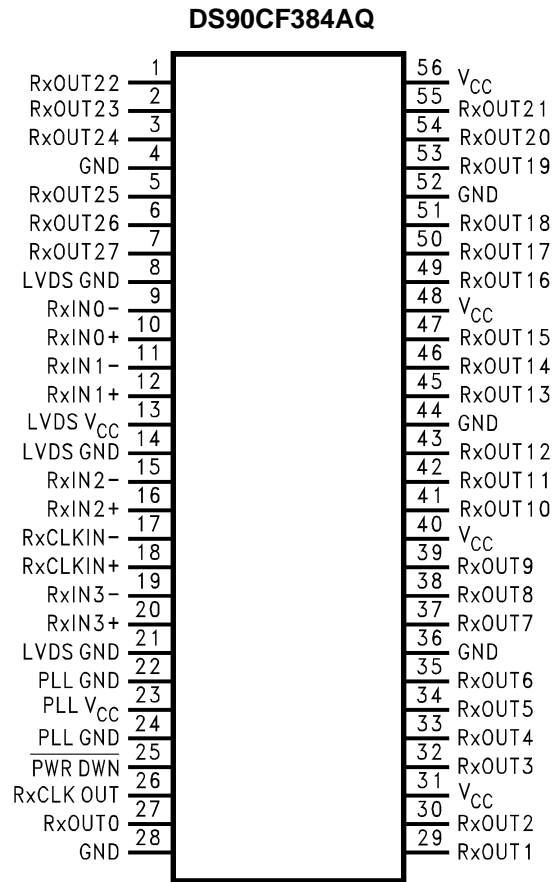


Figure 12. 56-Lead TSSOP (DGG Package)

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90CF384AQMT/ NOPB	Active	Production	TSSOP (DGG) 56	34 TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CF384AQ MT

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF384AQM TX/ NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF384AQMXX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS90CF384AQMT/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CF384AQMT/ NOPB.Z	DGG	TSSOP	56	34	495	10	2540	5.79

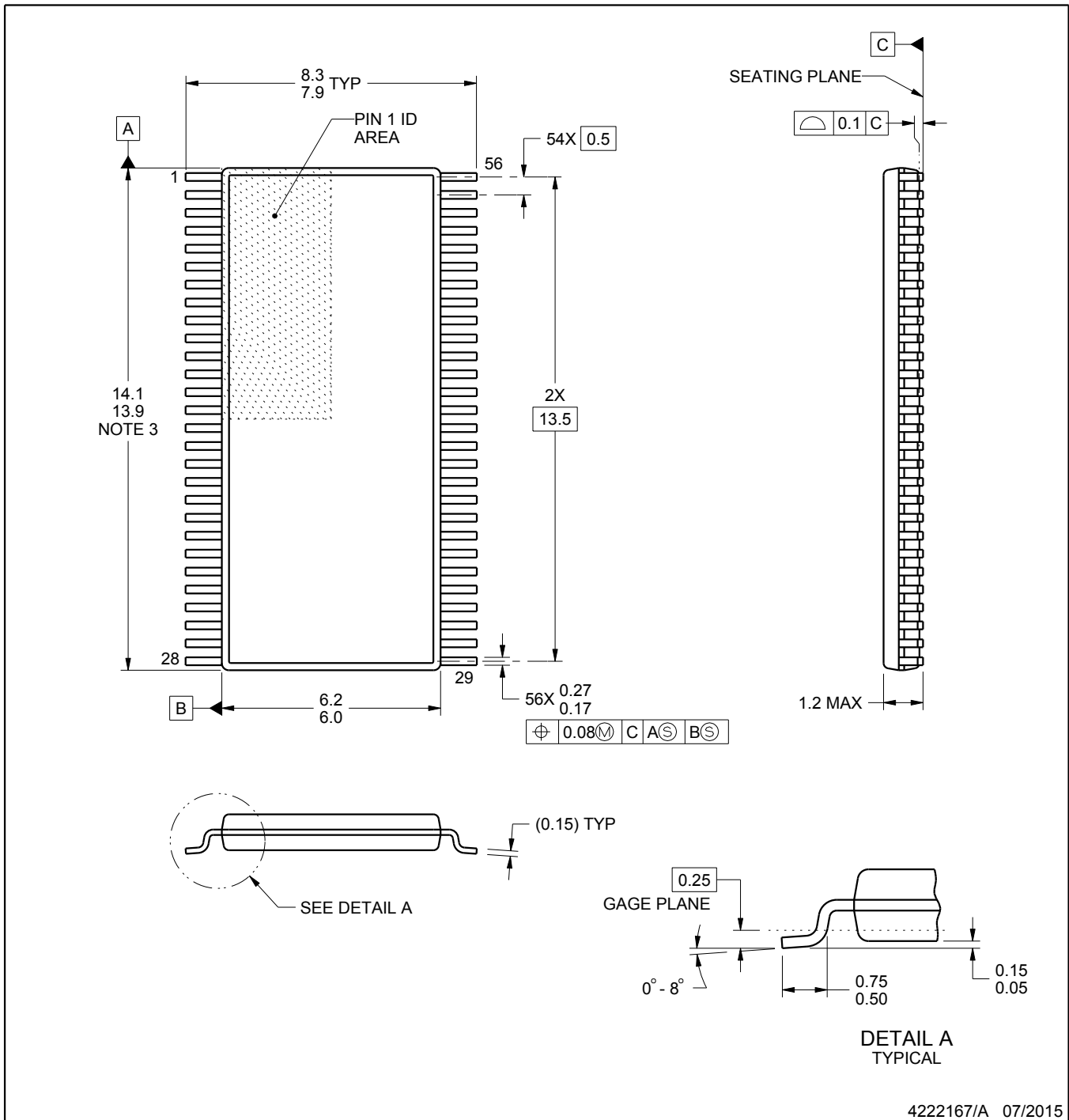
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

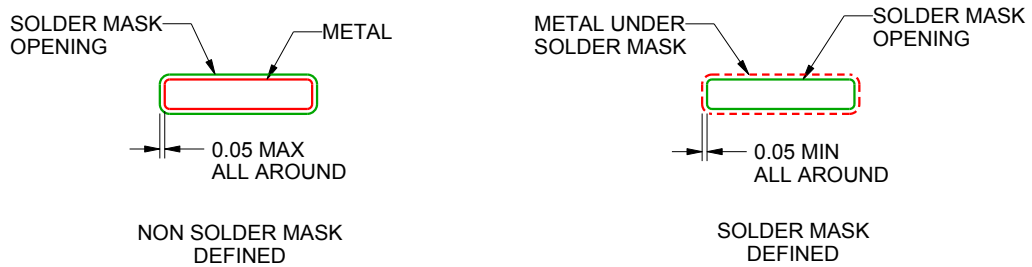
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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