

DS26C31x CMOS Quad Tri-State Differential Line Driver

1 Features

- TTL Input Compatible
- Typical Propagation Delays: 6 ns
- Typical Output Skew: 0.5 ns
- Outputs Will Not Load Line When $V_{CC} = 0$ V
- DS26C31T Meets the Requirements of EIA Standard RS-422
- Operation From Single 5-V Supply
- Tri-State Outputs for Connection to System Buses
- Low Quiescent Current
- Available in Surface Mount
- Mil-Std-883C Compliant

2 Applications

Differential Line Driver for RS-422 Applications

3 Description

The DS26C31 device is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken⁽²⁾. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-------------|---------------------|
| DS26C31M | SNLS3759577 | 9.90 mm × 3.91 mm |
| | PDIP (16) | 19.304 mm × 6.35 mm |
| DS26C31T | SNLS3759577 | 9.90 mm × 3.91 mm |
| | PDIP (16) | 19.304 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The DS26C31M (–55°C to 125°C) is tested with V_{OUT} between 6 V and 0 V while RS-422A condition is 6 V and –0.25 V.

4 Device Logic Diagram

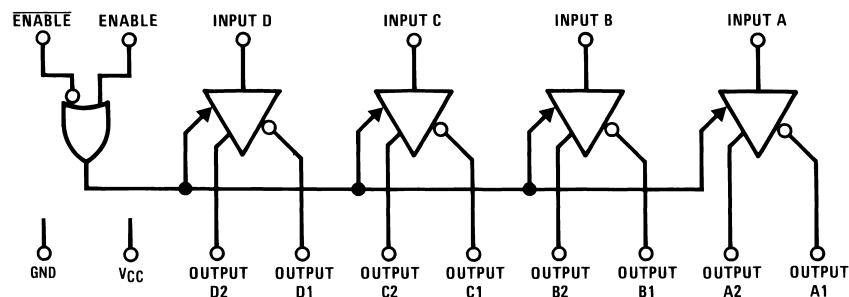


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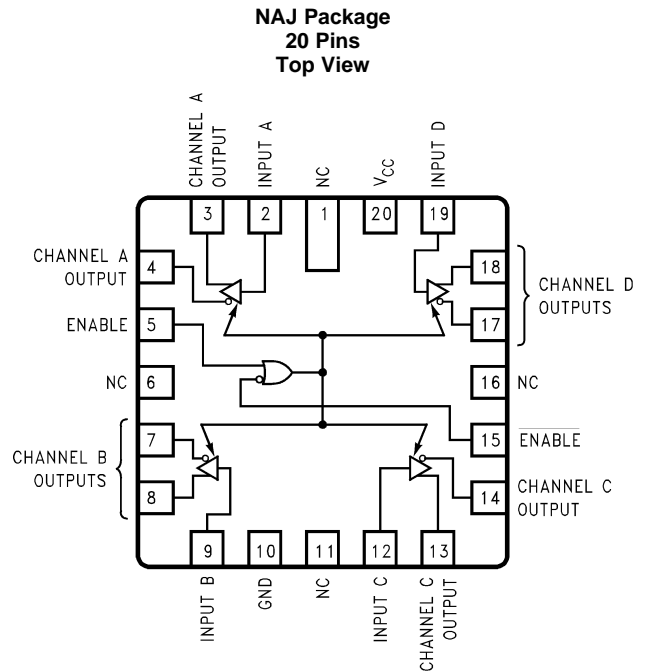
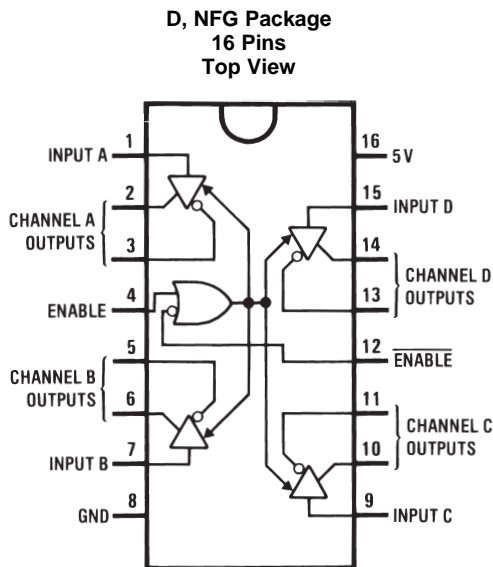
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (April 2013) to Revision C | Page |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> Added <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |

| Changes from Revision A (April 2013) to Revision B | Page |
|------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> Changed layout of National Data Sheet to TI format | 9 |

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------------------------|---------|-----|-------------------------------------------------------------------|
| NAME | NO. (1) | | |
| DIFFERENTIAL SIGNALING I/O | | | |
| CHANNEL A OUTPUTS (-, +) | 3, 2 | O | Channel A inverting and non-inverting differential driver outputs |
| CHANNEL B OUTPUTS (-, +) | 5, 6 | O | Channel B inverting and non-inverting differential driver outputs |
| CHANNEL C OUTPUTS (-, +) | 11, 10 | O | Channel C inverting and non-inverting differential driver outputs |
| CHANNEL D OUTPUTS (-, +) | 13, 14 | O | Channel D inverting and non-inverting differential driver outputs |
| INPUT A | 1 | I | TTL/CMOS compatible input for channel A |
| INPUT B | 7 | I | TTL/CMOS compatible input for channel B |
| INPUT C | 9 | I | TTL/CMOS compatible input for channel C |
| INPUT D | 15 | I | TTL/CMOS compatible input for channel D |
| CONTROL PINS | | | |
| ENABLE | 4 | I | Logic-high ENABLE Control |
| ENABLE | 12 | I | Logic-low ENABLE Control |
| POWER | | | |
| GND | 8 | — | GND Pin |
| VCC | 16 | — | Supply pin, provide 5 V supply |

(1) Pin numbers correspond to PDIP and SOIC packages.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| | | MIN | MAX | UNIT |
|--------------------------------------------------------|-----------------------|------|----------------|------|
| Supply Voltage (V_{CC}) | | -0.5 | 7 | V |
| DC Input Voltage (V_{IN}) | | -1.5 | $V_{CC} + 1.5$ | V |
| DC Output Voltage (V_{OUT}) | | -0.5 | 7 | V |
| Clamp Diode Current (I_{IK}, I_{OK}) | | -20 | 20 | mA |
| DC Output Current, per pin (I_{OUT}) | | -150 | 150 | mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | | | | |
| Max Power Dissipation (P_D) at 25°C ⁽⁴⁾ | Ceramic "NFE" package | | 2419 | mW |
| | Plastic "NFG" package | | 1736 | mW |
| | SOIC "D" package | | 1226 | mW |
| | Ceramic "NAD" package | | 1182 | mW |
| | Ceramic "NAJ" package | | 2134 | mW |
| Lead Temperature (T_L) | (Soldering, 4 s) | | 260 | °C |
| Storage Temperature, T_{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG package at 13.89 mW/°C, NFE package 16.13 mW/°C, D package 9.80 mW/°C, NAJ package 12.20 mW/°C, and NAD package 6.75 mW/°C.

7.2 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-----------------------------------------|-----------------------|------|----------|------|
| Supply Voltage (V_{CC}) | | 4.50 | 5.50 | V |
| DC Input or Output Voltage | (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temperature Range (T_A) | DS26C31T | -40 | 85 | °C |
| | DS26C31M | -55 | 125 | °C |
| Input Rise or Fall Times (t_r, t_f) | | | 500 | ns |

7.3 DC Electrical Characteristics

 $V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise specified)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------------------|-------------------------------------------------|--------------------------------------------------------------|----------------------------------------------------------|---------------------------------------|---------------|---------------|
| V_{IH} | High Level Input Voltage | 2.0 | | | V | |
| V_{IL} | Low Level Input Voltage | | | 0.8 | V | |
| V_{OH} | High Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = -20\text{ mA}$ | 3.4 | | V | |
| V_{OL} | Low Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 20\text{ mA}$ | 0.3 | 0.5 | V | |
| V_T | Differential Output Voltage | $R_L = 100\ \Omega$ See ⁽²⁾ | 3.1 | | V | |
| $ V_T - \overline{V_T} $ | Difference In Differential Output | $R_L = 100\ \Omega$ See ⁽²⁾ | | 0.4 | V | |
| V_{OS} | Common Mode Output Voltage | $R_L = 100\ \Omega$ See ⁽²⁾ | 1.8 | 3.0 | V | |
| $ V_{OS} - \overline{V_{OS}} $ | Difference In Common Mode Output | $R_L = 100\ \Omega$ See ⁽²⁾ | | 0.4 | V | |
| I_{IN} | Input Current | $V_{IN} = V_{CC}, \text{GND}, V_{IH}, \text{ or } V_{IL}$ | | ± 1.0 | μA | |
| I_{CC} | Quiescent Supply Current ⁽³⁾ | DS26C31T | $V_{IN} = V_{CC}$ or GND | 200 | 500 | μA |
| | | | $V_{IN} = 2.4\text{ V}$ or 0.5 V ⁽³⁾ | 0.8 | 2.0 | mA |
| | | DS26C31M | $V_{IN} = V_{CC}$ or GND | 200 | 500 | μA |
| | | | $V_{IN} = 2.4\text{ V}$ or 0.5 V ⁽³⁾ | 0.8 | 2.1 | mA |
| I_{OZ} | TRI-STATE Output Leakage Current | $V_{OUT} = V_{CC}$ or GND | | | | |
| | | ENABLE = V_{IL} | | ± 0.5 | ± 5.0 | μA |
| | | ENABLE = V_{IH} | | | | |
| I_{SC} | Output Short Circuit Current | $V_{IN} = V_{CC}$ or GND ⁽²⁾⁽⁴⁾ | | -30 | -150 | mA |
| I_{OFF} | Output Leakage Current Power Off ⁽²⁾ | DS26C31T | $V_{OUT} = 6\text{ V}$ | | 100 | μA |
| | | | $V_{CC} = 0\text{ V}$ | $V_{OUT} = -0.25\text{ V}$ | | -100 |
| | | DS26C31M | $V_{OUT} = 6\text{ V}$ | | 100 | μA |
| | | | $V_{CC} = 0\text{ V}$ | $V_{OUT} = 0\text{ V}$ ⁽⁵⁾ | | -100 |

(1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) See EIA Specification RS-422 for exact test conditions.

(3) Measured per input. All other inputs at V_{CC} or GND.

(4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

(5) The DS26C31M (-55°C to $+125^\circ\text{C}$) is tested with V_{OUT} between $+6\text{ V}$ and 0 V while RS-422A condition is $+6\text{ V}$ and -0.25 V .

7.4 Switching Characteristics

 $V_{CC} = 5\text{ V} \pm 10\%$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$ (Figure 22, Figure 23, Figure 24, Figure 25)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | DS26C31T | DS26C31M | UNIT |
|-----------------------|----------------------------------------------|-----|-----|----------|----------|------|
| | | | | MAX | MAX | |
| t_{PLH} , t_{PHL} | Propagation Delays Input to Output | 2 | 6 | 11 | 14 | ns |
| Skew | ⁽²⁾ | | 0.5 | 2.0 | 3.0 | ns |
| t_{TLH} , t_{THL} | Differential Output Rise And Fall Times | | 6 | 10 | 14 | ns |
| t_{PZH} | Output Enable Time | | 11 | 19 | 22 | ns |
| t_{PZL} | Output Enable Time | | 13 | 21 | 28 | ns |
| t_{PHZ} | Output Disable Time ⁽³⁾ | | 5 | 9 | 12 | ns |
| t_{PLZ} | Output Disable Time ⁽³⁾ | | 7 | 11 | 14 | ns |
| C_{PD} | Power Dissipation Capacitance ⁽⁴⁾ | | 50 | | | pF |
| C_{IN} | Input Capacitance | | 6 | | | pF |

- Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.
- Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
- Output disable time is the delay from $\overline{\text{ENABLE}}$ or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
- C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

7.5 Comparison Table of Switching Characteristics into “LS-Type” Load

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$ (Figure 23, Figure 25, Figure 26, Figure 27)⁽¹⁾

| PARAMETER | TEST CONDITIONS | DS26C31T | | DS26LS31C | | UNIT |
|-----------------------|-------------------------------------------------------------------------------------------|----------|-----|-----------|-----|------|
| | | TYP | MAX | TYP | MAX | |
| t_{PLH} , t_{PHL} | Propagation Delays Input to Output $C_L = 30\text{ pF}$ S1 Closed S2 Closed | 6 | 8 | 10 | 15 | ns |
| Skew | See ⁽²⁾ $C_L = 30\text{ pF}$ S1 Closed S2 Closed | 0.5 | 1.0 | 2.0 | 6.0 | ns |
| t_{THL} , t_{TLH} | Differential Output Rise and Fall Times $C_L = 30\text{ pF}$ S1 Closed S2 Closed | 4 | 6 | | | ns |
| t_{PLZ} | Output Disable Time ⁽³⁾ $C_L = 10\text{ pF}$ S1 Closed S2 Open | 6 | 9 | 15 | 35 | ns |
| t_{PHZ} | Output Disable Time ⁽³⁾ $C_L = 10\text{ pF}$ S1 Open S2 Closed | 4 | 7 | 15 | 25 | ns |
| t_{PZL} | Output Enable Time $C_L = 30\text{ pF}$ S1 Closed S2 Open | 14 | 20 | 20 | 30 | ns |
| t_{PZH} | Output Enable Time $C_L = 30\text{ pF}$ S1 Open S2 Closed | 11 | 17 | 20 | 30 | ns |

- This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or verified.
- Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
- Output disable time is the delay from $\overline{\text{ENABLE}}$ or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

7.6 Typical Characteristics

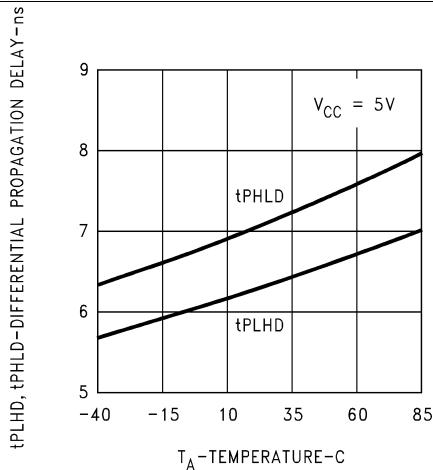


Figure 1. Differential Propagation Delay vs Temperature

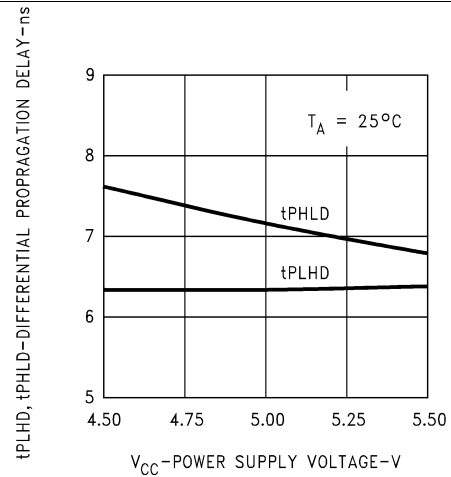


Figure 2. Differential Propagation Delay vs Power Supply Voltage

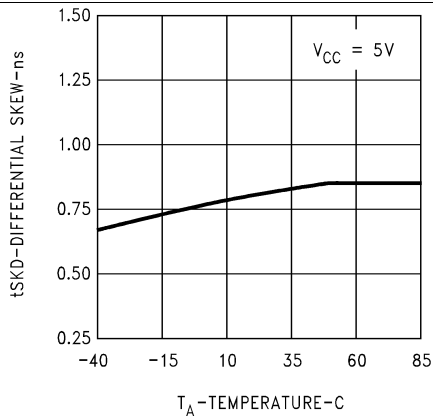


Figure 3. Differential Skew vs Temperature

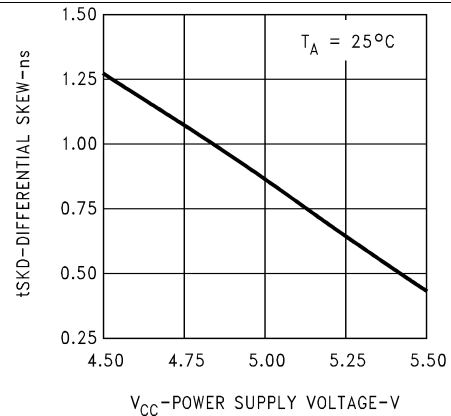


Figure 4. Differential Skew vs Power Supply Voltage

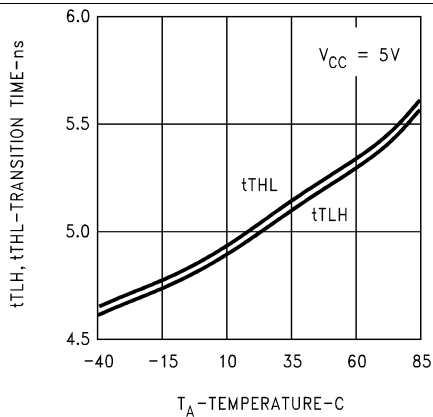


Figure 5. Differential Transition Time vs Temperature

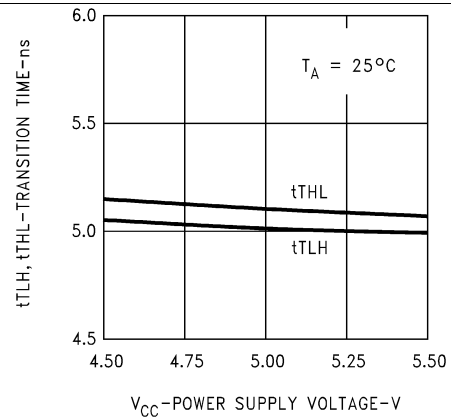


Figure 6. Differential Transition Time vs Power Supply Voltage

Typical Characteristics (continued)

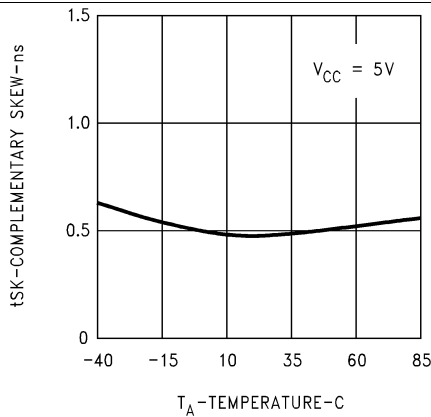


Figure 7. Complementary Skew vs Temperature

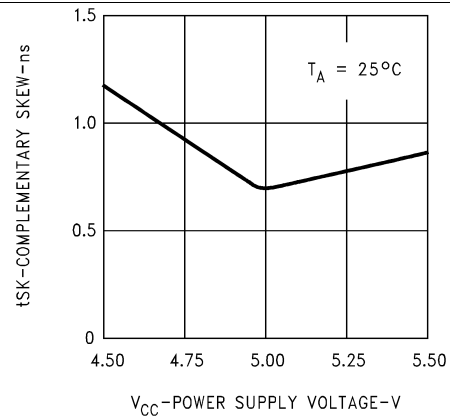


Figure 8. Complementary Skew vs Power Supply Voltage

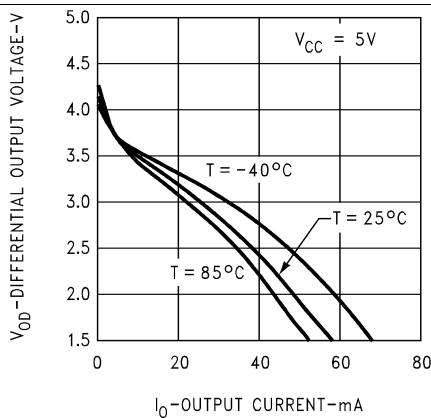


Figure 9. Differential Output Voltage vs Output Current

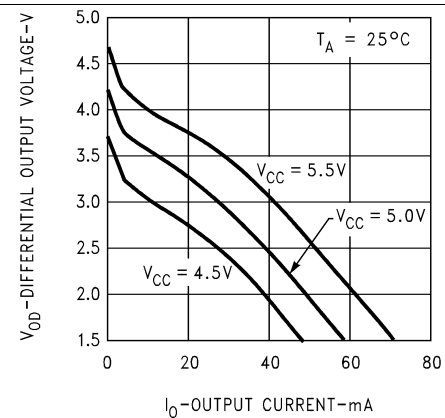


Figure 10. Differential Output Voltage vs Output Current

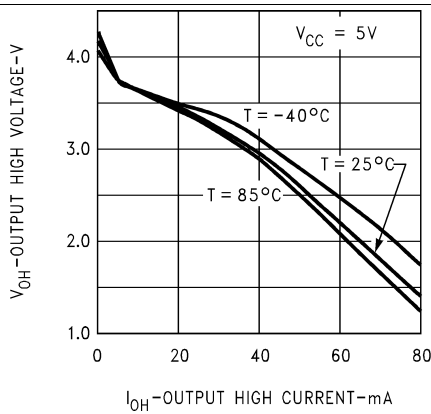


Figure 11. Output High Voltage vs Output High Current

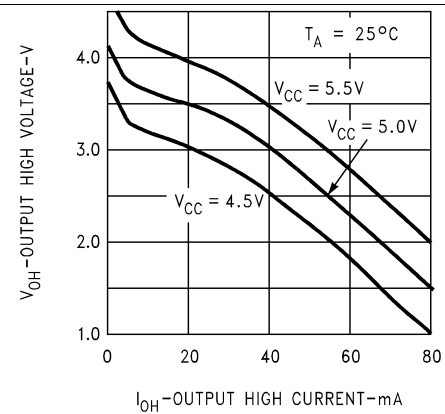


Figure 12. Output High Voltage vs Output High Current

Typical Characteristics (continued)

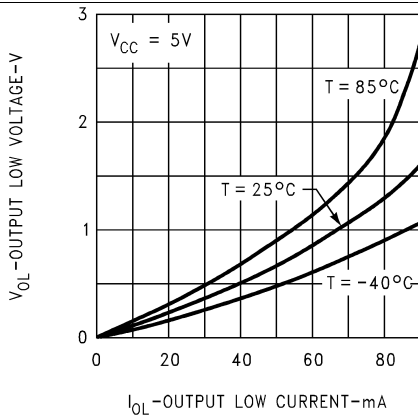


Figure 13. Output Low Voltage vs Output Low Current

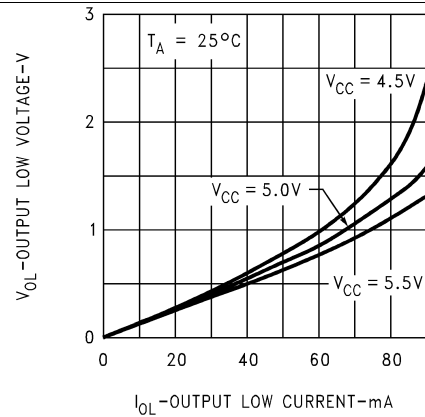


Figure 14. Output Low Voltage vs Output Low Current

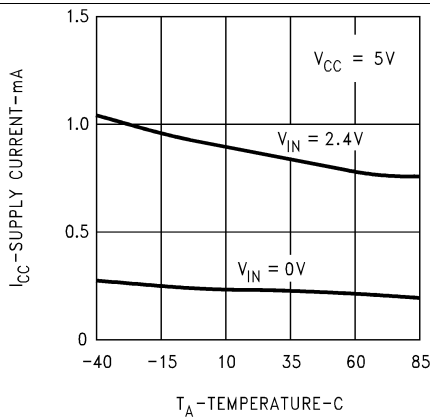


Figure 15. Supply Current vs Temperature

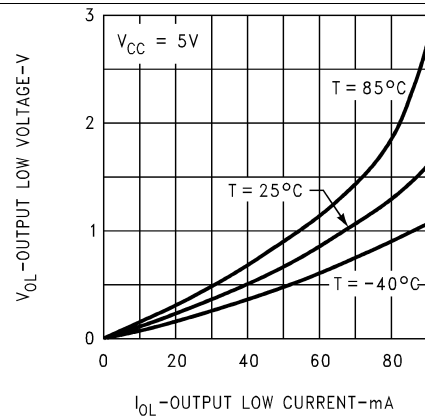


Figure 16. Output Low Voltage vs Output Low Current

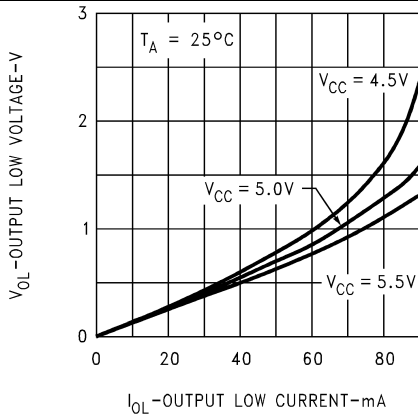


Figure 17. Output Low Voltage vs Output Low Current

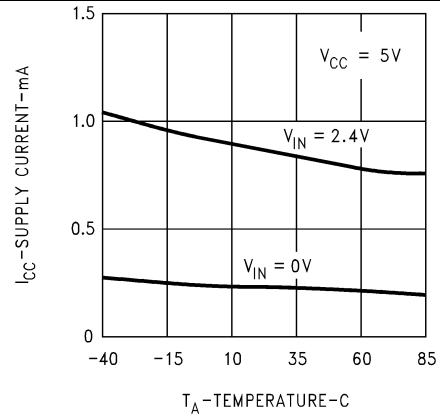


Figure 18. Supply Current vs Temperature

Typical Characteristics (continued)

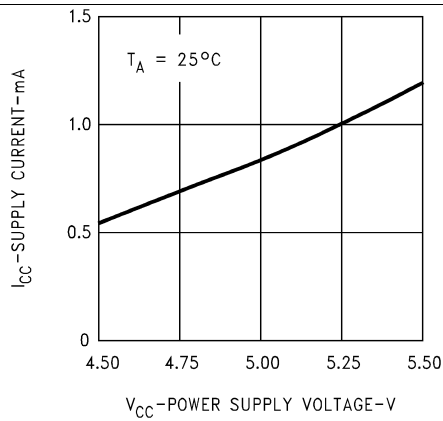


Figure 19. Supply Current vs Power Supply Voltage

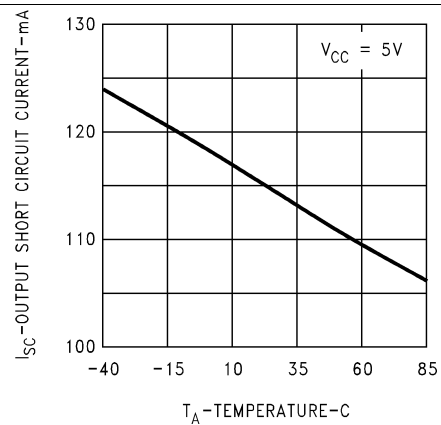


Figure 20. Output Short Circuit Current vs Temperature

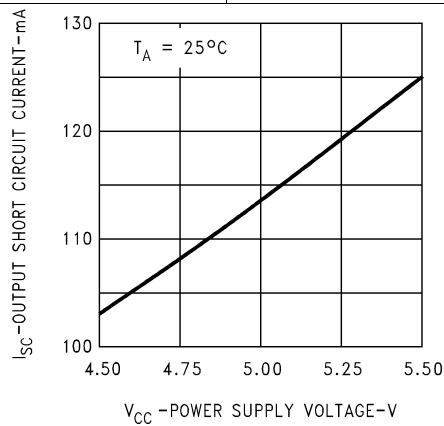
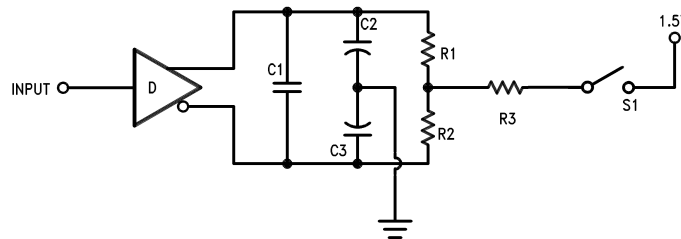


Figure 21. Output Short Circuit Current vs Power Supply Voltage

8 Parameter Measurement Information



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

Figure 22. AC Test Circuit

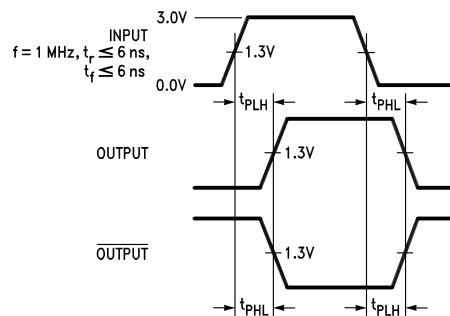


Figure 23. Propagation Delays

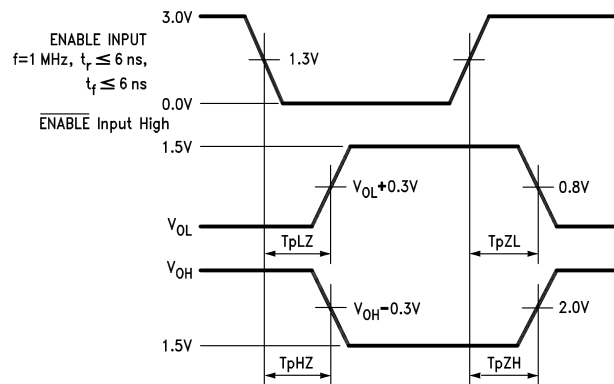
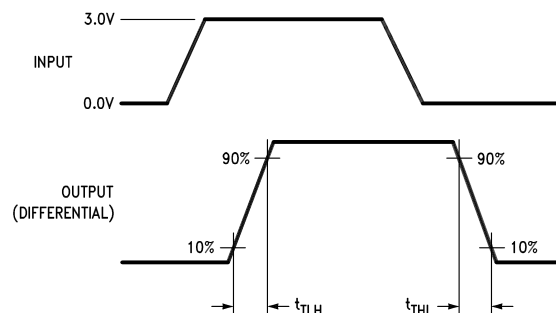
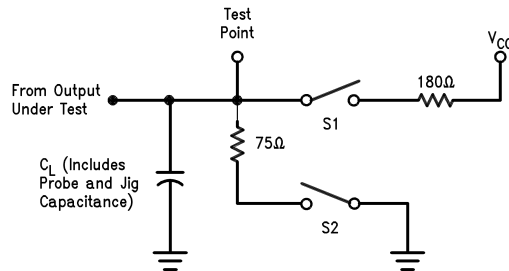
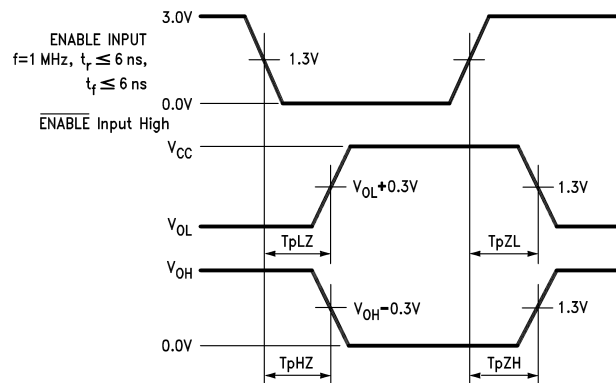


Figure 24. Enable and Disable Times



Input pulse; $f = 1 \text{ MHz}$, 50%; $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$

Figure 25. Differential Rise and Fall Times

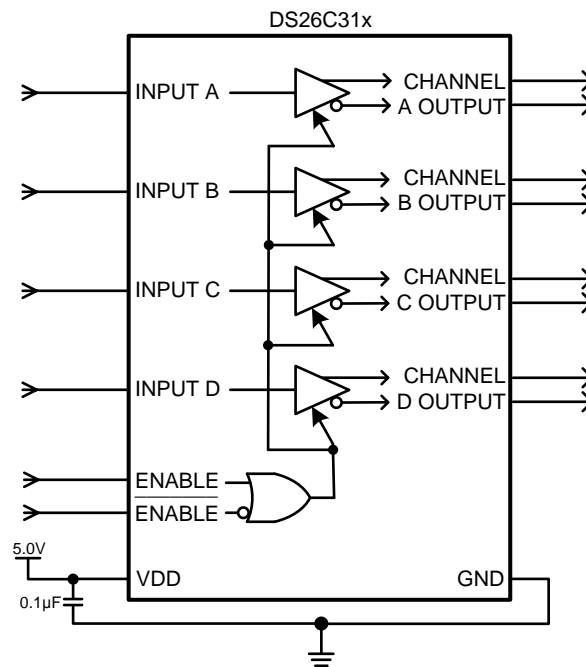
Parameter Measurement Information (continued)

Figure 26. Load AC Test Circuit for “LS-Type” Load

Figure 27. Enable and Disable Times for “LS-Type” Load

9 Detailed Description

9.1 Overview

The DS26C31 is a quad differential line driver designed for data transmission over balanced cable or printed circuit board traces. The DS26C31M supports a temperature range of -55°C to 125°C, while the DS26C31T supports a temperature range of -40°C to 85°C.

9.2 Functional Block Diagram



9.3 Feature Description

Each driver converts the TTL or CMOS signal at its input to a pair of complementary differential outputs. The drivers are enabled when the ENABLE control pin is a logic HIGH or when the $\overline{\text{ENABLE}}$ control pin is a logic LOW.

9.4 Device Functional Modes

Table 1. Function Table⁽¹⁾

| ENABLE | $\overline{\text{ENABLE}}$ | INPUT | NON-INVERTING OUTPUT | INVERTING OUTPUT |
|-----------------------------------------|----------------------------|-------|----------------------|------------------|
| L | H | X | Z | Z |
| All other combinations of enable inputs | | L | L | H |
| | | H | H | L |

- (1) L = Low logic state
X = Irrelevant
H = High logic state
Z = Tri-state (high impedance)

10 Application and Implementation

NOTE

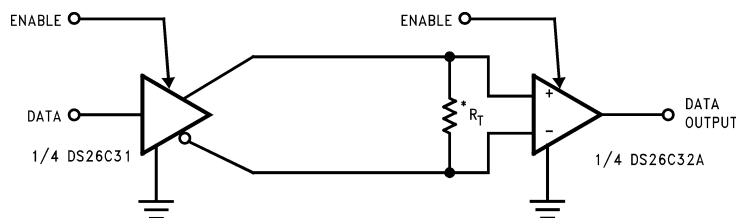
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DS26C31 is a quad differential line driver designed for applications that require long distance digital data transmission over balanced cables. The DS26C31 can be used in applications that require conversion from TTL or CMOS input levels to differential signal levels, compatible to RS-422. The use of complimentary signaling in a balanced transmission media provides good immunity in the midst of noisy environments or shifts in ground reference potential.

10.2 Typical Application

Figure 28 depicts a typical implementation of the DS26C31x device in a RS-422 application.



*R_T is optional although highly recommended to reduce reflection.

Figure 28. Two-Wire Balanced System, RS-422

10.2.1 Design Requirements

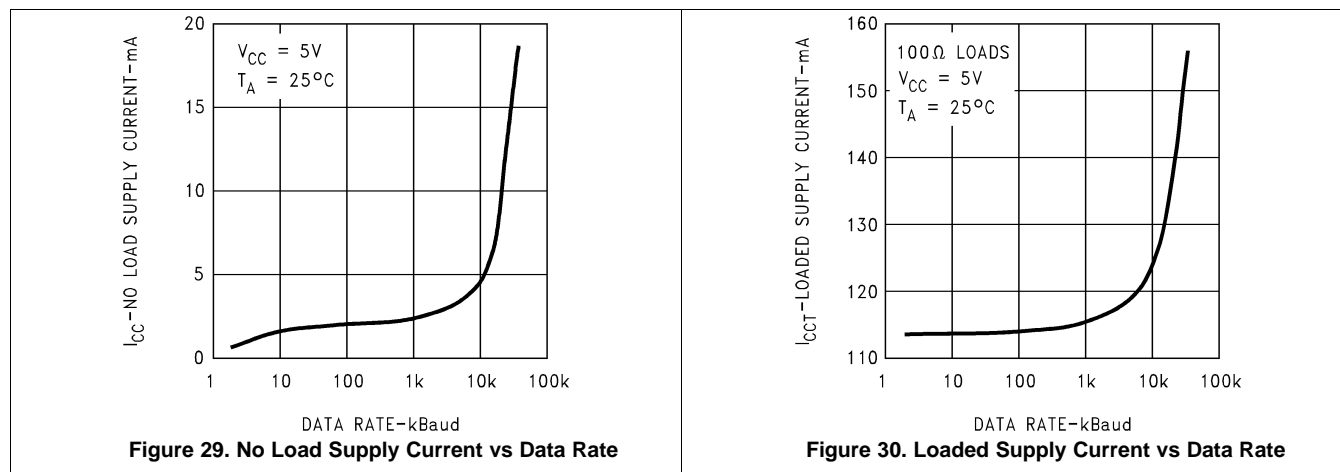
- Apply TTL or LVCMOS signal to driver input lines INPUT A-D.
- Transmit complementary outputs at OUTPUT A-D.
- Use controlled-impedance transmission lines such as printed circuit board traces, twisted-pair wires or parallel wire cable.
- Place a terminating resistor at the far end of the differential pair.

10.2.2 Detailed Design Procedure

- Connect VCC and GND pins to the power and ground planes of the PCB with a 0.1-μF bypass capacitor.
- Use TTL/LVCMOS logic levels at INPUT A-D.
- Use controlled-impedance transmission media for the differential output signals.
- Place an optional terminating resistor at the far-end of the differential pair to avoid reflection.

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

It is recommended that the supply (VCC) and ground (GND) pins be connected to power planes that are placed in the inner layers of the printed circuit board. A 0.1- μ F bypass capacitor should be connect to the VCC pin such that the capacitor is as close as possible to the device.

12 Layout

12.1 Layout Guidelines

The output differential signals of the device should be routed on one layer of the board, and clearance should be provided in order to minimize crosstalk between differential pairs that may be running in parallel over a long distance. Additionally, the differential pairs should have a controlled impedance with minimum impedance discontinuities and be terminated at the far-end, near the receiver, with a resistor that is closely matched to the differential pair impedance in order to minimize transmission line reflections. The differential pairs should be routed with uniform trace width and spacing to minimize impedance mismatching.

12.2 Layout Example

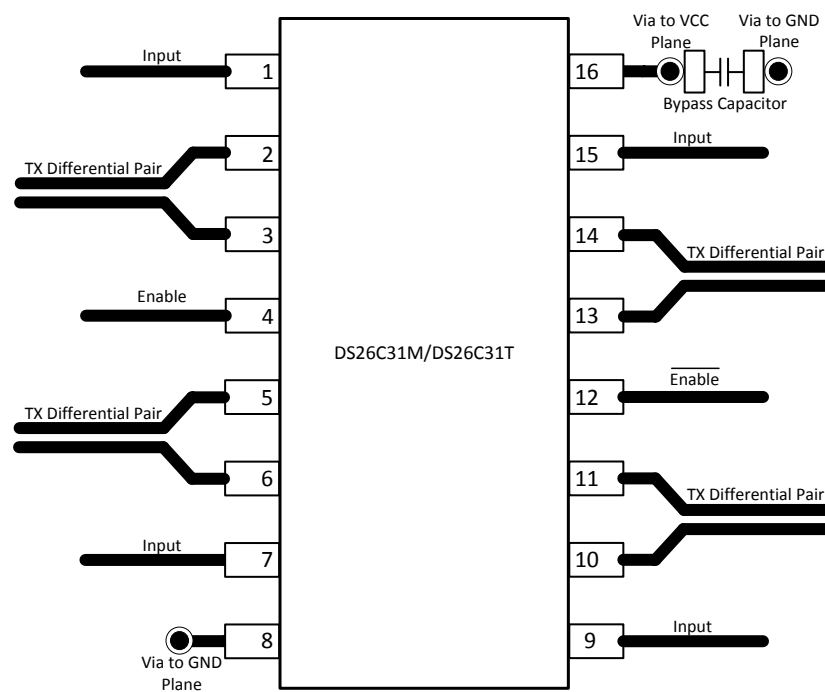


Figure 31. DS26C31 Example Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DS26C31M | Click here | Click here | Click here | Click here | Click here |
| DS26C31T | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DS26C31TM/NOPB | Active | Production | SOIC (D) 16 | 48 TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DS26C31TM |
| DS26C31TM/NOPB.Z | Active | Production | SOIC (D) 16 | 48 TUBE | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DS26C31TM |
| DS26C31TMX/NOPB | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DS26C31TM |
| DS26C31TMX/NOPB.Z | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | DS26C31TM |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS26C31TMX/NOPB | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.3 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS26C31TMX/NOPB | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS26C31TM/NOPB | D | SOIC | 16 | 48 | 495 | 8 | 4064 | 3.05 |
| DS26C31TM/NOPB.Z | D | SOIC | 16 | 48 | 495 | 8 | 4064 | 3.05 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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