FEATURES

- Automatic Equalization of Coaxial, Twin-Ax and Twisted Pair Cables
- High Data Rates: 150 Mbps to 1.5+ Gbps
- Up to 35 dB of Boost at 750 MHz
- LOS Detection and Output Enable
- Single-Ended or Differential Input
- 50Ω Differential Outputs
- Low Power Operation, 210 mW (typ) at 1.5 Gbps
- Industrial -40°C to +85°C Temperature
- Space-Saving 4 x 4 mm WQFN-16 Package

APPLICATIONS

- Cable Extention Applications
- Security Cameras
- Remote LCDs and LED Panels
- Data Recovery Equalization

DESCRIPTION

The DS15EA101 is an adaptive equalizer optimized for equalizing data transmitted over copper cables. The DS15EA101 operates over a wide range of data rates from 150 Mbps to 1.5+ Gbps and automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 35 dB at 750 MHz.

The DS15EA101 allows either single-ended or differential input drive. This enables equalization of coaxial cables as well as differential twin-ax and twisted pair cables.

Additional features include an LOS output and an output enable which, when tied together, disable the output when no signal is present.

The DS15EA101 is powered from a single 3.3V supply and consumes 210 mW at 1.5 Gbps. It operates over the full -40°C to +85°C industrial temperature range and is available in a space saving 4 x 4 mm WQFN-16 package which allows for high density placement of components in multi-channel applications.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Reference</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td>−0.5V to 3.6V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (all inputs)</td>
<td></td>
<td></td>
<td>−0.3V to $V_{CC} +0.3V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>−65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td></td>
<td></td>
<td>+150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature</td>
<td>(Soldering 4 Sec)</td>
<td></td>
<td>+260°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Thermal Resistance</td>
<td></td>
<td></td>
<td>$\theta_{JA}$ RGH0016A</td>
<td>+42.1°C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$\theta_{JC}$ RGH0016A</td>
<td>+8.2°C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Rating (HBM)</td>
<td></td>
<td></td>
<td>8 kV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Rating (MM)</td>
<td></td>
<td></td>
<td>250V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of Electrical Characteristics specifies acceptable device operating conditions.

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Reference</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ($V_{CC}$)</td>
<td></td>
<td></td>
<td>3.3V ±5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Coupling Capacitance</td>
<td></td>
<td></td>
<td>1.0 µF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Loop Capacitor (Connected between CAP+ and CAP-)</td>
<td></td>
<td></td>
<td>1.0 µF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Free Air Temperature ($T_A$)</td>
<td></td>
<td></td>
<td>−40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DC Electrical Characteristics**

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1) (2).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Reference</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CM}$</td>
<td>Input Common Mode Voltage</td>
<td>IN+, IN-</td>
<td>IN+ , IN-</td>
<td>1.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Output Common Mode Voltage</td>
<td>OUT+, OUT-</td>
<td>VOUT, VOUT/2</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing</td>
<td>50Ω load, differential</td>
<td></td>
<td>750</td>
<td>mV_{pp}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LOS}$</td>
<td>LOS Output Voltage</td>
<td>Valid signal not present</td>
<td>LOS</td>
<td>2.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN(EN)}$</td>
<td>EN Input Voltage</td>
<td>Min to disable outputs</td>
<td>EN</td>
<td>3.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td></td>
<td></td>
<td>63</td>
<td>77</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to 0 volts.

(2) Typical values are stated for $V_{CC} = +3.3V$ and $T_A = +25°C$.

(3) Specification is ensured by characterization.

(4) The maximum input voltage amplitude assumes a DC-balanced signal.

(5) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased.
## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified \(^{(1)}\).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Reference</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR(_{\text{IN}})</td>
<td>Input Data Rate</td>
<td>IN+, IN-</td>
<td>150, 1500 Mbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{\text{TRJ}})</td>
<td>Total Residual Jitter @ BER-12 (^{(2)})</td>
<td>1.5 Gbps 25m CAT5e (Belden 1700A), (^{(1)})</td>
<td>0.25</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
</tr>
<tr>
<td>                     1.0 Gbps 50m CAT5e (Belden 1700A), (^{(1)})</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>                     0.5 Gbps 100m CAT5e (Belden 1700A), (^{(1)})</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>                     1.5 Gbps 50m CAT7 (Siemon Tera), (^{(1)})</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>                     1.5 Gbps 75m CAT7 (Siemon Tera), (^{(1)})</td>
<td></td>
<td>0.30</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>                     1.0 Gbps 100m CAT7 (Siemon Tera), (^{(1)})</td>
<td></td>
<td>0.40</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>                     1.5 Gbps 200m Belden 9914, (^{(1)})</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
<td>UI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{\text{TLH}})</td>
<td>Transition Time from Low to High (20% – 80%), (^{(3)})</td>
<td>OUT+, OUT-</td>
<td>100</td>
<td>220</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{\text{THL}})</td>
<td>Transition Time from High to Low (20% – 80%), (^{(3)})</td>
<td></td>
<td>100</td>
<td>220</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R(_{\text{OUT}})</td>
<td>Output Resistance</td>
<td>single-ended, (^{(4)})</td>
<td>50</td>
<td></td>
<td></td>
<td>(\Omega)</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Typical values are stated for \(V_{\text{CC}} = +3.3\text{V}\) and \(T_A = +25^{\circ}\text{C}\).

\(^{(2)}\) The total residual jitter at BER-12 was calculated as \(DJ + 14.1xRJ\), where \(DJ\) is deterministic jitter and \(RJ\) is random jitter. The jitter is expressed as a portion of a unit interval (UI). One UI is a reciprocal of a bit rate (or data rate). For example, a 1.5 Gbps (gigabit per second) signal has \(1 / (1.5 \text{Gb/s}) = 666.67\text{ps}\) (picosecond) unit interval. A 0.25 UI jitter is equivalent to \(0.25 \times 666.67\text{ps} = 166.67\text{ps}\).

\(^{(3)}\) Specification is ensured by characterization.

\(^{(4)}\) Specification is ensured by design.

---

### CONNECTION DIAGRAM

16-Pad WQFN
Package Number RGH0016A
## PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>2</td>
<td>IN+</td>
<td>Non-inverting input pin.</td>
</tr>
<tr>
<td>3</td>
<td>IN-</td>
<td>Inverting input pin.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>5</td>
<td>CAP+</td>
<td>Loop filter positive pin.</td>
</tr>
<tr>
<td>6</td>
<td>CAP-</td>
<td>Loop filter negative pin.</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>10</td>
<td>OUT-</td>
<td>Inverting output pin.</td>
</tr>
<tr>
<td>11</td>
<td>OUT+</td>
<td>Non-inverting output pin.</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>Ground pin.</td>
</tr>
<tr>
<td>13</td>
<td>VCC</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>14</td>
<td>EN</td>
<td>Output enable pin.</td>
</tr>
<tr>
<td>15</td>
<td>LOS</td>
<td>Loss of signal circuitry output pin.</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>Power supply pin.</td>
</tr>
</tbody>
</table>
DEVICE OPERATION

Input Interfacing
The DS15EA101 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported. If the signal is differential, its amplitude must be 800 mVp-p ±10% (400 mV single-ended). If the signal is single-ended, its amplitude must be 800 mV ±10%.

Output Interfacing
The DS15EA101 uses current mode outputs. They are internally terminated with 50Ω. The following two figures illustrate typical DC-coupled interface to common differential receivers and assume that the receivers have high impedance inputs. While most receivers have an input common mode voltage range that can accommodate CML signals, it is recommended to check respective receiver’s datasheet prior to implementing the suggested interface implementations.

Cable Extender Application
The DS15EA101 together with the DS15BA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and field programmable gate arrays (FPGAs) over 100Ω differential (i.e. CAT5e/6/7 and twinax) and 50Ω coaxial cables. Setting correct DS15BA101 output amplitude and proper cable termination are keys for optimal operation. The following two figures show recommended chipset configuration for 100Ω differential and 50Ω coaxial cables.
Reference Design

There is a complete reference design (P/N: DriveCable02EVK) available for evaluation of the cable extender chipset (DS15BA101 and DS15EA101).

For more information visit http://www.ti.com/tool/drivecable02evk
Typical Performance

Maximum Data Rate as a Function of CAT7 (Siemon CAT7 Tera) Length

- **VCC** = 3.3V
- **TA** = 25°C
- NRZ PRBS-7

![Figure 5.](image)

Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

- **VCC** = 3.3V
- **TA** = -40°C
- NRZ PRBS-7

![Figure 6.](image)

Maximum Data Rate as a Function of 50Ω Coaxial (Belden 9914) Length

- **VCC** = 3.3V
- **TA** = 25°C
- NRZ PRBS-7

![Figure 7.](image)

Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 50m CAT5e

- **VCC** = 3.3V
- **TA** = 25°C
- 0.5 UI TIJ@BERT-12
- NRZ PRBS-7

![Figure 8.](image)

Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 75m CAT5e

- **VCC** = 3.3V
- **TA** = 85°C
- 0.5 UI TIJ@BERT-12
- NRZ PRBS-7

![Figure 9.](image)

Residual Jitter as a Function of Data Rate and Temperature for the Chipset with 100m CAT5e

- **VCC** = 3.3V
- **TA** = 85°C
- 0.5 UI TIJ@BERT-12
- NRZ PRBS-7

![Figure 10.](image)
Typical Performance (continued)

A 1.5 Gbps NRZ PRBS-7 After 25m CAT5e

An Equalized 1.5 Gbps NRZ PRBS-7 After 25m CAT5e

A 1.0 Gbps NRZ PRBS-7 After 50m CAT5e

An Equalized 1.0 Gbps NRZ PRBS-7 After 50m CAT5e

A 0.5 Gbps NRZ PRBS-7 After 100m CAT5e

An Equalized 0.5 Gbps NRZ PRBS-7 After 100m CAT5e
Typical Performance (continued)

A 1.5 Gbps NRZ PRBS-7 After 50m CAT7
V:100 mV / DIV, H:100 ps / DIV

An Equalized 1.5 Gbps NRZ PRBS-7 After 50m CAT7
V:100 mV / DIV, H:100 ps / DIV

Figure 17.

Figure 18.

An Equalized 1.5 Gbps NRZ PRBS-7 After 75m CAT7
V:100 mV / DIV, H:100 ps / DIV

A 1.5 Gbps NRZ PRBS-7 After 75m CAT7
V:100 mV / DIV, H:100 ps / DIV

Figure 19.

Figure 20.

A 1.0 Gbps NRZ PRBS-7 After 100m CAT7
V:100 mV / DIV, H:150 ps / DIV

An Equalized 1.0 Gbps NRZ PRBS-7 After 100m CAT7
V:100 mV / DIV, H:150 ps / DIV

Figure 21.

Figure 22.
Typical Performance (continued)

A 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914

V:100 mV / DIV, H:100 ps / DIV

Figure 23.

An Equalized 1.5 Gbps NRZ PRBS-7 After 200m Belden 9914

V:100 mV / DIV, H:100 ps / DIV

Figure 24.
## REVISION HISTORY

### Changes from Revision G (April 2013) to Revision H

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>10</td>
</tr>
</tbody>
</table>

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## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS15EA101SQ/NOPB</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>15EA101</td>
<td></td>
</tr>
<tr>
<td>DS15EA101SQE/NOPB</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>15EA101</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component thickness
- **K0**: Dimension designed to accommodate the component length
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**: Pocket Quadrants
- **Q2**: Sprocket Holes
- **Q3**: User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS15EA101SQ/NOPB</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.3</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>DS15EA101SQE/NOPB</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>250</td>
<td>178.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.3</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS15EA101SQ/NOPB</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>1000</td>
<td>208.0</td>
<td>191.0</td>
<td>35.0</td>
</tr>
<tr>
<td>DS15EA101SQE/NOPB</td>
<td>WQFN</td>
<td>RGH</td>
<td>16</td>
<td>250</td>
<td>208.0</td>
<td>191.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.

⚠️ The package thermal pad must be soldered to the board for thermal and mechanical performance.

See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

⚠️ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
The Pin 1 identifiers are either a molded, marked, or metal feature.

F. Compiles to JEDEC MO-220 variation WQFP-4.
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