1 特性

- 每通道 70mW（典型值）的低功耗，可选择关闭不必要的通道
- 支持无缝链路协商
- 启用主 ASIC，从而在较长的距离上满足前端眼图波形要求
- 高级可配置信号调节 I/O
  - 6GHz 时，接收高达 10dB 的连续时间线性均衡器 (CTLE)
  - 线性输出驱动器
  - 可变输出电压范围高达 1200mVp-p
- 可通过引脚选择 EEPROM 或 SMBus 接口进行编程
- 单电源电压：2.5V 或 3.3V
- -40°C 至 85°C 工作温度范围
- 10mm x 5.5mm 54 引脚超薄型四方扁平无引线（WQFN）封装内的直通引脚分配

2 应用

- 前端口 40G-CR4/SR4/LR4 链路扩展
- 背板 40G-KR4 链路扩展
- SAS/SATA/Pcie 链路扩展
- 其它速率高达 12.5Gbps 的专有高速接口

3 说明

DS125BR820 是一款超低功耗高性能中继器/转接驱动器，专用于支持高速接口速率高达 12.5Gbps 的八个通道，例如 40G-CR4、40G-KR4、SAS/SATA 和 PCIe。接收器的连续时间线性均衡器 (CTLE) 后接一个线性输出驱动器，可在 6GHz (12Gbps) 时提供 3dB 至 10dB 的可编程高频增益功能。CTLE 接收器能够打开一个因果间干扰 (ISI)（由电路板迹线或铜质同轴电缆等互连介质引起）而完全关闭的输入眼图状态。可编程的均衡能够可在互连通道内的实体布局方面实现最大程度的灵活性并提高通道的总体性能。

当在 40G-CR4/KR4、SAS/SATA 和 PCIe 应用中运行时，DS125BR820 保留发射信号特性，从而使得主机控制器和端点能够协商发射均衡器系数。这个链路协商协议的透明管理有助于实现系统级互用性并最大限度缩短延迟。可通过引脚控制、软件（SMBus 或 I2C）来轻松应用相关可编程设置，或者通过 external EEPROM 直接加载设置。在 EEPROM 模式下，配置信息在加电时自动加载，这样就免除了对于外部微控制器或软件驱动程序的需求。

器件信息(1)

<table>
<thead>
<tr>
<th>器件型号</th>
<th>封装</th>
<th>封装尺寸（标称值）</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS125BR820</td>
<td>WQFN (54)</td>
<td>10mm x 5.5mm</td>
</tr>
</tbody>
</table>

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用方框图

![典型应用方框图](image-url)
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4 修订历史记录

Changes from Original (July 2014) to Revision A

- 已添加 完整版文档发布 ...................................................... 1

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5 Pin Configuration and Functions

NOTE: Above 54-lead WQFN graphic is a TOP VIEW, looking down through the package.
<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NUMBER</th>
<th>I/O, TYPE</th>
<th>PIN DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIFFERENTIAL HIGH SPEED I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INB_0+, INB_0-</td>
<td>1, 2</td>
<td>I, LVCMOS</td>
<td>Inverting and non-inverting CML differential inputs to the equalizer.</td>
</tr>
<tr>
<td>INB_1+, INB_1-</td>
<td>3, 4</td>
<td>I, LVCMOS</td>
<td>On-chip 50 Ω termination resistor connects INB_n+ to VDD and INB_n- to VDD</td>
</tr>
<tr>
<td>INB_2+, INB_2-</td>
<td>5, 6</td>
<td>I, LVCMOS</td>
<td>depending on the state of RXDET. See Table 2. AC coupling required on high-speed I/O</td>
</tr>
<tr>
<td>INB_3+, INB_3-</td>
<td>7, 8</td>
<td>I, LVCMOS</td>
<td></td>
</tr>
<tr>
<td>OUTB_0+, OUTB_0-</td>
<td>45, 44</td>
<td>O, OPEN Drain</td>
<td>Inverting and non-inverting 50 Ω driver outputs. Compatible with AC coupled CML inputs. AC coupling required on high-speed I/O</td>
</tr>
<tr>
<td>OUTB_1+, OUTB_1-</td>
<td>43, 42</td>
<td>O, OPEN Drain</td>
<td></td>
</tr>
<tr>
<td>OUTB_2+, OUTB_2-</td>
<td>41, 40</td>
<td>O, OPEN Drain</td>
<td></td>
</tr>
<tr>
<td>INB_3+, INB_3-</td>
<td>39, 38</td>
<td>O, OPEN Drain</td>
<td></td>
</tr>
<tr>
<td>INB_2+, INB_2-</td>
<td>5, 6</td>
<td>I, LVCMOS</td>
<td></td>
</tr>
<tr>
<td>INB_1+, INB_1-</td>
<td>3, 4</td>
<td>I, LVCMOS</td>
<td></td>
</tr>
<tr>
<td>INB_0+, INB_0-</td>
<td>1, 2</td>
<td>I, LVCMOS</td>
<td></td>
</tr>
<tr>
<td>CONTROL PINS — SHARED (LVCMOS)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENSMB</td>
<td>48</td>
<td>I, LVCMOS</td>
<td>System Management Bus (SMBus) Enable Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Tie 1 kΩ to VDD = Register Access SMBus Slave Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FLOAT = Read External EEPROM (SMBus Master Mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Tie 1 kΩ to GND = Pin Mode</td>
</tr>
<tr>
<td>ENSMB = 1 (SMBus SLAVE MODE)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>50</td>
<td>I, LVCMOS, O, OPEN Drain</td>
<td>In SMBus Slave Mode, this pin is the SMBus clock I/O. Clock input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards (2)</td>
</tr>
<tr>
<td>SDA</td>
<td>49</td>
<td>I, LVCMOS, O, OPEN Drain</td>
<td>In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards (2)</td>
</tr>
<tr>
<td>AD0-AD3</td>
<td>54, 53, 47, 46</td>
<td>I, LVCMOS</td>
<td>SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1 kΩ pull-up or pull-down recommended. Note: In Pin Mode, AD2 must be tied via external 1 kΩ to GND.</td>
</tr>
<tr>
<td>RESERVED2</td>
<td>21</td>
<td>I, 4-LEVEL, LVCMOS</td>
<td>Reserved For applications requiring Signal Detect status register read-back:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Leave Pin 21 floating.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Write Reg 0x08[2] = 1 if Pin 21 is floating.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Otherwise, tie Pin 21 via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable).</td>
</tr>
<tr>
<td>RESERVED3</td>
<td>19</td>
<td>I, 4-LEVEL, LVCMOS</td>
<td>Reserved This input may be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND.</td>
</tr>
</tbody>
</table>

(1) LVCMOS inputs without the “Float” conditions must be driven to a logic low or high at all times or operation is not ensured. Input edge rate for LVCMOS/FLOAT inputs must be faster than 50 ns from 10–90%.
For 3.3 V mode operation, VIN pin input = 3.3 V and the logic “1” or “high” reference for the 4-level input is 3.3 V. For 2.5 V mode operation, VDD pin output= 2.5 V and the logic “1” or “high” reference for the 4-level input is 2.5 V.
(2) SCL and SDA pins can be tied either to 3.3 V or 2.5 V, regardless of whether the device is operating in 2.5 V mode or 3.3 V mode.
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NUMBER</th>
<th>I/O, TYPE</th>
<th>PIN DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENSMB = Float (SMBus MASTER MODE)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>50</td>
<td>I, LVCMOS, O, OPEN Drain</td>
<td>Clock output when loading EEPROM configuration, reverting to SMBus clock input when EEPROM load is complete (ALL_DONE = 0). External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards (2).</td>
</tr>
<tr>
<td>SDA</td>
<td>49</td>
<td>I, LVCMOS, O, OPEN Drain</td>
<td>In both SMBus Modes, this pin is the SMBus data I/O. Data input or open drain output. External 2 kΩ to 5 kΩ pull-up resistor to VDD or VIN recommended as per SMBus interface standards (2).</td>
</tr>
<tr>
<td>AD0-AD3</td>
<td>54, 53, 47, 46</td>
<td>I, LVCMOS</td>
<td>SMBus Slave Address Inputs. In both SMBus Modes, these pins are the user set SMBus slave address inputs. External 1 kΩ pull-up or pull-down recommended. Note: In Pin Mode, AD2 must be tied via external 1 kΩ to GND.</td>
</tr>
<tr>
<td>READ_EN</td>
<td>26</td>
<td>I, LVCMOS</td>
<td>A logic low on this pin starts the load from the external EEPROM (3). Once EEPROM load is complete (ALL_DONE = 0), this pin functionality remains as READ_EN. It does not revert to an SD_TH input.</td>
</tr>
</tbody>
</table>
| RESERVED2  | 21         | I, 4-LEVEL, LVCMOS | Reserved For applications requiring Signal Detect status register read-back:  
  ● Leave Pin 21 floating.  
  ● Write Reg 0x08[2] = 1 if Pin 21 is floating. Otherwise, tie Pin 21 via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable). |
| RESERVED3  | 19         | I, 4-LEVEL, LVCMOS | Reserved This input may be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND. |
| ENSMB = 0 (PIN MODE) |
| EQA        | 20         | I, 4-LEVEL, LVCMOS | EQA and EQB pins control the level of equalization for the A-channels and B-channels, respectively. The pins are defined as EQA and EQB only when ENSMB is de-asserted (low). Each of the four A-channels have the same level unless controlled by the SMBus control registers. Likewise, each of the four B-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers independently control each lane, and the EQB pin is converted to an AD3 input. See Table 4. |
| EQB        | 46         | I, 4-LEVEL, LVCMOS |  
| VODB0      | 53         | I, 4-LEVEL, LVCMOS | VODB[1:0] controls the output amplitude of the B-channels. The pins are defined as VODB[1:0] only when ENSMB is de-asserted (low). Each of the four B-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers provide independent control of each lane, and VODB[1:0] pins are converted to AD0, AD1 inputs. See Table 5. |
| VODB1      | 54         | I, 4-LEVEL, LVCMOS |  
| VODA0      | 49         | I, 4-LEVEL, LVCMOS | VODA[1:0] controls the output amplitude of the A-channels. The pins are defined as VODA[1:0] only when ENSMB is de-asserted (low). Each of the four A-channels have the same level unless controlled by the SMBus control registers. When the device operates in Slave or Master Mode, the SMBus registers provide independent control of each lane and the VODA[1:0] pins are converted to SCL and SDA. See Table 5. |
| VODA1      | 50         | I, 4-LEVEL, LVCMOS |  
| AD2        | 47         | I, LVCMOS | Reserved in Pin Mode (ENSMB = 0)  
This input must be tied via external 1 kΩ to GND. |
| SD_TH      | 26         | I, 4-LEVEL, LVCMOS | Controls the internal Signal Detect Status Threshold value when in Pin Mode and SMBus Slave Mode. This pin is to be used for system debugging only. See Table 3 for more information.  
For final designs, input can be left floating, tied via 1 kΩ to VDD, or tied via 1 kΩ to GND. |
| RESERVED2  | 21         | I, 4-LEVEL, LVCMOS | Reserved Tie via external 1 kΩ to GND (External 1 kΩ to VDD is also acceptable). |
| RESERVED3  | 19         | I, 4-LEVEL, LVCMOS | Reserved This input must be tied via external 1 kΩ to GND. |

(3) When READ_EN is low, the device attempts to load EEPROM. If EEPROM cannot be loaded successfully, for example due to an invalid or blank hex file, the DS125BR820 hangs indefinitely in an unknown state. ALL_DONE pin remains high in this situation.
## Pin Functions\(^{(1)}\) (continued)

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NUMBER</th>
<th>I/O, TYPE</th>
<th>PIN DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONTROL PINS — BOTH PIN AND SMBUS MODES (LVCMOS)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RXDET</td>
<td>22</td>
<td>I, 4-LEVEL, LVCMOS</td>
<td>The RXDET pin controls the input enable function. Depending on the input level, a 50 Ω or &gt;50 kΩ termination to the power rail is enabled. Pull up pin to VDD (2.5 V mode) or VIN (3.3 V mode) through 1 kΩ resistor to provide a 50 Ω termination to the power rail for normal operation. See Table 2.</td>
</tr>
<tr>
<td>RESERVED1</td>
<td>23</td>
<td>I, 4-LEVEL, LVCMOS</td>
<td>Reserved This input must be left floating.</td>
</tr>
<tr>
<td>VDD_SEL</td>
<td>25</td>
<td>I, FLOAT</td>
<td>Controls the internal regulator Float = 2.5 V mode Tie to GND = 3.3 V mode</td>
</tr>
<tr>
<td>PWDN</td>
<td>52</td>
<td>I, LVCMOS</td>
<td>Tie High = Low power - Power Down Tie to GND = Normal Operation See Table 2.</td>
</tr>
<tr>
<td>ALL_DONE</td>
<td>27</td>
<td>O, LVCMOS</td>
<td>Valid Register Load Status Output HIGH = External EEPROM load failed or incomplete LOW = External EEPROM load passed</td>
</tr>
<tr>
<td>POWER</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>24</td>
<td>Power</td>
<td>In 3.3 V mode, feed 3.3 V to VIN In 2.5 V mode, leave floating.</td>
</tr>
<tr>
<td>VDD</td>
<td>9, 14, 36, 41, 51</td>
<td>Power</td>
<td>Power Supply for CML and Analog Pins 2.5 V mode, connect to 2.5 V 3.3 V mode, connect 0.1 µF cap to each VDD Pin and GND See Power Supply Recommendations for proper power supply decoupling.</td>
</tr>
<tr>
<td>GND</td>
<td>DAP</td>
<td>Power</td>
<td>Ground pad (DAP - die attach pad).</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VDD to GND, 2.5 V Mode)</td>
<td>-0.5</td>
<td>+2.75</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage (VIN to GND, 3.3 V Mode)</td>
<td>-0.5</td>
<td>+4.0</td>
<td>V</td>
</tr>
<tr>
<td>LVCMOS Input/Output Voltage</td>
<td>-0.5</td>
<td>+4.0</td>
<td>V</td>
</tr>
<tr>
<td>CML Input Voltage</td>
<td>-0.5</td>
<td>VDD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>CML Input Current</td>
<td>-30</td>
<td>+30</td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability, and degradation of device reliability and performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

6.2 Handling Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage temperature range (TAstg)</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature Range Soldering (4 sec.) (T solder)</td>
<td>260</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Electrostatic discharge (V(_{ESD}))</td>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(2)})</td>
<td>-4000</td>
<td>4000</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(3)})</td>
<td>-1000</td>
<td>1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) For soldering specifications: See application note SNOA549.
(2) JEDEC document JEP155 states that 4000-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 1000-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (2.5 V mode)(^{(1)})</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage (3.3 V mode)(^{(1)})</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>SMBus (SDA, SCL)</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Noise up to 50 MHz(^{(2)})</td>
<td>100</td>
<td>mVP-p</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) DC plus AC power should not exceed these limits.
(2) Allowed supply noise (mVP-p sine wave) under typical conditions.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>DS125BR820 WQFN 54 PINS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R(_{JA}) Junction-to-ambient thermal resistance</td>
<td>26.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>R(_{JCtop}) Junction-to-case (top) thermal resistance</td>
<td>10.8</td>
<td></td>
</tr>
<tr>
<td>R(_{JB}) Junction-to-board thermal resistance</td>
<td>4.4</td>
<td></td>
</tr>
<tr>
<td>ψ(_{JT}) Junction-to-top characterization parameter</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>ψ(_{JB}) Junction-to-board characterization parameter</td>
<td>4.3</td>
<td></td>
</tr>
<tr>
<td>R(_{JCbot}) Junction-to-case (bottom) thermal resistance</td>
<td>1.5</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
## 6.5 Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DD} ) Current Consumption, 2.5 V Mode</td>
<td>( EQ = \text{Level 4, VOD = Level 6} ) RXDET = 1, PWDN = 0</td>
<td>220</td>
<td>280</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD} ) Current Consumption, 3.3 V Mode</td>
<td>( EQ = \text{Level 4, VOD = Level 6} ) RXDET = 1, PWDN = 0</td>
<td>220</td>
<td>280</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{DD} ) Power Down Current Consumption</td>
<td>PWDN = 1</td>
<td>14</td>
<td>27</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{DD} ) Integrated LDO Regulator</td>
<td>( V_{IN} = 3.0 \cdot 3.6 \text{ V} )</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td><strong>LVCMOS / LVTTL DC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IH25} ) High Level Input Voltage</td>
<td>2.5 V Supply Mode</td>
<td>1.7</td>
<td></td>
<td>( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH33} ) High Level Input Voltage</td>
<td>3.3 V Supply Mode</td>
<td>1.7</td>
<td></td>
<td>( V_{IN} )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} ) Low Level Input Voltage</td>
<td></td>
<td>0</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} ) High Level Output Voltage (ALL DONE pin)</td>
<td>( I_{OH} = -4 \text{mA} )</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Low Level Output Voltage (ALL DONE pin)</td>
<td>( I_{OL} = 4 \text{mA} )</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{IH} ) Input High Current (PWDN pin)</td>
<td>( V_{IN} = 3.6 \text{ V, LVMOS = 3.6 V} ) ( -15 ) ( +15 ) ( \mu A )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IL} ) Input Low Current (PWDN pin)</td>
<td>( V_{IN} = 3.6 \text{ V, LVMOS = 0 V} ) ( -15 ) ( +15 ) ( \mu A )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>4-LEVEL INPUT DC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IH} ) Input High Current with internal resistors (4–level input pin)</td>
<td>( V_{IN} = 3.6 \text{ V, LVMOS = 3.6 V} ) ( +20 ) ( +150 ) ( \mu A )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IL} ) Input Low Current with internal resistors (4–level input pin)</td>
<td>( V_{IN} = 3.6 \text{ V, LVMOS = 0 V} ) ( -160 ) ( -40 ) ( \mu A )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{TH} ) Voltage Threshold from Pin Mode Level 0 to R</td>
<td>( V_{DD} = 2.5 \text{ V (2.5 V supply mode)} ) Internal LDO Disabled</td>
<td>0.50</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Threshold from Pin Mode Level R to F Internal LDO Disabled</td>
<td>See Table 1 for details</td>
<td>1.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Threshold from Pin Mode Level F to 1</td>
<td></td>
<td>2.00</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Threshold from Pin Mode Level 0 to R Internal LDO Enabled</td>
<td>See Table 1 for details</td>
<td>0.66</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Threshold from Pin Mode Level R to F Internal LDO Enabled</td>
<td>See Table 1 for details</td>
<td>1.65</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Threshold from Pin Mode Level F to 1</td>
<td></td>
<td>2.64</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

### CML RECEIVER INPUTS \( (I_{n+}, I_{n-}) \)

| \( Z_{Rz\text{-DIFF-DC}} \) Rx DC differential mode impedance | Tested at VDD = 2.5 V | 80 | 100 | 120 | \( \Omega \) |
| \( Z_{Rz\text{-DC}} \) Rx DC single ended impedance | Tested at VDD = 2.5 V | 40 | 50 | 60 | \( \Omega \) |
| \( R_{Lz\text{-DIFF}} \) Rx Differential Input return loss | SDD11 10 MHz | -19 | | | dB |
| | SDD11 2 GHz | -14 | | | dB |
| | SDD11 6-11.1 GHz | -8 | | | dB |
| \( R_{Lz\text{-CM}} \) Rx Common mode return loss | SCC11 0.05 - 5 GHz | -10 | | | dB |
| \( V_{Rz\text{-ASSERT-DIFF-PP}} \) Signal detect assert level for active data signal | \( SD_{TH} = F \text{ (float), 1010 pattern at 12 Gbps} \) | 57 | | | mVp-p |
| \( V_{Rz\text{-DEASSERT-DIFF-PP}} \) Signal detect de-assert for inactive signal level | \( SD_{TH} = F \text{ (float), 1010 pattern at 12 Gbps} \) | 44 | | | mVp-p |
## Electrical Characteristics (continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HIGH SPEED OUTPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$RL_{Tx-DIFF}$</td>
<td>Tx Differential return loss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SDD22 10 MHz - 2 GHz</td>
<td>-15</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>SDD22 5.5 GHz</td>
<td>-12</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>SDD22 11.1 GHz</td>
<td>-10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$RL_{Tx-CM}$</td>
<td>Tx Common mode return loss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SCC22 50 MHz - 2.5 GHz</td>
<td>-8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$Z_{Tx-DIFF-DC}$</td>
<td>DC differential Tx impedance</td>
<td>100</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$I_{TX-SHORT}$</td>
<td>Transmitter short circuit current limit</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Total current when output is shorted to VDD or GND</td>
<td></td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{Tx-CM-DC-LINE-DELTA}$</td>
<td>Absolute delta of DC common mode voltage between Tx+ and Tx-</td>
<td></td>
<td></td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{Tx-DIFF1-PP}$</td>
<td>Output Voltage Differential Swing</td>
<td></td>
<td>615</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(^1))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VID = 600 mVp-p, VOD = Level 6(^2)(^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Tx-DIFF2-PP}$</td>
<td>Output Voltage Differential Swing</td>
<td></td>
<td>950</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(^1))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VID = 1000 mVp-p, VOD = Level 6(^2)(^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Tx-DIFF3-PP}$</td>
<td>Output Voltage Differential Swing</td>
<td></td>
<td>1100</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>Differential measurement with OUT_n+ and OUT_n-, AC-Coupled and terminated by 50 Ω to GND, Inputs AC-Coupled, Measured with 8T Pattern at 12 Gbps(^1))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VID = 1200 mVp-p, VOD = Level 6(^2)(^3))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{PDEQ}$</td>
<td>Differential propagation delay</td>
<td></td>
<td>80</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>EQ = Level 1 to Level 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Tx-CM-AC-P}$</td>
<td>AC common mode voltage</td>
<td></td>
<td>20</td>
<td></td>
<td>mV rms</td>
</tr>
<tr>
<td></td>
<td>VOD = Level 6, 12 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DISABLE-OUT}$</td>
<td>Tx disable output voltage</td>
<td></td>
<td>-30</td>
<td>1</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>Driver disabled via PWDN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OOG-OS-DATA}$</td>
<td>OOB idle output voltage</td>
<td></td>
<td>15</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>VID = 0 mVp-p</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OOG-OS-DATA}$</td>
<td>OOB offset delta</td>
<td></td>
<td>15</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>OOB pattern, EQ = Level 1, VOD = Level 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OOG-CM-DATA}$</td>
<td>OOB common mode delta</td>
<td></td>
<td>11</td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td></td>
<td>OOB pattern, EQ = Level 1, VOD = Level 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{TX-IDLE-SET-TO-IDLE}$</td>
<td>Time to transition to idle after differential signal</td>
<td>0.70</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>VID = 1.0 Vp-p, 1.5 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{TX-IDLE-TO-DIFF-DATA}$</td>
<td>Time to transition to valid differential signal after idle</td>
<td>0.04</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>VID = 1.0 Vp-p, 1.5 Gbps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) 8T pattern is defined as a 1111111100000000'b pattern bit sequence.
(2) ATE measurements for production are tested at DC.
(3) In 40G-CR4/KR4/SAS/SATA/PCIe applications, the output VOD level is not fixed. It adjusts automatically based on the VID input amplitude level. The output VOD level set by VODA/B[1:0] depends on the VID level and the frequency content. The DS125BR820 repeater is designed to be transparent in this mode, so the Tx-FIR (de-emphasis) is passed to the Rx to support the handshake negotiation link training.
### Electrical Characteristics (continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJ_{ADD}</td>
<td>Additive Random Jitter</td>
<td>0.36</td>
<td>ps</td>
<td>rms</td>
<td></td>
</tr>
<tr>
<td><strong>EQUALIZATION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DJE1</td>
<td>Residual deterministic jitter at 6 Gbps</td>
<td>0.06</td>
<td>UI</td>
<td>p-p</td>
<td></td>
</tr>
<tr>
<td>DJE2</td>
<td>Residual deterministic jitter at 12 Gbps</td>
<td>0.12</td>
<td>UI</td>
<td>p-p</td>
<td></td>
</tr>
</tbody>
</table>

(4) Additive random jitter is given in RMS value by the following equation: $RJ_{ADD} = \sqrt{(Output \ Jitter)^2 - (Input \ Jitter)^2}$. Typical input jitter for these measurements is 150 fs rms.

#### 6.6 Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SERIAL BUS INTERFACE DC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Data, Clock Input Low Voltage</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Data, Clock Input High Voltage</td>
<td>2.1</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>0</td>
<td>0.36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Nominal Bus Voltage</td>
<td>2.375</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH-Pin}$</td>
<td>Input Leakage Per Device Pin</td>
<td>+20</td>
<td>+150</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{IL-Pin}$</td>
<td>Input Leakage Per Device Pin</td>
<td>-160</td>
<td>-40</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>Capacitance for SDA and SCL</td>
<td>&lt; 5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{TERM}$</td>
<td>External Termination Resistance pull to $V_{DD}$ = 2.5 V ± 5% OR 3.3 V ± 10%</td>
<td>2000</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pullup $V_{DD} = 3.3 \text{ V}^{(1)(2)(3)}$</td>
<td>1000</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Recommended value.
(2) Recommended maximum capacitance load per bus segment is 400 pF.
(3) Maximum termination voltage should be identical to the device supply voltage.

#### 6.7 Timing Requirements Serial Bus Interface

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SERIAL BUS INTERFACE TIMING SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$F_{SMB}$</td>
<td>Bus Operating Frequency</td>
<td>400</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ENSMB = VDD (Slave Mode)</td>
<td>280</td>
<td>400</td>
<td>520</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>ENSMB = FLOAT (Master Mode)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{FALL}$</td>
<td>SCL or SDA Fall Time</td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Read operation $RP_{U} = 4.7 \ \text{kΩ}, \ C_{b} &lt; 50 \ \text{pF}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{RISE}$</td>
<td>SCL or SDA Rise Time</td>
<td>140</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Read operation $RP_{U} = 4.7 \ \text{kΩ}, \ C_{b} &lt; 50 \ \text{pF}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{F}$</td>
<td>Clock/Data Fall Time</td>
<td>300</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{R}$</td>
<td>Clock/Data Rise Time</td>
<td>1000</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{POR}$</td>
<td>Time in which a device must be operational after power-on reset</td>
<td>500</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.
Figure 1. Output Rise And Fall Transition Time

Figure 2. Propagation Delay Timing Diagram

Figure 3. Transmit Idle-Data and Data-Idle Response Time

Figure 4. SMBus Timing Parameters
6.8 Typical Characteristics

![Figure 5. Typical Power Dissipation vs. VOD](image)

**Test Conditions**
EQ Level 4
VOD_DB 000'b
T 25°C

![Figure 6. Typical VOD vs. VDD](image)

**Test Conditions**
Data Rate, Test Pattern 1.5625 Gbps, 1010 Pattern
VOD Level 6
EQ Level 1
T 25°C

![Figure 7. Typical VOD vs. Temperature](image)

**Test Conditions**
Data Rate, Test Pattern 1.5625 Gbps, 1010 Pattern
VOD Level 6
EQ Level 1
VDD 2.5 V

![Figure 8. Typical VOD vs. VID](image)

**Test Conditions**
Data Rate, Test Pattern 1.5625 Gbps, 1010 Pattern
EQ Level 1
T 25°C
VDD 2.5 V
7 Detailed Description

7.1 Overview
The DS125BR820 provides linear equalization for lossy printed circuit board backplanes and balanced cables. The DS125BR820 operates in three modes: Pin Control Mode (ENSMB = 0), SMBus Slave Mode (ENSMB = 1) and SMBus Master Mode (ENSMB = Float) to load register information from external EEPROM.

7.2 Functional Block Diagram
7.2.1 Functional Datapath Blocks

In an increasing number of high speed applications, transparency between Tx and Rx endpoints is essential to ensure high signal integrity. The DS125BR820 channel datapath uses one input gain stage equalization coupled with a linear driver. This combination provides a high level of transparency, thereby achieving greater drive distance in applications such as 40G-CR4, 40G-KR4, SAS, SATA, and PCIe that require Rx-Tx auto-negotiation and link-training. Refer to the Typical Applications section for more application information regarding recommended settings and placement.

7.3 Feature Description

The 4-level input pins use a resistor divider to help set the four valid control levels and provide a wider range of control settings when ENSMB = 0. There is an internal 30 kΩ pull-up and a 60 kΩ pull-down connected to the package pin. These resistors, together with the external resistor connection, combine to achieve the desired voltage level. By using the 1 kΩ pull-down, 20 kΩ pull-down, no connect, and 1 kΩ pull-up, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

### Table 1. 4–Level Control Pin Settings

<table>
<thead>
<tr>
<th>Level</th>
<th>Setting</th>
<th>Resulting Pin Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Tie 1 kΩ to GND</td>
<td>0.10 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.08 V</td>
</tr>
<tr>
<td>R</td>
<td>Tie 20 kΩ to GND</td>
<td>1/3 x V_IN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1/3 x V_DD</td>
</tr>
<tr>
<td>F</td>
<td>Float (leave pin open)</td>
<td>2/3 x V_IN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2/3 x V_DD</td>
</tr>
<tr>
<td>1</td>
<td>Tie 1 kΩ to V_IN or V_DD</td>
<td>V_IN - 0.05 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD - 0.04 V</td>
</tr>
</tbody>
</table>

Typical 4-Level Input Thresholds

- Internal Threshold between 0 and R = 0.2 * V_IN or V_DD
- Internal Threshold between R and F = 0.5 * V_IN or V_DD
- Internal Threshold between F and 1 = 0.8 * V_IN or V_DD

In order to minimize the startup current associated with the integrated 2.5 V regulator, the 1 kΩ pull-up / pull-down resistors are recommended. If several four level inputs require the same setting, it is possible to combine two or more 1 kΩ resistors into a single lower value resistor. As an example, combining two inputs with a single 500 Ω resistor is a valid way to save board space.

7.4 Device Functional Modes

7.4.1 Pin Control Mode:

When in Pin Mode (ENSMB = 0), equalization and VOD (output amplitude) can be selected via pin control for both the A-channels and B-channels per Table 4. The RXDET pin provides either automatic or manual control for input termination (50 Ω or > 50 kΩ to VDD). The receiver electrical signal detect status threshold is adjustable via the SD_TH pin. By setting signal-detect threshold level via the SD_TH pin, status information about a valid signal detect assert/de-assert can be read back via SMBus registers. Pin control mode is ideal in situations where neither MCU or EEPROM is available to access the device via SMBus SDA/SCL lines.

7.4.2 Slave SMBus Mode:

When in Slave SMBus Mode (ENSMB = 1), the VOD (output amplitude), equalization, and termination disable features are all programmable on an individual channel basis, rather than in collective A-channel and B-channel groups. Upon assertion of ENSMB, the EQx and VODx settings are controlled by SMBus immediately. It is important to note that SMBus settings can only be changed from their defaults after asserting Register Enable by setting Reg 0x06[3] = 1. The EQx and VODx pins are subsequently converted to AD0-AD3 SMBus address inputs. The other external control pins (RXDET and SD_TH) remain active unless their respective registers are written to and the appropriate override bit is set. If the user overrides a pin control, the input voltage level of that control pin is ignored until ENSMB is driven low (Pin Mode). In the event that channels are powered down via the PWDN pin, the state of all register settings are not affected.
## Device Functional Modes (continued)

### Table 2. Rx Detect Settings

<table>
<thead>
<tr>
<th>PWDN (^{(1)}) (Pin 52)</th>
<th>RXDET (^{(1)}) (Pin 22)</th>
<th>SMBus REG Bit[3:2]</th>
<th>INPUT TERMINATION</th>
<th>RECOMMENDED USE</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>00</td>
<td>Hi-Z</td>
<td>Manual Rx-Detect, input is Hi-Z</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>R</td>
<td>01</td>
<td>Pre Detect: Hi-Z Post Detect: 50 Ω</td>
<td>PCIe Only</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>F (Default)</td>
<td>10</td>
<td>Pre Detect: Hi-Z Post Detect: 50 Ω</td>
<td>PCIe Only</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Hi-Z</td>
<td>Power Down mode, input is Hi-Z, output drivers are disabled Used to reset Rx-Detect State Machine when held high for 5 µs</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) In SMBus Slave Mode, the Rx Detect State Machine can be manually reset in software by overriding the device PRSNT function. This is accomplished by setting the Override PRSNT bit (Reg 0x02[7]) and then toggling the PRSNT value bit (Reg 0x02[6]). See Table 9 for more information about resetting the Rx Detect State Machine.

### Table 3. Signal Detect Status Threshold Level\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Level</th>
<th>SD_TH (^{(1)}) (Pin 26)</th>
<th>SMBus REG BIT[3:2] (^{(1)}) and[1:0]</th>
<th>[3:2] ASSERT LEVEL (^{(1)}) (mVp-p)</th>
<th>[1:0] DE-ASSERT LEVEL (^{(1)}) (mVp-p)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>10</td>
<td>18</td>
<td>75</td>
</tr>
<tr>
<td>2</td>
<td>R</td>
<td>01</td>
<td>12</td>
<td>40</td>
</tr>
<tr>
<td>3</td>
<td>F (default)</td>
<td>00</td>
<td>15</td>
<td>50</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>11</td>
<td>16</td>
<td>58</td>
</tr>
</tbody>
</table>

\(^{(1)}\) VDD = 2.5 V, 25°C, 11 00 11 00 pattern at 3 Gbps and 101010 pattern at 12 Gbps

\(^{(2)}\) Signal detect status thresholds set the value at which a signal detect status is flagged via SMBus Reg 0x0A. Regardless of the threshold level, the output always remains enabled unless manually powered down.

### 7.4.3 SMBus Master Mode

When in SMBus Master Mode (ENSMB = Float), the VOD (output amplitude), equalization, and termination disable features for multiple devices can be loaded via external EEPROM. By asserting a Float condition on the ENSMB pin, an external EEPROM writes register settings to each device in accordance with its SMBus slave address. The settings programmable by external EEPROM provide only a subset of all the register bits available via SMBus Slave Mode, and the bit-mapping between SMBus Slave Mode registers and Master SMBus registers can be referenced in Table 6. Once the EEPROM successfully finishes loading each device's register settings, the device reverts back to SMBus Slave Mode and releases SDA/SCL control to an external master MCU. If the EEPROM fails to load settings to a particular device, for example due to an invalid or blank hex file, a time-out occurs and the device hangs in an unknown state.

### 7.5 Signal Conditioning Settings

Equalization and VOD settings accessible via the pin controls are chosen to meet the needs of most high speed applications. These settings can also be controlled via the SMBus registers. Each pin input has a total of four possible voltage level settings. Table 4 and Table 5 show both the Pin Mode and SMBus Mode settings that are used in order to program the equalization and VOD gain for each DS125BR820 channel.
### Signal Conditioning Settings (continued)

#### Table 4. Equalizer Settings\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Level</th>
<th>EQA(^{(3)})</th>
<th>EQB</th>
<th>dB at 1.5 GHz</th>
<th>dB at 2.5 GHz</th>
<th>dB at 4 GHz</th>
<th>dB at 5 GHz</th>
<th>dB at 6 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>xxxx xx00 = 0x00</td>
<td>2.1</td>
<td>2.5</td>
<td>2.7</td>
<td>2.9</td>
<td>3.0</td>
</tr>
<tr>
<td>2</td>
<td>R (\text{reserved} = 0x01)</td>
<td>4.0</td>
<td>5.1</td>
<td>6.4</td>
<td>6.8</td>
<td>7.4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>F (\text{reserved} = 0x02)</td>
<td>5.5</td>
<td>7.0</td>
<td>8.3</td>
<td>8.6</td>
<td>8.9</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>xxxx xx11 = 0x03</td>
<td>6.8</td>
<td>8.3</td>
<td>9.5</td>
<td>9.6</td>
<td>9.8</td>
</tr>
</tbody>
</table>

(1) Optimal EQ setting should be determined via simulation and prototype verification.
(2) Equalization boost values are inclusive of package loss.
(3) To program EQ Level 1-4 correctly in Pin Mode, RESERVED3 and AD2 pins must be tied via 1 k\(\Omega\) resistor to GND.

#### Table 5. Output Voltage Settings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Level</th>
<th>VODA1</th>
<th>VODA0</th>
<th>VODA - 3 bits([2:0])</th>
<th>VOD_DB - 3 bits([2:0])</th>
<th>VID Vp-p</th>
<th>VOD/VID Ratio(^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>000'b</td>
<td>000'b</td>
<td>1.2</td>
<td>0.57(^{(2)})</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>R</td>
<td>010'b</td>
<td>000'b</td>
<td>1.2</td>
<td>0.71</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>011'b</td>
<td>000'b</td>
<td>1.2</td>
<td>0.77</td>
</tr>
<tr>
<td>4</td>
<td>R</td>
<td>F</td>
<td>100'b</td>
<td>000'b</td>
<td>1.2</td>
<td>0.83</td>
</tr>
<tr>
<td>5</td>
<td>F</td>
<td>R</td>
<td>101'b</td>
<td>000'b</td>
<td>1.2</td>
<td>0.90</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>0</td>
<td>110'b</td>
<td>000'b</td>
<td>1.2</td>
<td>1.00</td>
</tr>
<tr>
<td>--</td>
<td>--</td>
<td>--</td>
<td>111'b</td>
<td>000'b</td>
<td>1.2</td>
<td>1.04(^{(2)(3)})</td>
</tr>
</tbody>
</table>

(1) For 40G-CR4/KR4/SAS/SATA/PCIe operation, it is important to keep the output amplitude and dynamic range as large as possible. When operating in Pin Mode, it is recommended to use VODA\([1:0]\) = VODB\([1:0]\) = Level 6. In SMBus Mode, it is also recommended to use Level 6 (that is, VOD = 110'b and VOD_DB = 000'b).
(2) These VOD settings are only accessible via SMBus Modes.
(3) VOD = 111'b setting in SMBus Mode is not recommended.
7.6 Programming

The DS125BR820 device supports reading directly from an external EEPROM device by implementing SMBus Master Mode. When using SMBus Master Mode, the DS125BR820 reads directly from specific location in the external EEPROM. When designing a system for using the external EEPROM, the user must follow these specific guidelines.

- Maximum EEPROM size is 8K (1024 x 8-bit).
- Set ENSMB = Float — enable the SMBus Master Mode.
- The external EEPROM device address byte must be 0xA0 and capable of 1 MHz operation at 2.5 V and 3.3 V supply.
- Set the AD[3:0] inputs for SMBus address byte. When the AD[3:0] = 0000'b, the device address byte is 0xB0.

When tying multiple DS125BR820 devices to the SDA and SCL bus, use these guidelines to configure the devices:

- Use SMBus AD[3:0] address bits so that each device can load its configuration from the EEPROM. Example below is for four devices. The first device in the sequence is conventionally address 0xB0, while subsequent devices follow the address order listed below.
  - U1: AD[3:0] = 0000 = 0xB0,
  - U2: AD[3:0] = 0001 = 0xB2,
  - U3: AD[3:0] = 0010 = 0xB4,
  - U4: AD[3:0] = 0011 = 0xB6

- Use a pull-up resistor on SDA and SCL; value = 2 kΩ to 5 kΩ
- Daisy-chain READ_EN (Pin 26) and ALL_DONE (Pin 27) from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.
  1. Tie READ_EN of the first device in the chain (U1) to GND.
  2. Tie ALL_DONE of U1 to READ_EN of U2.
  3. Tie ALL_DONE of U2 to READ_EN of U3.
  4. Tie ALL_DONE of U3 to READ_EN of U4.
  5. Optional: Tie ALL_DONE output of U4 to a LED to show the devices have been loaded successfully.

Once the ALL_DONE status pin of the last device is flagged to indicate that all devices sharing the SMBus line have been successfully programmed, control of the SMBus line is released by the repeater and the device reverts back to SMBus Slave Mode. At this point, an external MCU can perform any additional Read or Write operations.

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for the DS125BR820 device. The first three bytes of the EEPROM always contain a base header common and necessary to control initialization of all devices connected to the I2C bus. The CRC enable flag is used to enable or disable CRC checking. If CRC checking is disabled, a fixed pattern (8’hA5) is written/read instead of the CRC byte from the CRC location to simplify the control. There is a MAP bit to flag the presence of an address map that specifies the configuration data start address in the EEPROM. If the MAP bit is not present, the configuration data start address is assumed to follow the base header directly. Lastly, one bit in the base header is used to indicate whether EEPROM size > 256 bytes. This bit ensures that EEPROM slot addresses are formatted properly as one byte (EEPROM ≤ 256 bytes) or two bytes (EEPROM > 256 bytes) for subsequent address map headers. There are 37 bytes of data for each DS125BR820 device.

Note: The maximum EEPROM size supported is 8 kbits (1024 x 8 bits).

7.6.1 EEPROM Register Map for Single Device

A detailed EEPROM Register Map for a single device is shown in Table 6. For instances where multiple devices are written to EEPROM, the device starting address definitions align starting with Table 6 Byte 0x03.
<table>
<thead>
<tr>
<th>EEPROM Address Byte</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>0x01</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>0x03</td>
<td>PWDN_CH7</td>
<td>PWDN_CH6</td>
<td>PWDN_CH5</td>
<td>PWDN_CH4</td>
<td>PWDN_CH3</td>
<td>PWDN_CH2</td>
<td>PWDN_CH1</td>
</tr>
<tr>
<td>SMBus Register</td>
<td>0x01[7]</td>
<td>0x01[6]</td>
<td>0x01[5]</td>
<td>0x01[4]</td>
<td>0x01[3]</td>
<td>0x01[2]</td>
<td>0x01[1]</td>
<td>0x01[0]</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>0x04</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Ovrd_PWDN</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>0x05</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Ovrd_SD_TH</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x04</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>0x06</td>
<td>Reserved</td>
<td>Ovrd_RXDET</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x07</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<td>Description</td>
<td>0x07</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CH0_RXDET_1</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>Description</td>
<td>0x08</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CH0_EQ_1</td>
</tr>
<tr>
<td>SMBus Register</td>
<td>0x0F[7]</td>
<td>0x0F[6]</td>
<td>0x0F[5]</td>
<td>0x0F[4]</td>
<td>0x0F[3]</td>
<td>0x0F[2]</td>
<td>0x0F[1]</td>
<td>0x0F[0]</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x2F</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>EEPROM Address Byte</td>
<td>Bit 7</td>
<td>Bit 6</td>
<td>Bit 5</td>
<td>Bit 4</td>
<td>Bit 3</td>
<td>Bit 2</td>
<td>Bit 1</td>
<td>Bit 0</td>
</tr>
<tr>
<td>---------------------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>Description</td>
<td>CH0_SCP</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CH0_VOD_2</td>
<td>CH0_VOD_1</td>
<td>CH0_VOD_0</td>
<td></td>
</tr>
<tr>
<td>Default Value</td>
<td>0xAD</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>Description</td>
<td>CH0_VOD_DB_2</td>
<td>CH0_VOD_DB_1</td>
<td>CH0_VOD_DB_0</td>
<td>Reserved</td>
<td>CH0_THa_1</td>
<td>CH0_THa_0</td>
<td>CH0_THd_1</td>
<td>CH0_THd_0</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x40</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>CH1_RXDET_1</td>
<td>CH1_RXDET_0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default Value</td>
<td>0x02</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>CH1_EQ_1</td>
<td>CH1_EQ_0</td>
<td>CH1_SCP</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
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<td>Default Value</td>
<td>0xFA</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>CH1_VOD_DB_2</td>
<td>CH1_VOD_DB_1</td>
<td>CH1_VOD_DB_0</td>
<td>CH1_VOD_DB_2</td>
<td>CH1_VOD_DB_1</td>
<td>CH1_VOD_DB_0</td>
<td>Reserved</td>
<td></td>
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<tr>
<td>SMBus Register</td>
<td>0x0D</td>
<td>0x17[3]</td>
<td>0x17[2]</td>
<td>0x17[1]</td>
<td>0x17[0]</td>
<td>0x18[2]</td>
<td>0x18[1]</td>
<td>0x18[0]</td>
</tr>
<tr>
<td>Default Value</td>
<td>0xD4</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Description</td>
<td>CH2_RXDET_1</td>
<td>CH2_RXDET_0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CH2_THa_1</td>
<td>CH2_THa_0</td>
<td>CH2_THd_1</td>
<td>CH2_THd_0</td>
</tr>
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<td>0x0E</td>
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<td>Bit 3</td>
<td>Bit 2</td>
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<td>CH3_THd_0</td>
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<td>hi_idle_SD_CH4-7</td>
<td>fast_SD_CH0-3</td>
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<td>lo_gain_SD_CH0-3</td>
<td>lo_gain_SD_CH4-7</td>
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<td>Reserved</td>
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<td>CH4_RXDET_0</td>
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<td>Reserved</td>
<td>Reserved</td>
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<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CH4_VOD_2</td>
<td>CH4_VOD_1</td>
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</table>

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Table 6. EEPROM Register Map - Single Device With Default Value (continued)

<table>
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<tr>
<th>EEPROM Address Byte</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>CH4_VOD_DB_1</td>
<td>CH4_VOD_DB_0</td>
<td>Reserved</td>
<td>CH4_THa_1</td>
<td>CH4_THa_0</td>
<td>CH4_THd_1</td>
<td>CH4_THd_0</td>
<td>Reserved</td>
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<td>SMBus Register 0x19</td>
<td>0x2E[1]</td>
<td>0x2E[0]</td>
<td>0x2F[7]</td>
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<td>0x2F[2]</td>
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<td>CH5_RXDET_0</td>
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<td>CH5_EQ_1</td>
<td>CH5_EQ_0</td>
<td>CH5_SCP</td>
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<td>CH5_VOD_DB_2</td>
<td>CH5_VOD_DB_1</td>
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<td>CH5_THa_1</td>
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<td>0x35[2]</td>
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<td>CH6_RXDET_1</td>
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<td>Reserved</td>
<td>Reserved</td>
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Table 6. EEPROM Register Map - Single Device With Default Value (continued)

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<th>EEPROM Address Byte</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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<td>CH7_RXDET_1</td>
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<td>CH7_VOD_DB_1</td>
<td>CH7_VOD_DB_0</td>
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### Table 7. Example Of EEPROM For Four Devices Using Two Address Maps

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<th>Address (Hex)</th>
<th>EEPROM Data</th>
<th>Comments</th>
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</thead>
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<tr>
<td>0</td>
<td>00</td>
<td>0x43</td>
<td>CRC_EN = 0, Address Map = 1, &gt;256 bytes = 0, Device Count[3:0] = 3</td>
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<tr>
<td>1</td>
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</tr>
<tr>
<td>2</td>
<td>02</td>
<td>0x10</td>
<td>EEPROM Burst Size</td>
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<td>03</td>
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<td>CRC not used</td>
</tr>
<tr>
<td>4</td>
<td>04</td>
<td>0x0B</td>
<td>Device 0 Address Location</td>
</tr>
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<td>05</td>
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<td>CRC not used</td>
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<td>6</td>
<td>06</td>
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<td>Device 1 Address Location</td>
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<td>CRC not used</td>
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<td>Device 2 Address Location</td>
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<td>CRC not used</td>
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<td>0A</td>
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<td>Device 3 Address Location</td>
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<td>Begin Device 0, 1 - Address Offset 3</td>
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<td>17</td>
<td>11</td>
<td>0xAD</td>
<td>VOD CHB0 = 101'b</td>
</tr>
<tr>
<td>18</td>
<td>12</td>
<td>0x00</td>
<td>VOD_DB CHB0 = 000'b</td>
</tr>
<tr>
<td>19</td>
<td>13</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>14</td>
<td>0x1A</td>
<td>EQ CHB1 = 0x01</td>
</tr>
<tr>
<td>21</td>
<td>15</td>
<td>0xD0</td>
<td>VOD CHB1 = 101'b, VOD_DB CHB1 = 000'b</td>
</tr>
<tr>
<td>22</td>
<td>16</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>17</td>
<td>0x01</td>
<td>EQ CHB2 = 0x01</td>
</tr>
<tr>
<td>24</td>
<td>18</td>
<td>0xAD</td>
<td>VOD CHB2 = 101'b</td>
</tr>
<tr>
<td>25</td>
<td>19</td>
<td>0x00</td>
<td>VOD_DB CHB2 = 000'b</td>
</tr>
<tr>
<td>26</td>
<td>1A</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>1B</td>
<td>0x1A</td>
<td>EQ CHB3 = 0x01</td>
</tr>
<tr>
<td>28</td>
<td>1C</td>
<td>0xD0</td>
<td>VOD CHB3 = 101'b, VOD_DB CHB3 = 000'b</td>
</tr>
<tr>
<td>29</td>
<td>1D</td>
<td>0x09</td>
<td>Signal Detect Status Threshold Control</td>
</tr>
<tr>
<td>30</td>
<td>1E</td>
<td>0x80</td>
<td>Signal Detect Status Threshold Control</td>
</tr>
<tr>
<td>31</td>
<td>1F</td>
<td>0x07</td>
<td>EQ CHA0 = 0x03</td>
</tr>
<tr>
<td>32</td>
<td>20</td>
<td>0x5C</td>
<td>VOD CHA0 = 110'b</td>
</tr>
<tr>
<td>33</td>
<td>21</td>
<td>0x00</td>
<td>VOD_DB CHA0 = 000'b</td>
</tr>
<tr>
<td>34</td>
<td>22</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>23</td>
<td>0x15</td>
<td>EQ CHA1 = 0x00</td>
</tr>
<tr>
<td>36</td>
<td>24</td>
<td>0xC0</td>
<td>VOD CHA1 = 110'b, VOD_DB CHA1 = 000'b</td>
</tr>
<tr>
<td>37</td>
<td>25</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>26</td>
<td>0x07</td>
<td>EQ CHA2 = 0x03</td>
</tr>
<tr>
<td>39</td>
<td>27</td>
<td>0x5C</td>
<td>VOD CHA2 = 110'b</td>
</tr>
<tr>
<td>40</td>
<td>28</td>
<td>0x00</td>
<td>VOD_DB CHA2 = 000'b</td>
</tr>
<tr>
<td>41</td>
<td>29</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>2A</td>
<td>0x75</td>
<td>EQ CHA3 = 0x00</td>
</tr>
<tr>
<td>43</td>
<td>2B</td>
<td>0xC0</td>
<td>VOD CHA3 = 110'b, VOD_DB CHA3 = 000'b</td>
</tr>
<tr>
<td>44</td>
<td>2C</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>2D</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>2E</td>
<td>0x54</td>
<td></td>
</tr>
</tbody>
</table>
Table 7. Example Of EEPROM For Four Devices Using Two Address Maps (continued)

<table>
<thead>
<tr>
<th>EEPROM Address</th>
<th>Address (Hex)</th>
<th>EEPROM Data</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>47</td>
<td>2F</td>
<td>0x54</td>
<td>End Device 0, 1 - Address Offset 39</td>
</tr>
<tr>
<td>48</td>
<td>30</td>
<td>0x00</td>
<td>Begin Device 2, 3 - Address Offset 3</td>
</tr>
<tr>
<td>49</td>
<td>31</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>32</td>
<td>0x04</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>33</td>
<td>0x07</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>34</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>35</td>
<td>0x01</td>
<td>EQ CHB0 = 0x01</td>
</tr>
<tr>
<td>54</td>
<td>36</td>
<td>0xAB</td>
<td>VOD CHB0 = 011'b</td>
</tr>
<tr>
<td>55</td>
<td>37</td>
<td>0x00</td>
<td>VOD_DB CHB0 = 000'b</td>
</tr>
<tr>
<td>56</td>
<td>38</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>39</td>
<td>0x1A</td>
<td>EQ CHB1 = 0x01</td>
</tr>
<tr>
<td>58</td>
<td>3A</td>
<td>0xB0</td>
<td>VOD CHB1 = 011'b, VOD_DB CHB1 = 000'b</td>
</tr>
<tr>
<td>59</td>
<td>3B</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>3C</td>
<td>0x01</td>
<td>EQ CHB2 = 0x01</td>
</tr>
<tr>
<td>61</td>
<td>3D</td>
<td>0xAB</td>
<td>VOD CHB2 = 011'b</td>
</tr>
<tr>
<td>62</td>
<td>3E</td>
<td>0x00</td>
<td>VOD_DB CHB2 = 000'b</td>
</tr>
<tr>
<td>63</td>
<td>3F</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>40</td>
<td>0x1A</td>
<td>EQ CHB3 = 0x01</td>
</tr>
<tr>
<td>65</td>
<td>41</td>
<td>0xB0</td>
<td>VOD CHB3 = 011'b, VOD_DB CHB3 = 000'b</td>
</tr>
<tr>
<td>66</td>
<td>42</td>
<td>0x09</td>
<td>Signal Detect Status Threshold Control</td>
</tr>
<tr>
<td>67</td>
<td>43</td>
<td>0x80</td>
<td>Signal Detect Status Threshold Control</td>
</tr>
<tr>
<td>68</td>
<td>44</td>
<td>0x07</td>
<td>EQ CHA0 = 0x03</td>
</tr>
<tr>
<td>69</td>
<td>45</td>
<td>0x5C</td>
<td>VOD CHA0 = 110'b</td>
</tr>
<tr>
<td>70</td>
<td>46</td>
<td>0x00</td>
<td>VOD_DB CHA0 = 000'b</td>
</tr>
<tr>
<td>71</td>
<td>47</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>48</td>
<td>0x15</td>
<td>EQ CHA1 = 0x00</td>
</tr>
<tr>
<td>73</td>
<td>49</td>
<td>0xA0</td>
<td>VOD CHA1 = 101'b, VOD_DB CHA1 = 000'b</td>
</tr>
<tr>
<td>74</td>
<td>4A</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>4B</td>
<td>0x07</td>
<td>EQ CHA2 = 0x03</td>
</tr>
<tr>
<td>76</td>
<td>4C</td>
<td>0x5C</td>
<td>VOD CHA2 = 110'b</td>
</tr>
<tr>
<td>77</td>
<td>4D</td>
<td>0x00</td>
<td>VOD_DB CHA2 = 000'b</td>
</tr>
<tr>
<td>78</td>
<td>4E</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>4F</td>
<td>0x15</td>
<td>EQ CHA3 = 0x00</td>
</tr>
<tr>
<td>80</td>
<td>50</td>
<td>0xA0</td>
<td>VOD CHA3 = 101'b, VOD_DB CHA3 = 000'b</td>
</tr>
<tr>
<td>81</td>
<td>51</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>82</td>
<td>52</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>83</td>
<td>53</td>
<td>0x54</td>
<td></td>
</tr>
<tr>
<td>84</td>
<td>54</td>
<td>0x54</td>
<td>End Device 2, 3 - Address Offset 39</td>
</tr>
</tbody>
</table>

Note: CRC_EN = 0, Address Map = 1, >256 byte = 0, Device Count[3:0] = 3. Multiple devices can point to the same address map. Maximum EEPROM size is 8 kbits (1024 x 8-bits).
7.7 Register Maps

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. Tie EN_SMB = 1 kΩ to VDD (2.5 V mode) or VIN (3.3 V mode) to enable SMBus Slave Mode and allow access to the configuration registers.

The DS125BR820 uses AD[3:0] inputs in both SMBus Modes. These AD[3:0] pins are the user set SMBus slave address inputs and have internal pull-downs. Based on the SMBus 2.0 specification, the DS125BR820 has a 7-bit slave address. The LSB is set to 0'b (for a WRITE). When AD[3:0] pins are left floating or pulled low, AD[3:0] = 0000'b, and the device default address byte is 0xB0. The device supports up to 16 address bytes, as shown in Table 8:

<table>
<thead>
<tr>
<th>AD[3:0] Settings</th>
<th>Full Slave Address Byte (7-Bit Address + Write Bit)</th>
<th>7-Bit Slave Address (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>B0</td>
<td>58</td>
</tr>
<tr>
<td>0001</td>
<td>B2</td>
<td>59</td>
</tr>
<tr>
<td>0010</td>
<td>B4</td>
<td>5A</td>
</tr>
<tr>
<td>0011</td>
<td>B6</td>
<td>5B</td>
</tr>
<tr>
<td>0100</td>
<td>B8</td>
<td>5C</td>
</tr>
<tr>
<td>0101</td>
<td>BA</td>
<td>5D</td>
</tr>
<tr>
<td>0110</td>
<td>BC</td>
<td>5E</td>
</tr>
<tr>
<td>0111</td>
<td>BE</td>
<td>5F</td>
</tr>
<tr>
<td>1000</td>
<td>C0</td>
<td>60</td>
</tr>
<tr>
<td>1001</td>
<td>C2</td>
<td>61</td>
</tr>
<tr>
<td>1010</td>
<td>C4</td>
<td>62</td>
</tr>
<tr>
<td>1011</td>
<td>C6</td>
<td>63</td>
</tr>
<tr>
<td>1100</td>
<td>C8</td>
<td>64</td>
</tr>
<tr>
<td>1101</td>
<td>CA</td>
<td>65</td>
</tr>
<tr>
<td>1110</td>
<td>CC</td>
<td>66</td>
</tr>
<tr>
<td>1111</td>
<td>CE</td>
<td>67</td>
</tr>
</tbody>
</table>

The SDA/SCL pins are 3.3 V tolerant, but are not 5V tolerant. An external pull-up resistor is required on the SDA line. The resistor value can be from 2 kΩ to 5 kΩ depending on the voltage, loading and speed. The SCL may also require an external pull-up resistor and it depends on the Host that drives the bus.

7.7.1 Transfer Of Data Via The SMBus

During normal operation, the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH}, then the bus transfers to the IDLE state.

7.7.2 SMBus Transactions

The device supports WRITE and READ transactions. See Table 9 for register address, type (Read/Write, Read Only), default value, and function information.
7.7.3 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).
1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drive the 8-bit data byte.
6. The Device drives an ACK bit (“0”).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE, and communication with other SMBus devices may now occur.

7.7.4 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).
1. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The Device (Slave) drives the ACK bit (“0”).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (“0”).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The Device drives an ACK bit “0”.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit “1” indicating end of the READ transfer.
10. The Host drives a STOP condition.

The READ transaction is completed, the bus goes IDLE, and communication with other SMBus devices may now occur.
### Table 9. SMBus Slave Mode Register Map

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Observation</td>
<td>7</td>
<td>Reserved</td>
<td>R/W</td>
<td>Set bit to 0</td>
<td>Observation of AD[3:0] bits [6]: AD3 [5]: AD2 [4]: AD1 [3]: AD0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:3</td>
<td>Address Bit AD[3:0]</td>
<td>R</td>
<td>0x00</td>
<td>Power Down per Channel [7]: CH7 – CHA_3 [6]: CH6 – CHA_2 [5]: CH5 – CHA_1 [4]: CH4 – CHA_0 [3]: CH3 – CHB_3 [2]: CH2 – CHB_2 [1]: CH1 – CHB_1 [0]: CH0 – CHB_0 0x00 = all channels enabled 0xFF = all channels disabled Note: Override PWDN pin and enable register control via Reg 0x02[0]</td>
</tr>
<tr>
<td>0x01</td>
<td>PWDN Channels</td>
<td>7:0</td>
<td>PWDN CHx</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override PWDN, PRSNT 1 = Override Automatic Rx Detect State Machine Reset 1 = Set Rx Detect State Machine Reset 0 = Clear Rx Detect State Machine Reset Set bits to 0 Set bit to 0 Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5:2</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override PWDN Pin Control 1 = Block PWDN pin control (Register control enabled) 0 = Allow PWDN pin control (Register control disabled) Set bits to 0</td>
</tr>
<tr>
<td>0x03</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Slave Register Control 1 = Enable SMBus Slave Mode Register Control Note: In order to change VOD, VOD_DB, and EQ of the channels in slave mode, this bit must be set to 1. Set bits to 0 Set bit to 1</td>
</tr>
<tr>
<td>0x04</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Slave Register Control 1 = Enable SMBus Slave Mode Register Control Note: In order to change VOD, VOD_DB, and EQ of the channels in slave mode, this bit must be set to 1. Set bits to 0 Set bit to 1</td>
</tr>
<tr>
<td>0x05</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Slave Register Control 1 = Enable SMBus Slave Mode Register Control Note: In order to change VOD, VOD_DB, and EQ of the channels in slave mode, this bit must be set to 1. Set bits to 0 Set bit to 1</td>
</tr>
<tr>
<td>0x06</td>
<td>Digital Reset</td>
<td>7</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x01 Yes</td>
<td>Digital Reset and Control 1 = Self clearing reset for SMBus registers (register settings return to default values) 1 = Self clearing reset to SMBus master state machine Set bits to 0 0001'b</td>
</tr>
<tr>
<td></td>
<td>and Control</td>
<td>6</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x01 Yes</td>
<td>Digital Reset and Control 1 = Self clearing reset for SMBus registers (register settings return to default values) 1 = Self clearing reset to SMBus master state machine Set bits to 0 0001'b</td>
</tr>
<tr>
<td>0x07</td>
<td>Override SD_TH</td>
<td>6</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override Pin Control 1 = Block SD_TH pin control (Register control enabled) 0 = Allow SD_TH pin control (Register control disabled) Set bits to 0 Set bit to 0</td>
</tr>
<tr>
<td></td>
<td>RXDET</td>
<td>5:4</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override Pin Control 1 = Block SD_TH pin control (Register control enabled) 0 = Allow SD_TH pin control (Register control disabled) Set bits to 0 Set bit to 0</td>
</tr>
<tr>
<td></td>
<td>Reserved</td>
<td>3</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override Pin Control 1 = Block RXDET pin control (Register control enabled) 0 = Allow RXDET pin control (Register control disabled) Set bits to 0 Set bit to 0</td>
</tr>
<tr>
<td></td>
<td>Reserved</td>
<td>2</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00 Yes</td>
<td>Override Pin Control 1 = Block RXDET pin control (Register control enabled) 0 = Allow RXDET pin control (Register control disabled) Set bits to 0 Set bit to 0</td>
</tr>
<tr>
<td>Address</td>
<td>Register Name</td>
<td>Bit</td>
<td>Field</td>
<td>Type</td>
<td>Default</td>
<td>EEPROM Reg Bit</td>
</tr>
<tr>
<td>---------</td>
<td>------------------</td>
<td>------</td>
<td>---------------</td>
<td>------</td>
<td>---------</td>
<td>----------------</td>
</tr>
<tr>
<td>0x09</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td>0x0A</td>
<td>Signal Detect</td>
<td>7.0</td>
<td>SD_TH Status</td>
<td>R</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Monitor</td>
<td></td>
<td>[7]: CH7 – CHA_3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[5]: CH5 – CHA_1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[3]: CH3 – CHB_3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[1]: CH1 – CHB_1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Signal detected at input</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: These bits only function when RESERVED2 pin = FLOAT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0B</td>
<td>Reserved</td>
<td>7</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x70</td>
<td>Yes</td>
</tr>
<tr>
<td>0x0C</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
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<td>EQ Control</td>
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<td>VOD Control</td>
<td>R/W</td>
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### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0x11    | CH0 - CHB_0        | 7   | RXDET Status    | R    |         |                | Observation bit for RXDET CH0 - CHB_0  
1 = Input 50 Ω terminated to VDD  
0 = Input is Hi-Z  
|         |                    | 6:5 | Reserved        |      |         |                | Set bits to 0                                                                                                                                 |
|         |                    | 4:3 | Reserved        |      |         |                | Set bits to 0                                                                                                                                 |
|         | VOD_DB             | 2:0 | VOD_DB Control  | R/W  | 0x02    | Yes            | OUTB_0 VOD_DB Control  
000'b = 0 dB (recommended)  
001'b = –1.5 dB  
010'b = –3.5 dB (default)  
011'b = –5 dB  
100'b = –6 dB  
101'b = –8 dB  
110'b = –9 dB  
111'b = –12 dB  
Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction. |
| 0x12    | CH0 - CHB_0        | 7   | Reserved        | R/W  | 0x00    | Yes            | Set bit to 0                                                                                                                                 |
|         | SD_TH              | 6:4 | Reserved        |      |         |                | Set bits to 0                                                                                                                                 |
|         |                    | 3:2 | Signal Detect Status Assert Threshold | R/W  |         | Yes            | Status Assert threshold (1010 pattern 12 Gbps)  
00'b = 50 mVp-p (default)  
01'b = 40 mVp-p  
10'b = 75 mVp-p  
11'b = 58 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
|         |                    | 1:0 | Signal Detect Status De-assert Threshold | R/W  |         | Yes            | Status De-assert threshold (1010 pattern 12 Gbps)  
00'b = 37 mVp-p (default)  
01'b = 22 mVp-p  
10'b = 55 mVp-p  
11'b = 45 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
| 0x13    | Reserved           | 7:0 | Reserved        | R/W  | 0x00    | Set bits to 0  | Set bits to 0                                                                                                                                 |
| 0x14    | Reserved           | 7:0 | Reserved        | R/W  | 0x00    | Set bits to 0  | Set bits to 0                                                                                                                                 |
| 0x15    | CH1 - CHB_1        | 7:6 | Reserved        |      |         |                | Set bits to 0                                                                                                                                 |
|         | RXDET              | 5:4 | Reserved        |      |         |                | Set bits to 0                                                                                                                                 |
|         |                    | 3:2 | RXDET           | R/W  | 0x00    | Yes            | 00'b = Input is Hi-Z impedance  
01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω  
10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω  
11'b = Input is 50 Ω  
Note: Override RXDET pin and enable register control via Reg 0x08[3] |
| 0x16    | CH1 - CHB_1        | 7:0 | EQ Control      | R/W  | 0x2F    | Yes            | INB_1 EQ Control - total of four levels. See Table 4.                                                                                      |

Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x17</td>
<td>CH1 - CHB_1 VOD</td>
<td>7</td>
<td>Short Circuit Protection</td>
<td>0x0</td>
<td>Yes</td>
<td>0xAD</td>
<td>1 = Enable the short circuit protection 0 = Disable the short circuit protection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:3</td>
<td>Reserved</td>
<td>R/W</td>
<td>Yes</td>
<td></td>
<td>Set bits to 0101'b</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:0</td>
<td>VOD Control</td>
<td>R/W</td>
<td>Yes</td>
<td></td>
<td>OUTB_1 VOD Control: VOD / VID Ratio</td>
</tr>
<tr>
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<td>000'b = 0.57</td>
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<td></td>
<td></td>
<td>001'b = 0.65</td>
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<td>010'b = 0.71</td>
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<td>011'b = 0.77</td>
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<td>100'b = 0.83</td>
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<td>101'b = 0.90 (default)</td>
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<td></td>
<td>110'b = 1.00 (recommended)</td>
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<td>111'b = 1.04</td>
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<td>CH1 - CHB_1 VOD</td>
<td>7</td>
<td>RXDET Status</td>
<td>R</td>
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<td>Observation bit for RXDET CH1 - CHB_1</td>
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<td>6:5</td>
<td>Reserved</td>
<td>R/W</td>
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<td>1 = Input 50 Ω terminated to VDD</td>
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<td>4:3</td>
<td>Reserved</td>
<td>R/W</td>
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<td>0 = Input is Hi-Z</td>
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<tr>
<td>0x18</td>
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<td>2:0</td>
<td>VOD_DB Control</td>
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<td>OUTB_1 VOD_DB Control</td>
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<td>000'b = 0 dB (recommended)</td>
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<td>001'b = –1.5 dB</td>
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<td>010'b = –3.5 dB (default)</td>
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<td>011'b = –5 dB</td>
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<td>100'b = –6 dB</td>
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<td>101'b = –8 dB</td>
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<td>110'b = –9 dB</td>
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<td>111'b = –12 dB</td>
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<td>Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.</td>
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<tr>
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<td>CH1 - CHB_1 SD_TH</td>
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<td>Reserved</td>
<td>R/W</td>
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<td>0x00</td>
<td>Status Assert threshold (1010 pattern 12 Gbps)</td>
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<td>6:4</td>
<td>Reserved</td>
<td>R/W</td>
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<td>00'b = 50 mVP-p</td>
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<td>3:2</td>
<td>Signal Detect Status Assert Threshold</td>
<td>R/W</td>
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<td>01'b = 40 mVP-p</td>
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<td>10'b = 75 mVP-p</td>
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<td>11'b = 58 mVP-p</td>
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<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
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<td>1:0</td>
<td>Signal Detect Status De-assert Threshold</td>
<td>R/W</td>
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<td>0x00</td>
<td>Status De-assert threshold (1010 pattern 12 Gbps)</td>
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<td>00'b = 37 mVP-p</td>
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<td>01'b = 22 mVP-p</td>
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<td>10'b = 55 mVP-p</td>
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<td>11'b = 45 mVP-p</td>
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<td></td>
<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
</tr>
</tbody>
</table>

| 0x1A    | Reserved             | 7:0 | Reserved        | R/W   | 0x00    |                | Set bits to 0                                                              |
| 0x1B    | Reserved             | 7:0 | Reserved        | R/W   | 0x00    |                | Set bits to 0                                                              |
### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
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<td>CH2 - CHB_2</td>
<td>7:6</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td>RXDET</td>
<td>5:4</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3:2</td>
<td>RXDET</td>
<td>R/W</td>
<td>0x00</td>
<td>Yes</td>
<td>00'b = Input is Hi-Z impedance 01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω 10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω 11'b = Input is 50 Ω Note: Override RXDET pin and enable register control via Reg 0x08[3]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td>0x1D</td>
<td>CH2 - CHB_2</td>
<td>7:0</td>
<td>EQ Control</td>
<td>R/W</td>
<td>0x2F</td>
<td>Yes</td>
<td>INB_2 EQ Control - total of four levels. See Table 4.</td>
</tr>
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<td>Eq</td>
<td>6:3</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x2F</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:0</td>
<td>VOD Control</td>
<td>R/W</td>
<td>0xAD</td>
<td>Yes</td>
<td>OUTB_2 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83 101'b = 0.90 (default) 110'b = 1.00 (recommended) 111'b = 1.04</td>
</tr>
<tr>
<td>0x1E</td>
<td>CH2 - CHB_2</td>
<td>7</td>
<td>Short Circuit Protection</td>
<td>R/W</td>
<td>0xAD</td>
<td>Yes</td>
<td>1 = Enable the short circuit protection 0 = Disable the short circuit protection</td>
</tr>
<tr>
<td></td>
<td>VOD</td>
<td>6:3</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x02</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
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<td></td>
<td>2:0</td>
<td>VOD_DB Control</td>
<td>R/W</td>
<td>0x02</td>
<td>Yes</td>
<td>Observation bit for RXDET CH2 - CHB_2 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z</td>
</tr>
<tr>
<td>0x1F</td>
<td>CH2 - CHB_2</td>
<td>7</td>
<td>RXDET Status</td>
<td>R</td>
<td>0x02</td>
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<td>Set bits to 0</td>
</tr>
<tr>
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<td>VOD_DB</td>
<td>6:5</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x02</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4:3</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x02</td>
<td></td>
<td>Set bits to 0</td>
</tr>
</tbody>
</table>

Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.
### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x20</td>
<td>CH2 - CHB_2</td>
<td>7</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Set bit to 0</td>
</tr>
<tr>
<td></td>
<td>SD_TH</td>
<td>6:4</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3:2</td>
<td>Signal Detect</td>
<td></td>
<td>Yes</td>
<td>0x00</td>
<td>Status Assert threshold (1010 pattern 12 Gbps)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Status Assert</td>
<td></td>
<td></td>
<td></td>
<td>00'b = 50 mVp-p (default)</td>
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<td>01'b = 40 mVp-p</td>
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<td>10'b = 75 mVp-p</td>
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<td>11'b = 58 mVp-p</td>
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<td>Note: Override</td>
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<td>SD_TH pin and enable register control via Reg 0x08[6]</td>
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<td>R/W</td>
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<td>Set bits to 0</td>
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<td>Set bits to 0</td>
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<td>RXDET</td>
<td>R/W</td>
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<td>00'b = Input is Hi-Z impedance</td>
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<td>01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
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<td>10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
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<td>11'b = Input is 50 Ω</td>
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<td>Note: Override RXDET pin and enable register control via Reg 0x08[3]</td>
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<td>CH3 - CHB_3</td>
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<td>R/W</td>
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<td>INB_3 EQ Control - total of four levels. See Table 4.</td>
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<td>1 = Enable the short circuit protection</td>
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<td>Protection</td>
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<td>0 = Disable the short circuit protection</td>
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<td>2:0</td>
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<td>OUTB_3 VOD Control: VOD / VID Ratio</td>
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<td>000'b = 0.57</td>
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<td>001'b = 0.65</td>
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<td>010'b = 0.71</td>
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<td>011'b = 0.77</td>
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<td>100'b = 0.83</td>
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<td>101'b = 0.90 (default)</td>
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<td>110'b = 1.00 (recommended)</td>
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<td>111'b = 1.04</td>
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### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0x26    | CH3 - CHB_3 VOD_DB | 7    | RXDET Status     | R    | 1       | 0x02           | Observation bit for RXDET CH3 - CHB_3  
1 = Input 50 Ω terminated to VDD  
0 = Input is Hi-Z                                                              |
|         |                 | 6:5  | Reserved         |      |         |                | Set bits to 0                                                                                       |
|         |                 | 4:3  | Reserved         |      |         |                | Set bits to 0                                                                                       |
| 0x26    | CH3 - CHB_3 VOD_DB | 2:0  | VOD_DB Control   | R/W  | Yes     | 0x02           | OUTB_3 VOD_DB Control  
000'b = 0 dB (recommended)  
001'b = −1.5 dB  
010'b = −3.5 dB (default)  
011'b = −5 dB  
100'b = −6 dB  
101'b = −8 dB  
110'b = −9 dB  
111'b = −12 dB (default)  
Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction. |
| 0x27    | CH3 - CHB_3 SD_TH | 7    | Reserved         |      | Yes     | 0x00           | Status Assert threshold (1010 pattern 12 Gbps)  
00'b = 50 mVp-p (default)  
01'b = 40 mVp-p  
10'b = 75 mVp-p  
11'b = 58 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
|         |                 | 6:4  | Reserved         |      |         |                | Set bits to 0                                                                                       |
|         |                 | 3:2  | Signal Detect Status Assert Threshold | R/W  | Yes     | 0x00           | Status De-assert threshold (1010 pattern 12 Gbps)  
00'b = 37 mVp-p (default)  
01'b = 22 mVp-p  
10'b = 55 mVp-p  
11'b = 45 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
|         |                 | 1:0  | Signal Detect Status De-assert Threshold | R/W  | Yes     | 0x00           |                                               |
| 0x28    | Signal Detect Status Control | 7    | Reserved         |      |         | 0x00           | Set bits to 0                                                                                       |
|         |                 | 6    | Reserved         |      |         |                | Set bits to 1                                                                                       |
|         |                 | 5:4  | High SD_TH Status | R/W  | Yes     | 0x4C           | Enable Higher Range of Signal Detect Status Thresholds  
[5]: CH0 - CH3  
[4]: CH4 - CH7 |
|         |                 | 3:2  | Fast Signal Detect Status | R/W  | Yes     | 0x4C           | Enable Fast Signal Detect Status  
[3]: CH0 - CH3  
[2]: CH4 - CH7  
Note: In Fast Signal Detect, assert/de-assert response occurs after approximately 3-4 ns |
|         |                 | 1:0  | Reduced SD Status Gain | R/W  | Yes     | 0x4C           | Enable Reduced Signal Detect Status Gain  
[1]: CH0 - CH3  
[0]: CH4 - CH7 |
| 0x29    | Reserved        | 7:0  | Reserved         | R/W  | 0x00    | 0x00           | Set bits to 0                                                                                       |
| 0x2A    | Reserved        | 7:0  | Reserved         | R/W  | 0x00    | 0x00           | Set bits to 0                                                                                       |
### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
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<tr>
<td>0x2B</td>
<td>CH4 - CHA_0</td>
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<td>Set bits to 0</td>
<td>R/W 0x00</td>
<td>00'b = Input is Hi-Z impedance</td>
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<td>RXDET</td>
<td>5:4</td>
<td>Reserved</td>
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<td>Set bits to 0</td>
<td></td>
<td>01'b = Auto Rx-Detect,</td>
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<td>outputs test every 12 ms for 600 ms (50 times) then</td>
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<td>stops; termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
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<td>10'b = Auto Rx-Detect,</td>
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<td>outputs test every 12 ms until detection occurs;</td>
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<td>termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
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<td>11'b = Input is 50 Ω Note: Override RXDET pin and enable register control</td>
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<td>via Reg 0x08[3]</td>
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<td>Reserved</td>
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<td>Set bits to 0</td>
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<td>00'b = Input is 50 Ω terminated to VDD</td>
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<td>0x2C</td>
<td>CH4 - CHA_0</td>
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<td>EQ Control</td>
<td>R/W</td>
<td>0x2F</td>
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<td>01'b = Input is Hi-Z</td>
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<td>Eq</td>
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<td>11'b = 50 Ω terminated to VDD</td>
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<td>Note: Override RXDET pin and enable register control</td>
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<td>via Reg 0x08[3]</td>
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<td>Set bits to 0</td>
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<td>00'b = Enable the short circuit protection</td>
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<td>OUTA_0 VOD Control: VOD / VID Ratio</td>
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<td>001'b = 0.65</td>
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<td>101'b = 0.90 (default)</td>
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<td>110'b = 1.00 (recommended)</td>
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<td>111'b = 1.04</td>
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<td>Set bits to 0</td>
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<td>00'b = 0 dB (recommended)</td>
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<td>01'b = –1.5 dB</td>
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<td>10'b = –3.5 dB (default)</td>
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<td>00'b = –6 dB</td>
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<td>Note: Changing VOD_DB bits effectively lowers the</td>
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<td>Signal Detect</td>
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<td>Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default)</td>
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<td>11'b = 58 mVp-p</td>
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<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
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<td>R/W</td>
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<td>RXDET</td>
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<td>3:2</td>
<td>RXDET</td>
<td>R/W</td>
<td>Yes</td>
<td>00'b</td>
<td>Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default)</td>
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<td>01'b = 22 mVp-p</td>
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<td>10'b</td>
<td>10'b = 55 mVp-p</td>
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<td>11'b</td>
<td>11'b = 45 mVp-p</td>
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<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
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<td>R/W</td>
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<td>INA_1 EQ Control - total of four levels. See Table 4.</td>
</tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x34</td>
<td>CH5 - CHA_1</td>
<td>7</td>
<td>Short Circuit</td>
<td>R/W</td>
<td>Yes</td>
<td>0x0D</td>
<td>1 = Enable the short circuit protection 0 = Disable the short circuit protection</td>
</tr>
<tr>
<td></td>
<td>VOD</td>
<td>6:3</td>
<td>Protection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:0</td>
<td>VOD Control</td>
<td>R/W</td>
<td>Yes</td>
<td>0xAD</td>
<td>OUTA_1 VOD Control: VOD / VID Ratio 000'b = 0.57 001'b = 0.65 010'b = 0.71 011'b = 0.77 100'b = 0.83</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101'b</td>
<td>101'b = 0.90 (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110'b</td>
<td>110'b = 1.00 (recommended)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111'b</td>
<td>111'b = 1.04</td>
</tr>
</tbody>
</table>

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### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0x35    | CH5 - CHA_1 VOD_DB    | 7   | RXDET Status | R    |         | 0x02          | Observation bit for RXDET CH5 - CHA1  
1 = Input 50 Ω terminated to VDD  
0 = Input is Hi-Z  
Set bits to 0                                                                                   |
|         |                       | 6:5 | Reserved |      |         |                |                                                                                               |
|         |                       | 4:3 | Reserved |      |         |                |                                                                                               |
|         |                       | 2:0 | VOD_DB Control | R/W |         | Yes           | OUTA_1 VOD_DB Control  
000'b = 0 dB (recommended)  
001'b = –1.5 dB  
010'b = –3.5 dB (default)  
011'b = –5 dB  
100'b = –6 dB  
101'b = –8 dB  
110'b = –9 dB  
111'b = –12 dB  
Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction. |
| 0x36    | CH5 - CHA_1 SD_TH     | 7   | Reserved |      |         | 0x00          | Yes Set bit to 0                                                                                   |
|         |                       | 6:4 | Reserved |      |         |                |                                                                                               |
|         |                       | 3:2 | Signal Detect Status Assert Threshold | R/W |         | Yes           | Status Assert threshold (1010 pattern 12 Gbps)  
00'b = 50 mVp-p (default)  
01'b = 40 mVp-p  
10'b = 75 mVp-p  
11'b = 58 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
|         |                       |     |         |      |         |                |                                                                                               |
|         |                       | 1:0 | Signal Detect Status De-assert Threshold | R/W |         | Yes           | Status De-assert threshold (1010 pattern 12 Gbps)  
00'b = 37 mVp-p (default)  
01'b = 22 mVp-p  
10'b = 55 mVp-p  
11'b = 45 mVp-p  
Note: Override SD_TH pin and enable register control via Reg 0x08[6] |
| 0x37    | Reserved              | 7:0 | Reserved | R/W  | 0x00    |                | Set bits to 0                                                                                   |
| 0x38    | Reserved              | 7:0 | Reserved | R/W  | 0x00    |                | Set bits to 0                                                                                   |
| 0x39    | CH6 - CHA_2 RXDET    | 7:6 | Reserved |      |         |                |                                                                                               |
|         |                       | 5:4 | Reserved |      |         |                |                                                                                               |
|         |                       | 3:2 | RXDET | R/W  | 0x00    | Yes           | 00'b = Input is Hi-Z impedance  
01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω  
10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω  
11'b = Input is 50 Ω  
Note: Override RXDET pin and enable register control via Reg 0x08[3] |
|         |                       | 1:0 | Reserved |      |         |                |                                                                                               |
| 0x3A    | CH6 - CHA_2 EQ       | 7:0 | EQ Control | R/W  | 0x2F    | Yes           | INA_2 EQ Control - total of four levels.  
See Table 4.                                                                                  |
### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3B</td>
<td>CH6 - CHA_2 VOD</td>
<td>7</td>
<td>Short Circuit Protection</td>
<td>R/W</td>
<td>Yes</td>
<td>0xAD</td>
<td>1 = Enable the short circuit protection 0 = Disable the short circuit protection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:3</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Set bits to 0101'b</td>
</tr>
<tr>
<td>0x3C</td>
<td>CH6 - CHA_2 VOD_DB</td>
<td>7</td>
<td>RXDET Status</td>
<td>R</td>
<td></td>
<td></td>
<td>Observation bit for RXDET CH6 - CHA_2 1 = Input 50 Ω terminated to VDD 0 = Input is Hi-Z</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:5</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4:3</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td>0x3D</td>
<td>CH6 - CHA_2 SD_TH</td>
<td>7</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td>0x00</td>
<td>Set bit to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:4</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3:2</td>
<td>Signal Detect Status Assert Threshold</td>
<td>R/W</td>
<td>Yes</td>
<td>0x00</td>
<td>Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default) 01'b = 40 mVp-p 10'b = 75 mVp-p 11'b = 58 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1:0</td>
<td>Signal Detect Status De-assert Threshold</td>
<td>R/W</td>
<td>Yes</td>
<td>0x00</td>
<td>Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default) 01'b = 22 mVp-p 10'b = 55 mVp-p 11'b = 45 mVp-p Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
</tr>
<tr>
<td>0x3E</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td>0x3F</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
</tbody>
</table>
Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x40</td>
<td>CH7 - CHA_3 RXDET</td>
<td>7:6</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td>00'b = Input is Hi-Z impedance</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5:4</td>
<td>Reserved</td>
<td>Yes</td>
<td>01'b = Auto Rx-Detect, outputs test every 12 ms for 600 ms (50 times) then stops; termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4:3</td>
<td>Reserved</td>
<td>Yes</td>
<td>10'b = Auto Rx-Detect, outputs test every 12 ms until detection occurs; termination is Hi-Z until detection; once detected input termination is 50 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3:2</td>
<td>RXDET</td>
<td>Yes</td>
<td>11'b = Input is 50 Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1:0</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>Note: Override RXDET pin and enable register control via Reg 0x08[3]</td>
<td></td>
</tr>
<tr>
<td>0x41</td>
<td>CH7 - CHA_3 EQ</td>
<td>7:0</td>
<td>EQ Control</td>
<td>R/W</td>
<td>0x2F</td>
<td>Yes</td>
<td>INA_3 EQ Control - total of four levels. See Table 4.</td>
</tr>
<tr>
<td>0x42</td>
<td>CH7 - CHA_3 VOD</td>
<td>7</td>
<td>Short Circuit Protection</td>
<td>Yes</td>
<td>1 = Enable the short circuit protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:3</td>
<td>Reserved</td>
<td>Yes</td>
<td>0 = Disable the short circuit protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:0</td>
<td>VOD Control</td>
<td>0xAD</td>
<td>0xAD</td>
<td>OUTA_3 VOD Control: VOD / VID Ratio</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>000'b = 0.57</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001'b = 0.65</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010'b = 0.71</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011'b = 0.77</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100'b = 0.83</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101'b = 0.90 (default)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110'b = 1.00 (recommended)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111'b = 1.04</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x43</td>
<td>CH7 - CHA_3 VOD_DB</td>
<td>7</td>
<td>RXDET Status</td>
<td>R</td>
<td></td>
<td>Observation bit for RXDET CH7 - CHA_3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:5</td>
<td>Reserved</td>
<td></td>
<td>1 = Input 50 Ω terminated to VDD</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4:3</td>
<td>Reserved</td>
<td></td>
<td>0 = Input is Hi-Z</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2:0</td>
<td>VOD_DB Control</td>
<td>0x02</td>
<td>0x02</td>
<td>OUTA_3 VOD_DB Control</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Yes</td>
<td>000'b = 0 dB (recommended)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001'b = –1.5 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010'b = –3.5 dB (default)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011'b = –5 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100'b = –6 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101'b = –8 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110'b = –9 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111'b = –12 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: Changing VOD_DB bits effectively lowers the output VOD dynamic range by a factor of the corresponding amount of dB reduction.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x44</td>
<td>CH7 - CHA_3 SD_TH</td>
<td>7</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Set bit to 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:4</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>Set bits to 0</td>
</tr>
<tr>
<td>0x45</td>
<td>Reserved</td>
<td>7</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>0x00</td>
<td>Status Assert threshold (1010 pattern 12 Gbps) 00'b = 50 mVp-p (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01'b = 40 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10'b = 75 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11'b = 58 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:4</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
</tr>
<tr>
<td>0x46</td>
<td>Reserved</td>
<td>7</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>0x00</td>
<td>Status De-assert threshold (1010 pattern 12 Gbps) 00'b = 37 mVp-p (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01'b = 22 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10'b = 55 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11'b = 45 mVp-p</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6:4</td>
<td>Reserved</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Note: Override SD_TH pin and enable register control via Reg 0x08[6]</td>
</tr>
</tbody>
</table>

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### Table 9. SMBus Slave Mode Register Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Default</th>
<th>EEPROM Reg Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x61</td>
<td>Reserved</td>
<td>7:0</td>
<td>Reserved</td>
<td>R/W</td>
<td>0x00</td>
<td></td>
<td>Set bits to 0</td>
</tr>
</tbody>
</table>
8 Applications and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Signal Integrity in 40G-CR4/KR4/SAS/SATA/PCIe Applications

In 40G-CR4/KR4/SAS/SATA/PCIe applications, specifications require Rx-Tx link training to establish and optimize signal conditioning settings for data rates up to 12.5 Gbps. In link training, the Rx partner requests a series of FIR coefficients from the Tx partner at speed. This polling sequence is designed to pre-condition the signal path with an optimized link between the endpoints. Link training occurs at the following data-rates:

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Operating Data Rate (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40G-CR4</td>
<td>10.3125</td>
</tr>
<tr>
<td>40G-KR4</td>
<td>10.3125</td>
</tr>
<tr>
<td>SAS-3</td>
<td>12.0</td>
</tr>
<tr>
<td>PCIe Gen-3</td>
<td>8.0</td>
</tr>
</tbody>
</table>

(1) There is no link training with Tx FIR coefficients for the respective lower generation data rates.

The DS125BR820 works to extend the reach possible by using active linear equalization to the channel, boosting attenuated signals so that they can be more easily recovered at the Rx. The repeater outputs are specially designed to be transparent to Tx FIR signaling in order to pass information critical for optimal link training to the Rx. Suggested settings for the A-channels and B-channels are given in Table 11 and Table 12. Further adjustments to $EQ_x$ and $VOD_x$ settings may optimize signal margin on the link for different system applications:

Table 10. Link Training Data-Rates

<table>
<thead>
<tr>
<th>Protocol(1)</th>
<th>Operating Data Rate (Gbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40G-CR4</td>
<td>10.3125</td>
</tr>
<tr>
<td>40G-KR4</td>
<td>10.3125</td>
</tr>
<tr>
<td>SAS-3</td>
<td>12.0</td>
</tr>
<tr>
<td>PCIe Gen-3</td>
<td>8.0</td>
</tr>
</tbody>
</table>

Table 11. Suggested Device Settings in Pin Mode

<table>
<thead>
<tr>
<th>Channel Settings</th>
<th>Pin Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$EQ_x$</td>
<td>Level 1</td>
</tr>
<tr>
<td>$VOD_x[1:0]$</td>
<td>Level 6 (1, 0)</td>
</tr>
</tbody>
</table>

Table 12. Suggested Device Settings in SMBus Modes

<table>
<thead>
<tr>
<th>Channel Settings</th>
<th>SMBus Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$EQ_x$</td>
<td>0x00</td>
</tr>
<tr>
<td>$VOD_x$</td>
<td>110'b</td>
</tr>
<tr>
<td>$VOD_{DB}$</td>
<td>000'b</td>
</tr>
</tbody>
</table>

The SMBus Slave Mode code example in Table 13 may be used to program the DS125BR820 with the recommended device settings:

Table 13. SMBus Example Sequence

<table>
<thead>
<tr>
<th>Register</th>
<th>Write Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x06</td>
<td>0x18</td>
<td>Set SMBus Slave Mode Register Enable.</td>
</tr>
<tr>
<td>0x0F</td>
<td>0x00</td>
<td>Set CHB_0 EQ to 0x00.</td>
</tr>
<tr>
<td>0x10</td>
<td>0xAE</td>
<td>Set CHB_0 VOD to 110'b.</td>
</tr>
<tr>
<td>0x11</td>
<td>0x00</td>
<td>Set CHB_0 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x16</td>
<td>0x00</td>
<td>Set CHB_1 EQ to 0x00.</td>
</tr>
<tr>
<td>0x17</td>
<td>0xAE</td>
<td>Set CHB_1 VOD to 110'b.</td>
</tr>
</tbody>
</table>
Table 13. SMBus Example Sequence (continued)

<table>
<thead>
<tr>
<th>Register</th>
<th>Write Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x18</td>
<td>0x00</td>
<td>Set CHB_1 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x1D</td>
<td>0x00</td>
<td>Set CHB_2 EQ to 0x00.</td>
</tr>
<tr>
<td>0x1E</td>
<td>0xAE</td>
<td>Set CHB_2 VOD to 110'b.</td>
</tr>
<tr>
<td>0x1F</td>
<td>0x00</td>
<td>Set CHB_2 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x24</td>
<td>0x00</td>
<td>Set CHB_3 EQ to 0x00.</td>
</tr>
<tr>
<td>0x25</td>
<td>0xAE</td>
<td>Set CHB_3 VOD to 110'b.</td>
</tr>
<tr>
<td>0x26</td>
<td>0x00</td>
<td>Set CHB_3 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x2C</td>
<td>0x00</td>
<td>Set CHA_0 EQ to 0x00.</td>
</tr>
<tr>
<td>0x2D</td>
<td>0xAE</td>
<td>Set CHA_0 VOD to 110'b.</td>
</tr>
<tr>
<td>0x2E</td>
<td>0x00</td>
<td>Set CHA_0 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x33</td>
<td>0x00</td>
<td>Set CHA_1 EQ to 0x00.</td>
</tr>
<tr>
<td>0x34</td>
<td>0xAE</td>
<td>Set CHA_1 VOD to 110'b.</td>
</tr>
<tr>
<td>0x35</td>
<td>0x00</td>
<td>Set CHA_1 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x3A</td>
<td>0x00</td>
<td>Set CHA_2 EQ to 0x00.</td>
</tr>
<tr>
<td>0x3B</td>
<td>0xAE</td>
<td>Set CHA_2 VOD to 110'b.</td>
</tr>
<tr>
<td>0x3C</td>
<td>0x00</td>
<td>Set CHA_2 VOD_DB to 000'b.</td>
</tr>
<tr>
<td>0x41</td>
<td>0x00</td>
<td>Set CHA_3 EQ to 0x00.</td>
</tr>
<tr>
<td>0x42</td>
<td>0xAE</td>
<td>Set CHA_3 VOD to 110'b.</td>
</tr>
<tr>
<td>0x43</td>
<td>0x00</td>
<td>Set CHA_3 VOD_DB to 000'b.</td>
</tr>
</tbody>
</table>

8.1.2 Signal Integrity in 40G-SR4/LR4 Applications

In 40G-SR4/LR4 applications, the ideal device settings must be tuned. In particular, EQ and VOD settings must be optimized in order to aid the link partners in meeting the nPPI eye mask test. While tuning the DS125BR820 contributes to signal quality improvement, it is equally important to ensure that the link partner ASIC Tx FIR signal characteristics are optimized as well to facilitate error-free data transmission. Suggested settings for the A-channels and B-channels in a 40G-SR4/LR4 environment can be referenced in Table 11 and Table 12.

8.1.3 Rx Detect Functionality in 40G-CR4/KR4/SAS/SATA Applications

Unlike PCIe systems, 40G-CR4/KR4/SAS/SATA systems use a low speed communications sequence to detect and communicate device capabilities between host ASIC and link partners. This communication eliminates the need to detect for endpoints like in a PCIe application. For 40G-CR4/KR4/SAS/SATA systems, it is recommended to tie the RXDET pin high. This ensures any link-training sequences sent by the host ASIC can reach the link partner receiver without any additional latency due to termination detection sequences.

8.2 Typical Applications

8.2.1 Generic High Speed Repeater

The DS125BR820 extends PCB and cable reach in multiple applications by using active linear equalization. The high linearity of this device aids specifically in protocols requiring link training and can be used in line cards, backplanes, motherboards, and active cable assemblies, thereby improving margin and overall eye performance. The capability of the repeater can be explored across a range of data rates and ASIC-to-link-partner signaling, as shown in the following two test setup connections.

![Test Setup Connections Diagram](image-url)
Typical Applications (continued)

![Test Setup Connections Diagram](image)

**Figure 10. Test Setup Connections Diagram**

### 8.2.1.1 Design Requirements
As with any high speed design, there are many factors which influence the overall performance. Below are a list of critical areas for consideration and study during design.

- Use 100 Ω impedance traces. Generally these are very loosely coupled to ease routing length differences.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- The maximum body size for AC-coupling capacitors is 0402.
- Back-drill connector vias and signal vias to minimize stub length.
- Use Reference plane vias to ensure a low inductance path for the return current.

### 8.2.1.2 Detailed Design Procedure
The DS125BR820 is designed to be placed at an offset location with respect to the overall channel attenuation. In order to optimize performance, the repeater requires tuning to extend the reach of the cable or trace length while also recovering a solid eye opening. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance for each specific application environment.

Examples of the repeater performance as a generic high speed datapath repeater are illustrated in the performance curves in the next section.

### 8.2.1.3 Application Performance Plots

![Performance Curves](image)

**Figure 11. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps**

**Figure 12. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps**
Typical Applications (continued)

No Repeater Used
TJ (1.0E-12) = 43.7 ps

Figure 13. TL = 10 Inch 5-Mil FR4 Trace, No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 18.1 ps

Figure 14. TL = 10 Inch 5-Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps

No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye

Figure 15. TL = 20 Inch 5-Mil FR4 Trace, No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 35.5 ps

Figure 16. TL = 20 Inch 5-Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps

No Repeater
TJ (1.0E-12) = Not Available Due to Closed Eye

Figure 17. TL = 5-Meter 30-AWG 100 Ω Twin-Axial Cable, No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 41.4 ps

Figure 18. TL = 5-Meter 30-AWG 100 Ω Twin-Axial Cable, DS125BR820 CHA_0, 8 Gbps
Typical Applications (continued)

No Repeater Used
TJ (1.0E-12) = 24.3 ps

Figure 19. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps

No Repeater Used
TJ (1.0E-12) = 50.6 ps

Figure 21. TL = 10 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps

No Repeater Used
TJ (1.0E-12) = 49.1 ps

Figure 23. TL = 20 Inch 5–Mil FR4 Trace, No Repeater, 10.3125 Gbps

DS125BR820 Settings: EQA = Level 2, VODA = Level 6
TJ (1.0E-12) = 14.0 ps

Figure 20. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps

DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 18.7 ps

Figure 22. TL = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 49.1 ps

Figure 24. TL = 20 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 10.3125 Gbps
Typical Applications (continued)

No Repeater
TJ (1.0E-12) = 26.1 ps
Figure 25. TL = 5 Inch 5–Mil FR4 Trace, No Repeater, 12 Gbps

DS125BR820 Settings: EQA = Level 2, VODA = Level 6
TJ (1.0E-12) = 13.1 ps
Figure 26. TL = 5 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 12 Gbps

No Repeater
TJ (1.0E-12) = 56.6 ps
Figure 27. TL = 10 Inch 5–Mil FR4 Trace, No Repeater, 12 Gbps

DS125BR820 Settings: EQA = Level 3, VODA = Level 6
TJ (1.0E-12) = 20.1 ps
Figure 28. TL = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 12 Gbps

No Repeater Used
TJ (1.0E-12) = Not Available Due to Closed Eye
Figure 29. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
TJ (1.0E-12) = 33.0 ps
Figure 30. TL1 = 15 Inch 5–Mil FR4 Trace, TL2 = 10 Inch 5–Mil FR4 Trace, DS125BR820 CHA_0, 8 Gbps
8.2.2 Front Port Applications (40G-CR4/SR4/LR4)

The DS125BR820 can be used in front port applications to extend the reach between the host ASIC and the front-port cage. Front port applications typically include 40G-CR4/SR4/LR4. For 40GbE front port optical protocols like 40G-SR4/LR4, the DS125BR820 is designed to support the front-port eye mask and jitter requirements of applicable standards like nPPI. For 40GbE front port copper protocols like 40G-CR4, the DS125BR820 is designed to provide channel equalization in a transparent fashion so as not to inhibit IEEE802.3ba Clause 72 link training. In all of these front port cases, the DS125BR820 can also be used to support eye mask and jitter requirements for SFF-8431 if the 40GbE QSFP+ port is intended to support 4x10G SFP+ applications as well. Below is a typical example of the DS125BR820 used in a front port line-card application.

![Typical Front-Port System Configuration](image)

8.2.2.1 Design Requirements

As with any high speed design, there are many factors that influence the overall performance. Please reference Design Requirements in the Generic High Speed Repeater application section for a list of critical areas for consideration and study during design.
Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

In front port applications, it is important to ensure that the placement of the DS125BR820 corresponds with the direction of the data flow, since the device is unidirectional. For egress applications, the DS125BR820 should be placed close to the connector cage, and for ingress applications, the DS125BR820 should be placed closer to the switch ASIC. Once the DS125BR820 placement is decided on the signal path, the repeater must be tuned. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance in order to meet the link training requirements for 40G-CR4 and eye mask requirements for 40G-SR4/LR4.

An example of a test configuration used to evaluate the DS125BR820 in this application can be seen in Figure 34. For more information about DS125BR820 front port applications, please refer to application note SNLA226:

![Figure 34. 10 GbE Transmitter with DS125BR820 QSFP+ Test Board](image)

8.2.2.3 Application Performance Plots

![DS125BR820 Settings: EQA = Level 2, VODA = Level 6](image)

DS125BR820 Settings: EQA = Level 2, VODA = Level 6

**Figure 35. nPPI Eye Mask Performance with 5 Inch 4-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps**

![DS125BR820 Settings: EQA = Level 2, VODA = Level 6](image)

DS125BR820 Settings: EQA = Level 2, VODA = Level 6

**Figure 36. nPPI Jitter Performance with 5 Inch 4-Mil FR4 Input Trace, Test Pattern = PRBS-9, 10.3125 Gbps**
8.2.3 PCIe Board Applications (PCIe Gen-3)

The DS125BR820 can be used to extend trace length on motherboards and line cards in PCIe Gen-3 applications. The high linearity of the DS125BR820 aids in the link training protocol required by PCIe Gen-3 at 8 Gbps in accordance with PCI-SIG standards. For PCIe Gen-3, preservation of the pre-cursor and post-cursor Tx FIR presets (P1-P10) is crucial to successful signal transmission from motherboard system root complex to line card ASIC or Embedded Processor. Below is a typical example of the DS125BR820 used in a PCIe application:

8.2.3.1 Design Requirements

As with any high speed design, there are many factors that influence the overall performance. Please reference Design Requirements in the Generic High Speed Repeater application section for a list of critical areas for consideration and study during design.
Typical Applications (continued)

8.2.3.2 Design Procedure

In PCIe Gen-3 applications, there is a large range of flexibility regarding the placement of the DS125BR820 in the signal path due to the high linearity of the device. If the PCIe slot must also support lower speeds like PCIe Gen-1 (2.5 Gbps) and Gen-2 (5.0 Gbps), it is recommended to place the DS125BR820 closer to the endpoint Rx. Once the DS125BR820 is placed on the signal path, the repeater must be tuned. To tune the repeater, the settings mentioned in Table 11 (for Pin Mode) and Table 12 (for SMBus Modes) are recommended as a default starting point for most applications. Once these settings are configured, additional tuning of the EQ and, to a lesser extent, VOD may be required to optimize the repeater performance to pass link training preset requirements for PCIe Gen-3.

An example of a test configuration used to evaluate the DS125BR820 in this application can be seen in Figure 40. For more information about DS125BR820 PCIe applications, please refer to application note SNLA227:

Figure 40. Typical PCIe Gen-3 Add-In Card Test Diagram
Typical Applications (continued)

8.2.3.3 Application Performance Plots

No Repeater Used
Composite Eye Height: 50.39 mV
Minimum Eye Width: 49.87 ps
Overall SigTest Result: Fail

Figure 41. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 112.2 mV
Minimum Eye Width: 83.82 ps
Overall SigTest Result: Pass

Figure 42. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
DS125BR820, 8 Gbps

No Repeater Used
Composite Eye Height: 50.39 mV
Minimum Eye Width: 49.87 ps
Overall SigTest Result: Fail

Figure 43. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 112.2 mV
Minimum Eye Width: 83.82 ps
Overall SigTest Result: Pass

Figure 44. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace, No TL2
DS125BR820, 8 Gbps
Typical Applications (continued)

No Repeater Used
Composite Eye Height: 0.057 mV
Minimum Eye Width: 37.66 ps
Overall SigTest Result: Fail

Figure 45. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 77.26 mV
Minimum Eye Width: 78.24 ps
Overall SigTest Result: Pass

Figure 46. PCIe Gen-3, Preset 7, Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
DS125BR820, 8 Gbps

No Repeater Used
Composite Eye Height: 0.057 mV
Minimum Eye Width: 37.66 ps
Overall SigTest Result: Fail

Figure 47. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
No Repeater, 8 Gbps

DS125BR820 Settings: EQA = Level 4, VODA = Level 6
Composite Eye Height: 77.26 mV
Minimum Eye Width: 78.24 ps
Overall SigTest Result: Pass

Figure 48. PCIe Gen-3, Preset 7, Non-Transition Eye
TL1 = 10 Inch 4-Mil FR4 Trace,
TL2 = 5 Inch 4-Mil FR4 Trace
DS125BR820, 8 Gbps
9 Power Supply Recommendations

Two approaches are recommended to ensure that the DS125BR820 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS125BR820. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

The DS125BR820 has an optional internal voltage regulator to provide the 2.5 V supply to the device. In 3.3 V mode operation, the VIN pin = 3.3 V is used to supply power to the device. The internal regulator then provides the 2.5 V to the VDD pins of the device and a 0.1 µF cap is needed at each of the five VDD pins for power supply de-coupling (total capacitance should equal 0.5 µF). The VDD_SEL pin must be tied to GND to enable the internal regulator. In 2.5 V mode operation, the VIN pin should be left open and 2.5 V supply must be applied to the five VDD pins to power the device. The VDD_SEL pin must be left open (no connect) to disable the internal regulator.

![3.3 V or 2.5 V Supply Connection Diagram](image-url)
10 Layout

10.1 Layout Guidelines

The CML inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 100 Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board. To minimize the effects of crosstalk, a 5:1 ratio or greater should be maintained between inter-pair and intra-pair spacing. See AN-1187 “Leadless Leadframe Package (LLP) Application Report” (literature number SNOA401) for additional information on QFN (WQFN) packages.

10.2 Layout Example

![Figure 50. Typical Routing Options](image-url)

The graphic shown above depicts different transmission line topologies which can be used in various combinations to achieve the optimal system performance. Impedance discontinuities at the differential via can be minimized or eliminated by increasing the swell around each hole and by providing for a low inductance return current path. When the via structure is associated with a thick backplane PCB, further optimization such as back drilling is often used to reduce the detrimental high frequency effects of stubs on the signal path.
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11.3 术语表
SLYZ022 — TI 术语表。
这份术语表列出并解释术语、首字母缩略词和定义。

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<td>逻辑</td>
<td><a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a></td>
</tr>
<tr>
<td>电源管理</td>
<td><a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a></td>
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<tr>
<td>微控制器 (MCU)</td>
<td><a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a></td>
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<tr>
<td>RFID系统</td>
<td><a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a></td>
</tr>
<tr>
<td>OMAP应用处理器</td>
<td><a href="http://www.ti.com/omap">www.ti.com/omap</a></td>
</tr>
<tr>
<td>无线连通性</td>
<td><a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a></td>
</tr>
</tbody>
</table>

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## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS125BR820NJYR</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>125B820A0</td>
<td></td>
</tr>
<tr>
<td>DS125BR820NJYT</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>125B820A0</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### REEL DIMENSIONS

- Reel Diameter: 330.0 mm
- Reel Width (W1): 16.4 mm
- A0: 5.8 mm
- B0: 10.3 mm
- K0: 1.0 mm
- P1: 12.0 mm
- W: 16.0 mm

### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS125BR820NJYR</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>5.8</td>
<td>10.3</td>
<td>1.0</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>DS125BR820NJYT</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>250</td>
<td>178.0</td>
<td>16.4</td>
<td>5.8</td>
<td>10.3</td>
<td>1.0</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS125BR820NJYR</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>2000</td>
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<td>38.0</td>
</tr>
<tr>
<td>DS125BR820NJYT</td>
<td>WQFN</td>
<td>NJY</td>
<td>54</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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