配备双电流检测运放和DC-DC降压稳压器的汽车用三相前级驱动器

查询样品: DRV8301-Q1

特性

- 符合汽车应用要求
- 具有经 **AEC-Q100** 测试的下列结果：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4A**
- 运行电源电压 **6V-60V**
- **2.3A** 灌电流和 **1.7A** 拉电流栅极驱动能力
- 集成双路具有可调增益和偏移的电流检测运放
- 集成降压转换器以支持高达 **1.5A** 外部负载
- 兼容**3**路或**6**路脉宽调制 **(PWM)** 输入方式的独立半桥控制
- 具有 **100%** 占空比支持的自举栅极驱动器
- 可编程死区时间以保护外部场效应晶体管 **(FET)** 不被击穿
- 减少电磁干扰 **(EMI)** 的转换率控制
- 外部 **MOSFET** 的可编程过流保护
- 兼容 **3.3V** 和 **5V** 数字逻辑接口
- **SPI** 接口
- 耐热增强型 **56** 引脚薄型小外形尺寸封装 **(TSSOP)** 散热垫向下 **DCA** 封装

应用范围

- 汽车用 **3** 相无刷直流电机和永磁同步电机
- 水泵、油泵、燃料泵

说明

DRV8301-Q1 是一款针对三相电机驱动应用的汽车用栅极驱动器集成电路 (IC)。 它提供三个半桥驱动器，每个驱动器能够驱动两个 N 类型 MOSFET，一个用于高侧，一个用于低侧。 它支持高达 2.3A 吸入和 1.7A 源出峰值电流能力，单一电源输入且电压范围宽（6V 至 60V）。 DRV8301-Q1 使用自举栅极驱动电路且支持 100% 占空比。 此栅极驱动器具有高侧 FET 和低侧 FET 自动握手短路保护，来防止短路电流击穿。 通过监测外接功率场效应管的Vds，提供对外部功率器件的过流保护。

DRV8301-Q1 包括两个用于精确电流测量的电流检测运放。 此电流检测运放支持双向电流感测，并且提供高达 3V 的可调输出偏移。

DRV8301-Q1 内部集成开关模式降压电源转换器，此转换器具有可调输出和开关频率，以支持外围微控制器 (MCU) 电源或额外的系统电源需求。 此降压转换器能够驱动高达 1.5A 负载。

SPI 接口提供详细的故障报告以及灵活的参数设置，诸如针对电流检测运放的增益控制，栅极驱动器的转换率控制等。

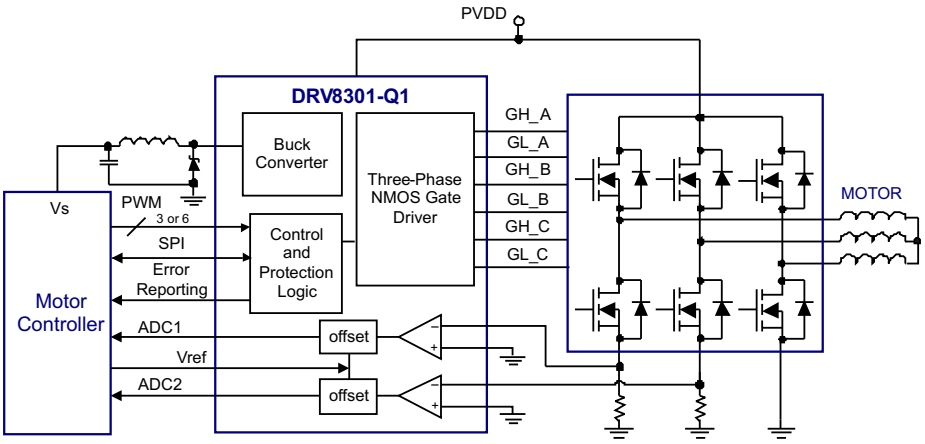


Figure 1. DRV8301 Simplified Application Schematic

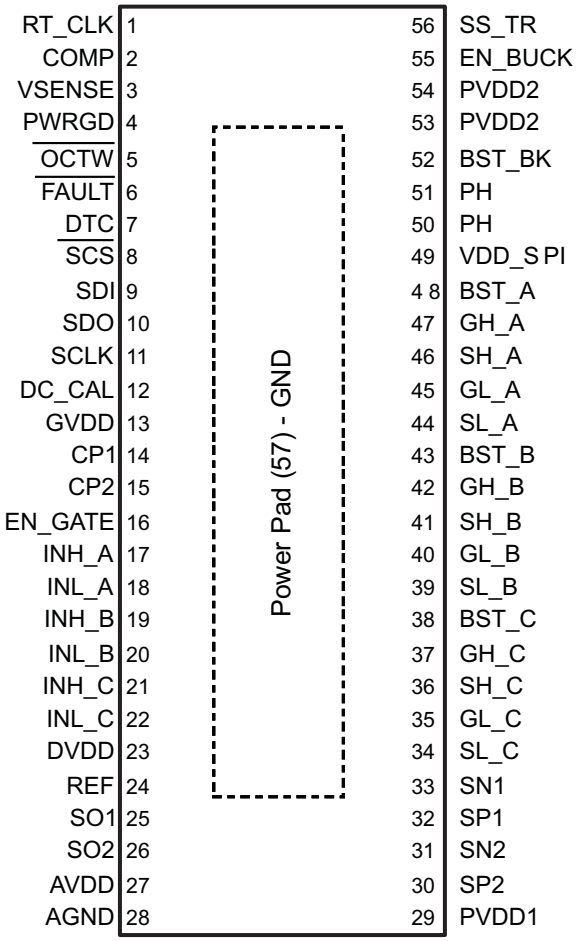
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

PIN ASSIGNMENT

The DRV8301-Q1 is designed to fit the 56-pin DCA package. Here is the pinout of the device.



PIN FUNCTIONS

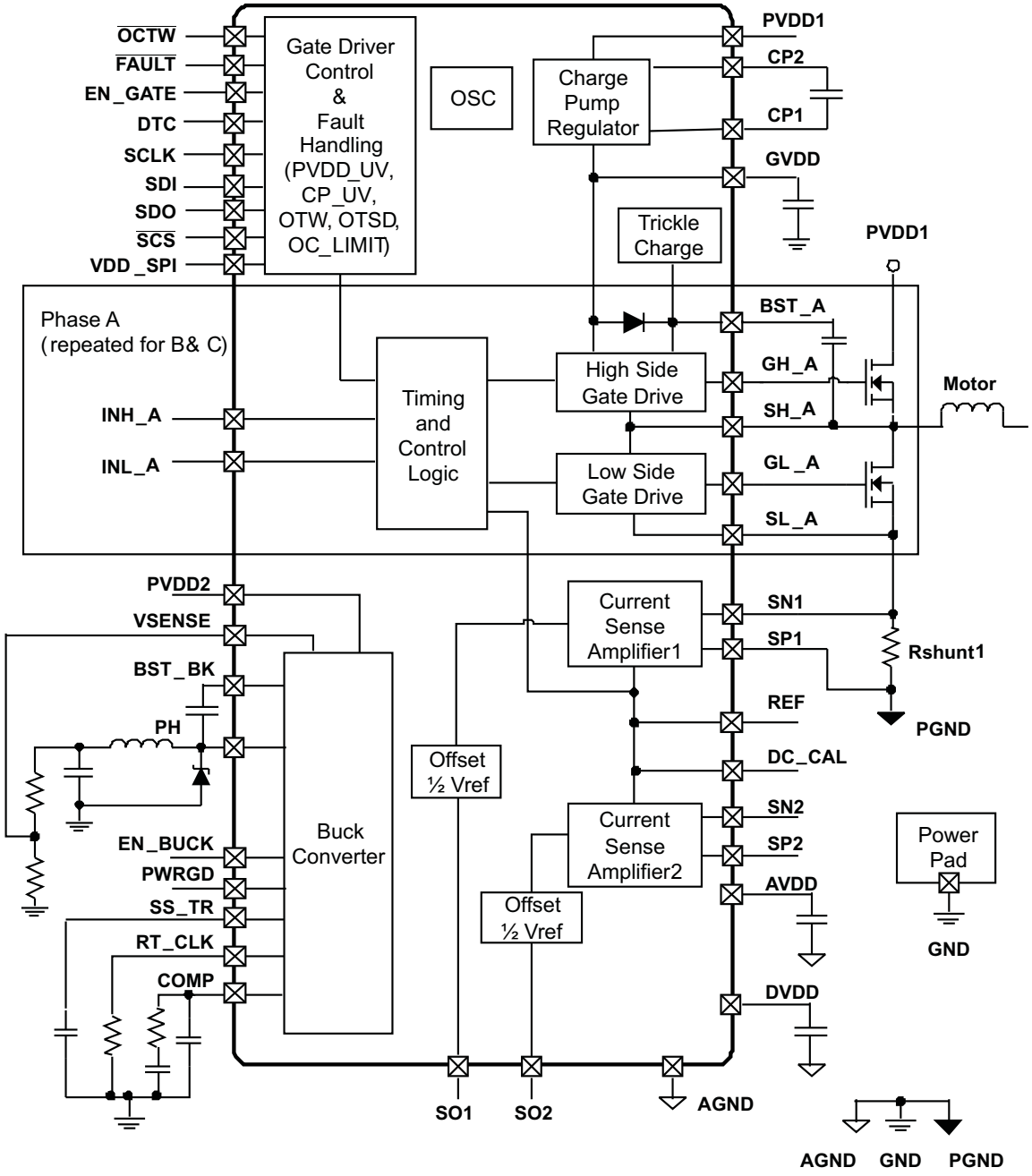
PIN		I/O(1)	DESCRIPTION
NAME	NO.		
RT_CLK	1	I	Resistor timing and external clock for buck regulator. Resistor should connect to GND (power pad) with very short trace to reduce the potential clock jitter due to noise.
COMP	2	O	Buck error amplifier output and input to the output switch current comparator.
VSENSE	3	I	Buck output voltage sense pin. Inverting node of error amplifier.
PWRGD	4	I	An open drain output with external pull-up resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, over-voltage, or EN_BUCK shut down
$\overline{\text{OCTW}}$	5	O	Over current or/and over temperature warning indicator. This output is open drain with external pull-up resistor required. Programmable output mode via SPI registers.
$\overline{\text{FAULT}}$	6	O	Fault report indicator. This output is open drain with external pull-up resistor required.
DTC	7	I	Dead-time adjustment with external resistor to GND
$\overline{\text{SCS}}$	8	I	SPI chip select
SDI	9	I	SPI input
SDO	10	O	SPI output
SCLK	11	I	SPI clock signal
DC_CAL	12	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can be done through external microcontroller.
GVDD	13	P	Internal gate driver voltage regulator. GVDD cap should connect to GND
CP1	14	P	Charge pump pin 1, ceramic cap should be used between CP1 and CP2
CP2	15	P	Charge pump pin 2, ceramic cap should be used between CP1 and CP2
EN_GATE	16	I	Enable gate driver and current shunt amplifiers. Control buck via EN_BUCK pin.
INH_A	17	I	PWM Input signal (high side), half-bridge A
INL_A	18	I	PWM Input signal (low side), half-bridge A
INH_B	19	I	PWM Input signal (high side), half-bridge B
INL_B	20	I	PWM Input signal (low side), half-bridge B
INH_C	21	I	PWM Input signal (high side), half-bridge C
INL_C	22	I	PWM Input signal (low side), half-bridge C
DVDD	23	P	Internal 3.3V supply voltage. DVDD cap should connect to AGND. This is an output, but not specified to drive external circuitry.
REF	24	I	Reference voltage to set output of shunt amplfiiers with a bias voltage which equals to half of the voltage set on this pin. Connect to ADC reference in microcontroller.
SO1	25	O	Output of current amplifier 1
SO2	26	O	Output of current amplifier 2
AVDD	27	P	Internal 6V supply voltage, AVDD cap should always be installed and connected to AGND. This is an output, but not specified to drive external circuitry.
AGND	28	P	Analog ground pin
PVDD1	29	P	Power supply pin for gate driver, current shunt amplifier, and SPI communication. PVDD1 is independent of buck power supply, PVDD2. PVDD1 cap should connect to GND
SP2	30	I	Input of current amplifier 2 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best commom mode rejection.
SN2	31	I	Input of current amplifier 2 (connecting to negative input of amplifier).
SP1	32	I	Input of current amplifier 1 (connecting to positive input of amplifier). Recommend to connect to ground side of the sense resistor for the best commom mode rejection.
SN1	33	I	Input of current amplifier 1 (connecting to negative input of amplifier).
SL_C	34	I	Low-Side MOSFET source connection, half-bridge C. Low-side V_{DS} measured between this pin and SH_C.
GL_C	35	O	Gate drive output for Low-Side MOSFET, half-bridge C
SH_C	36	I	High-Side MOSFET source connection, half-bridge C. High-side V_{DS} measured between this pin and PVDD1.
GH_C	37	O	Gate drive output for High-Side MOSFET, half-bridge C

(1) KEY: I =Input, O = Output, P = Power

PIN FUNCTIONS (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
BST_C	38	P	Bootstrap cap pin for half-bridge C
SL_B	39	I	Low-Side MOSFET source connection, half-bridge B. Low-side V_{DS} measured between this pin and SH_B.
GL_B	40	O	Gate drive output for Low-Side MOSFET, half-bridge B
SH_B	41	I	High-Side MOSFET source connection, half-bridge B. High-side V_{DS} measured between this pin and PVDD1.
GH_B	42	O	Gate drive output for High-Side MOSFET, half-bridge B
BST_B	43	P	Bootstrap cap pin for half-bridge B
SL_A	44	I	Low-Side MOSFET source connection, half-bridge A. Low-side V_{DS} measured between this pin and SH_A.
GL_A	45	O	Gate drive output for Low-Side MOSFET, half-bridge A
SH_A	46	I	High-Side MOSFET source connection, half-bridge A. High-side V_{DS} measured between this pin and PVDD1.
GH_A	47	O	Gate drive output for High-Side MOSFET, half-bridge A
BST_A	48	P	Bootstrap cap pin for half-bridge A
VDD_SPI	49	I	SPI supply pin to support 3.3V or 5V logic. Connect to either 3.3V or 5V.
PH	50, 51	O	The source of the internal high side MOSFET of buck converter
BST_BK	52	P	Bootstrap cap pin for buck converter
PVDD2	53,54	P	Power supply pin for buck converter, PVDD2 cap should connect to GND.
EN_BUCK	55	I	Enable buck converter. Internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors
SS_TR	56	I	Buck soft-start and tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. Cap should connect to GND
GND (POWER PAD)	57	P	GND pin. The exposed power pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

			VALUE		UNITS
			MIN	MAX	
PVDD	Supply voltage range including transient	Relative to PGND	–0.3	70	V
$PVDD_{RAMP}$	Maximum supply voltage ramp rate	Voltage rising up to $PVDD_{MAX}$		1	V/µs
V_{PGND}	Maximum voltage between PGND and GND		±0.3		V
I_{IN_MAX}	Maximum current, all digital and analog input pins except $\overline{FAULT}$ and $\overline{OCTW}$ pins		±1		mA
$I_{IN\_OD\_MAX}$	Maximum sinking current for open drain pins ($\overline{FAULT}$ and $\overline{OCTW}$ Pins)		7		mA
V_{OPA_IN}	Voltage range for SPx and SNx pins		±0.6		V
V_{LOGIC}	Input voltage range for logic/digital pins (INH_A, INL_A, INH_B, INL_B, INH_C, INL_C, EN_GATE, SCLK, SDI, SCS, DC_CAL)		-0.3	7	V
V_{GVDD}	Maximum voltage for GVDD Pin		13.2		V
V_{AVDD}	Maximum voltage for AVDD Pin		8		V
V_{DVDD}	Maximum voltage for DVDD Pin		3.6		V
V_{VDD_SPI}	Maximum voltage for VDD_SPI Pin		7		V
V_{SDO}	Maximum voltage for SDO Pin		VDD_SPI +0.3		V
V_{REF}	Maximum reference voltage for current amplifier		7		V
I_{REF}	Maximum current for REF Pin		100		µA
T_J	Maximum operating junction temperature range		–40	150	°C
$T_{STORAGE}$	Storage temperature range		–55	150	°C
	Capacitive discharge model		Per AEC-Q100		
	Human body model		Per AEC-Q100		

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8301-Q1 DCA 56 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	30.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	33.5	
θ_{JB}	Junction-to-board thermal resistance(4)	17.5	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	7.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNITS
PVDD1	DC supply voltage PVDD1 for normal operation	Relative to PGND	6		60	V
PVDD2	DC supply voltage PVDD2 for buck converter		3.5		60	V
C_{PVDD1}	External capacitance on PVDD1 pin (ceramic cap) 20% tolerance			4.7		µF
C_{PVDD2}	External capacitance on PVDD2 pin (ceramic cap) 20% tolerance			4.7		µF
C_{AVDD}	External capacitance on AVDD pin (ceramic cap) 20% tolerance			1		µF
C_{DVDD}	External capacitance on DVDD pin (ceramic cap) 20% tolerance			1		µF
C_{GVDD}	External capacitance on GVDD pin (ceramic cap) 20% tolerance			2.2		µF
C_{CP}	Flying cap on charge pump pins (between CP1 and CP2) (ceramic cap) 20% tolerance			22		nF
C_{BST}	Bootstrap cap (ceramic cap)			100		nF
I_{DIN_EN}	Input current of digital pins when EN_GATE is high				100	µA
I_{DIN_DIS}	Input current of digital pins when EN_GATE is low				1	µA
C_{DIN}	Maximum capacitance on digital input pin				10	pF
C_{O_OPA}	Maximum output capacitance on outputs of shunt amplifier				20	pF
R_{DTC}	Dead time control resistor range. Time range is 50ns (-GND) to 500ns (150kΩ) with a linear approximation.		0		150	kΩ
I_{FAULT}	$\overline{FAULT}$ pin sink current. Open-drain	V = 0.4 V			2	mA
I_{OCTW}	$\overline{OCTW}$ pin sink current. Open-drain	V = 0.4 V			2	mA
V_{REF}	External voltage reference voltage for current shunt amplifiers		2		6	V
f_{gate}	Operating switching frequency of gate driver	Qg(TOT) = 25 nC or total 30 mA gate drive average current			200	kHz
I_{gate}	Total average gate drive current				30	mA
T_A	Ambient temperature		–40		125	°C

ELECTRICAL CHARACTERISTICS

PVDD = 6 V to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT PINS: INH_X, INL_X, M_PWM (SCS), M_OC (SDI), GAIN(SDO), EN_GATE, DC_CAL						
V_{IH}	High input threshold		2			V
V_{IL}	Low input threshold				0.8	V
R_{EN_GATE}	Internal pull down resistor for EN_GATE			100		kΩ
R_{INH_X}	Internal pull down resistor for high side PWMs (INH_A, INH_B, and INH_C)	EN_GATE high		100		kΩ
R_{INH_X}	Internal pull down resistor for low side PWMs (INL_A, INL_B, and INL_C)	EN_GATE high		100		kΩ
R_{SCS}	Internal pull down resistor for $\overline{SCS}$	EN_GATE high		100		kΩ
R_{SDI}	Internal pull down resistor for SDI	EN_GATE high		100		kΩ
R_{DC_CAL}	Internal pull down resistor for DC_CAL	EN_GATE high		100		kΩ
R_{SCLK}	Internal pull down resistor for SCLK	EN_GATE high		100		kΩ
OUTPUT PINS: $\overline{FAULT}$ AND $\overline{OCTW}$						
V_{OL}	Low output threshold	I_O = 2 mA			0.4	V
V_{OH}	High output threshold	External 47 kΩ pull up resistor connected to 3-5.5 V	2.4			V
I_{OH}	Leakage Current on Open Drain Pins When Logic High ($\overline{FAULT}$ and $\overline{OCTW}$)				1	µA

ELECTRICAL CHARACTERISTICS (continued)

PVDD = 6 V to 60 V, T_C = 25°C, unless specified under test condition

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE OUTPUT: GH_A, GH_B, GH_C, GL_A, GL_B, GL_C						
V_{GX_NORM}	Gate driver Vgs voltage	PVDD = 8V–60V, I_{gate} = 30mA, C_{CP} = 22nF	9.5		11.5	V
		PVDD = 8V–60V, I_{gate} = 30mA, C_{CP} = 220nF	9.5		11.5	
V_{GX_MIN}	Gate driver Vgs voltage	PVDD = 6V–8V, I_{gate} = 15mA, C_{CP} = 22nF	8.8			V
		PVDD = 6V–8V, I_{gate} = 30mA, C_{CP} = 220nF	8.3			
I_{oso1}	Maximum source current setting 1, peak	Vgs of FET equals to 2 V. REG 0x02		1.7		A
I_{osi1}	Maximum sink current setting 1, peak	Vgs of FET equals to 8 V. REG 0x02		2.3		A
I_{oso2}	Source current setting 2, peak	Vgs of FET equals to 2 V. REG 0x02		0.7		A
I_{osi2}	Sink current setting 2, peak	Vgs of FET equals to 8 V. REG 0x02		1		A
I_{oso3}	Source current setting 3, peak	Vgs of FET equals to 2 V. REG 0x02		0.25		A
I_{osi3}	Sink current setting 3, peak	Vgs of FET equals to 8 V. REG 0x02		0.5		A
R_{gate_off}	Gate output impedence during standby mode when EN_GATE low (pins GH_x, GL_x)		1.6		2.4	kΩ
SUPPLY CURRENTS						
I_{PVDD1_STB}	PVDD1 supply current, standby	EN_GATE is low. PVDD1 = 8V.		20	50	µA
I_{PVDD1_OP}	PVDD1 supply current, operating	EN_GATE is high, no load on gate drive output, switching at 10 kHz, 100 nC gate charge		15		mA
I_{PVDD1_HIZ}	PVDD1 Supply current, HiZ	EN_GATE is high, gate not switching	2	5	10	mA
INTERNAL REGULATOR VOLTAGE						
A_{VDD}	AVDD voltage	PVDD = 8V - 60V	6	6.5	7	V
		PVDD = 6V - 60V	5.5		6	
D_{VDD}	DVDD voltage		3	3.3	3.6	V
VOLTAGE PROTECTION						
V_{PVDD_UV}	Under voltage protection limit, PVDD	PVDD falling			5.9	V
		PVDD rising			6	
V_{GVDD_UV}	Under voltage protection limit, GVDD	GVDD falling			7.5	V
V_{GVDD_OV}	Over voltage protection limit, GVDD			16		V
CURRENT PROTECTION, (VDS SENSING)						
V_{DS_OC}	Drain-source voltage protection limit	PVDD = 8V - 60V	0.125		2.4	V
		PVDD = 6V - 8V (1)	0.125		1.491	
T_{oc}	OC sensing response time			1.5		µs
T_{OC_PULSE}	$\overline{OCTW}$ pin reporting pulse stretch length for OC event			64		µs

(1) Reduced A_{VDD} voltage range results in limitations on settings for over current protection. See Table 10.

GATE TIMING AND PROTECTION CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING, OUTPUT PINS						
$t_{pd,lf-O}$	Positive input falling to GH_x falling	CL=1nF, 50% to 50%		45		ns
$t_{pd,lr-O}$	Positive input rising to GL_x falling	CL=1nF, 50% to 50%		45		ns
T_{d_min}	Minimum dead time after hand shaking (1)				50	ns
T_{dtp}	Dead Time	With R_{DTC} set to different values	50		500	ns
t_{GDr}	Rise time, gate drive output	CL=1nF, 10% to 90%		25		ns
t_{GDF}	Fall time, gate drive output	CL=1nF, 90% to 10%		25		ns
T_{ON_MIN}	Minimum on pulse	Not including handshake communication. Hiz to on state, output of gate driver			50	ns
T_{pd_match}	Propagation delay matching between high side and low side				5	ns
T_{dt_match}	Deadtime matching				5	ns
TIMING, PROTECTION AND CONTROL						
$t_{pd,R\_GATE-OP}$	Start up time, from EN_GATE active high to device ready for normal operation	PVDD is up before start up, all charge pump caps and regulator caps as in recommended condition		5	10	ms
$t_{pd,R\_GATE-Quick}$	If EN_GATE goes from high to low and back to high state within quick reset time, it will only reset all faults and gate driver without powering down charge pump, current amp, and related internal voltage regulators.	Maximum low pulse time			10	us
$t_{pd,E-L}$	Delay, error event to all gates low			200		ns
$t_{pd,E-FAULT}$	Delay, error event to $\overline{FAULT}$ low			200		ns
OTW_CLR	Junction temperature for resetting over temperature warning			115		°C
OTW_SET/OTSD_CLR	Junction temperature for over temperature warning and resetting over temperature shut down			130		°C
OTSD_SET	Junction temperature for over temperature shut down		150			°C

(1) Dead time programming definition: Adjustable delay from GH_x falling edge to GL_X rising edge, and GL_X falling edge to GH_X rising edge. This is a minimum dead-time insertion. It is not added to the value set by the microcontroller externally.

CURRENT SHUNT AMPLIFIER CHARACTERISTICS

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G1	Gain option 1	Tc = -40°C-125°C	9.5	10	10.5	V/V
G2	Gain option 2	Tc = -40°C-125°C	18	20	21	V/V
G3	Gain Option 3	Tc = -40°C-125°C	38	40	42	V/V
G4	Gain Option 4	Tc = -40°C-125°C	75	80	85	V/V
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 10, Vstep = 2 V		300		ns
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 20, Vstep = 2 V		600		ns
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 40, Vstep = 2 V		1.2		µs
Tsettling	Settling time to 1%	Tc = 0-60°C, G = 80, Vstep = 2 V		2.4		µs
Vswing	Output swing linear range		0.3		5.7	V
Slew Rate		G = 10		10		V/µs
DC_offset	Offset error RTI	G = 10 with input shorted			4	mV
Drift_offset	Offset drift RTI			10		µV/C
Ibias	Input bias current				100	µA
Vin_com	Common input mode range		–0.15		0.15	V
Vin_dif	Differential input range		–0.3		0.3	V
Vo_bias	Output bias	With zero input current, Vref up to 6 V	–0.5%	0.5×Vref	0.5%	V
CMRR_OV	Overall CMRR with gain resistor mismatch	CMRR at DC, gain = 10	70	85		dB

BUCK CONVERTER CHARACTERISTICS

T_C = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
$I_{SD(PVDD2)}$	Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 60 V		1.3	4	µA
$I_{NON\_SW(PVDD2)}$	Operating: nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V		116	136	µA
V_{EN_BUCK}	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
R_{DS_ON}	On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
I_{LIM}	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
F_{sw}	Switching frequency	RT = 200 kΩ	450	581	720	kHz
PWRGD	VSENSE threshold	VSENSE falling		92%		
		VSENSE rising		94%		
		VSENSE rising		109%		
		VSENSE falling		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω

SPI CHARACTERISTICS (Slave Mode Only)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SPI_READY}	SPI ready after EN_GATE transitions to HIGH	PVDD > 6 V		5	10	ms
t_{CLK}	Minimum SPI clock period		100			ns
t_{CLKH}	Clock high time		40			
t_{CLKL}	Clock low time		40			
t_{SU_SDI}	SDI input data setup time		20			ns

SPI CHARACTERISTICS (Slave Mode Only) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HD_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time, CLK high to SDO valid	C_L = 20 pF			20	ns
t_{HD_SDO}	SDO output data hold time		40			
t_{SU_SCS}	SCS setup time		50			ns
t_{HD_SCS}	SCS hold time		50			ns
t_{HI_SCS}	SCS minimum high time before SCS active low		40			ns
t_{ACC}	SCS access time, SCS low to SDO out of high impedance			10		ns
t_{DIS}	SCS disable time, SCS high to SDO high impedance			10		ns

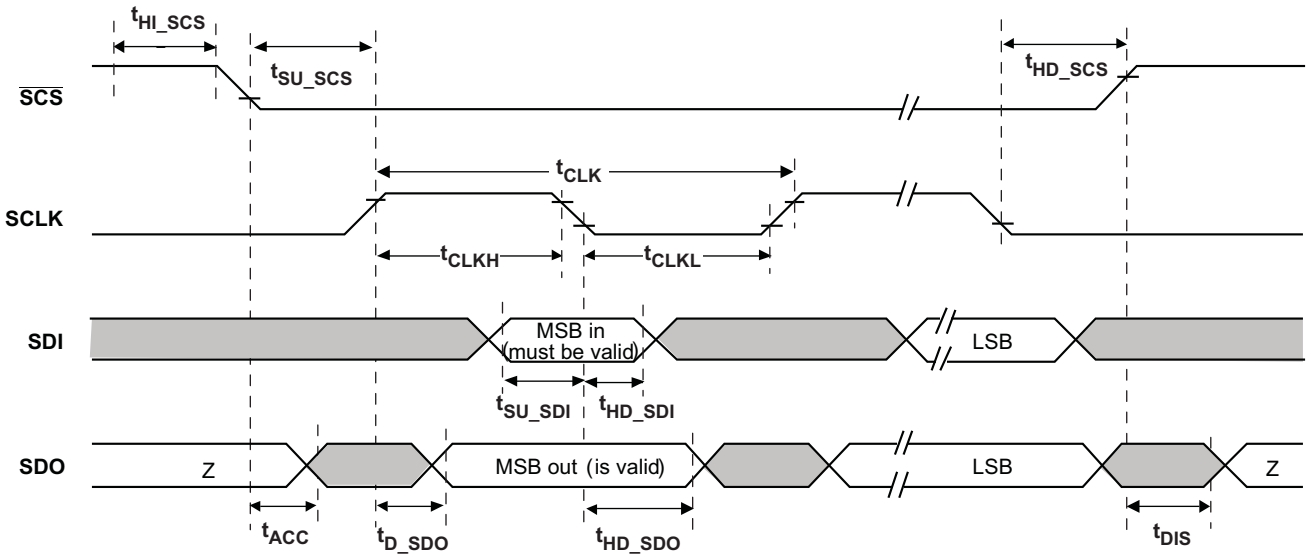


Figure 2. SPI Slave Mode Timing Definition

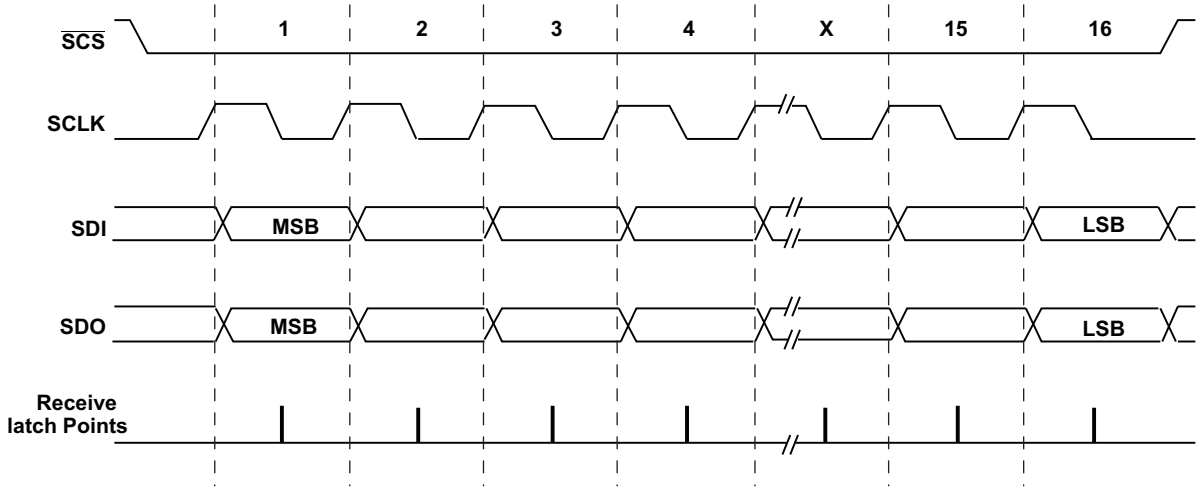


Figure 3. SPI Slave Mode Timing Diagram

FUNCTIONAL DESCRIPTION

THREE-PHASE GATE DRIVER

The DRV8301-Q1 provides three half bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low side.

Gate driver has following features:

- Internal hand shake between high side and low side FETs during switching transition to prevent current shoot through.
- Programmable slew rate or current driving capability through SPI interface.
- Support up to 200kHz switching frequency with Qg(TOT)=25nC or total 30mA gate drive average current
- Provide cycle-by-cycle current limiting and latch over-current (OC) shut down of external FETs. Current is sensed through FET drain-to-source voltage and the over-current level is programmable through SPI interface
- Vds sensing range is programmable from 0.060V to 2.4V and with 5 bit programmable resolution through SPI.
- High side gate drive will survive negative output from half bridge up to –10V for 10ns
- During EN_GATE pin low and fault conditions, gate driver will keep external FETs in high impedance mode.
- Programmable dead time through DTC pin. Dead time control range: 50ns to 500ns. Short DTC pin to ground will provide minimum dead time (50ns). External dead time will override internal dead time as long as the time is longer than the dead time setting (minimum hand shake time cannot be reduced in order to prevent shoot through current).
- Bootstraps are used in high side FETs of three-phase pre-gate driver. Trickle charge circuitry is used to replenish current leakage from bootstrap cap and support 100% duty cycle operation.

CURRENT SHUNT AMPLIFIERS

The DRV8301-Q1 includes two high performance current shunt amplifiers for accurate current measurement. The current amplifiers provide output offset up to 3V to support bi-directional current sensing.

Current shunt amplifier has following features:

- Programmable gain: 4 gain settings through SPI command
- Programmable output offset through reference pin (half of the Vref)
- Minimize DC offset and drift over temperature with dc calibrating through SPI command or DC_CAL pin. When DC calibration is enabled, device will short input of current shunt amplifier and disconnect the load. DC calibrating can be done at anytime even when FET is switching since the load is disconnected. For best result, perform the DC calibrating during switching off period when no load is present to reduce the potential noise impact to the amplifier.

The output of current shunt amplifier can be calculated as:

$$V_O = \frac{V_{REF}}{2} - G \times (SN_X - SP_X) \quad (1)$$

Where Vref is the reference voltage, G is the gain of the amplifier; SNx and SPx are the inputs of channel x. SPx should connect to resistor ground for the best common mode rejection.

Figure 4 shows current amplifier simplified block diagram.

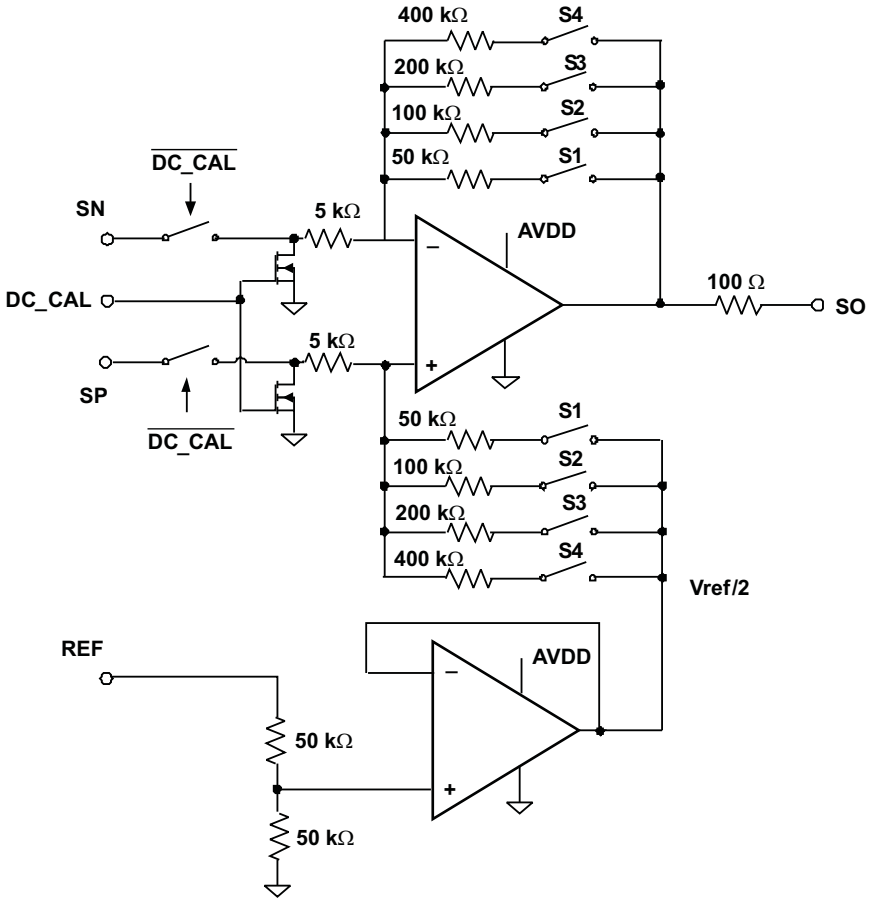


Figure 4. Current Shunt Amplifier Simplified Block Diagram

BUCK CONVERTER

The buck converter in the DR8301 is the same as the TPS54160 buck converter. Although integrated in the same device, buck converter is designed completely independent of rest of the gate driver circuitry. Since buck will support external MCU or other external power need, the independency of buck operation is very critical for a reliable system; this will give buck minimum impact from gate driver operations. Some examples are: when gate driver shuts down due to any failure, buck will still operate unless the fault is coming from buck itself. The buck keeps operating at much lower PVDD of 3.5V, this will assure the system to have a smooth power up and power down sequence when gate driver is not able to operate due to a low PVDD.

The buck has an integrated high side n-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The wide switching frequency of 300kHz to 2200kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT_CLK pin. The device has an internal phase lock loop (PLL) on the RT_CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The buck converter has a default start up voltage of approximately 2.5V. The EN_BUCK pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) threshold with two external resistors. In addition, the pull up current provides a default condition. When the EN_BUCK pin is floating the device will operate. The operating current is 116µA when not switching and under no load. When the device is disabled, the supply current is 1.3µA.

The integrated 200mΩ high side MOSFET allows for high efficiency power supply designs capable of delivering 1.5 amperes of continuous current to a load. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The buck can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8V reference.

The BUCK has a power good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pull-up resistor is used.

The BUCK minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power good comparator. When the OV comparator is activated, the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS_TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow start time. A resistor divider can be coupled to the pin for critical power supply sequencing requirements. The SS_TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault,

The BUCK, also, discharges the slow start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit will slow start the output from the fault voltage to the nominal regulation voltage once a fault condition is removed. A frequency foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

PROTECTION FEATURES

Power Stage Protection

The DRV8301-Q1 provides over-current and under-voltage protection for the MOSFET power stage. During fault shut down conditions, all gate driver outputs will be kept low to ensure external FETs at high impedance state.

Over-Current Protection (OCP) and Reporting

To protect the power stage from damage due to high currents, a V_{DS} sensing circuitry is implemented in the DRV8301-Q1. Based on $R_{DS(on)}$ of the power MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be calculated which, when exceeded, triggers the OC protection feature. This voltage threshold level is programmable through SPI command.

There are total 4 OC_MODE settings in SPI.

1. Current Limit Mode

   When current limit mode is enabled, device operates current limiting instead of OC shut down during OC event. The over-current event is reported through $\overline{\text{OCTW}}$ pin. $\overline{\text{OCTW}}$ reporting should hold low during same PWM cycle or for a max 64µs period (internal timer) so external controller has enough time to sample the warning signal. If in the middle of reporting, other FET(s) gets OC, then OCTW reporting will hold low and recount another 64µS unless PWM cycles on both FETs are ended.

   There are two current control settings in current limit mode (selected by one bit in SPI and default is CBC mode).
   - Setting 1 (CBC mode): during OC event, the FET that detected OC will turn off until next PWM cycle.
   - Setting 2 (off-time control mode):
     - During OC event, the FET that detected OC will turn off for 64us as off time and back to normal after that (so same FET will be on again) if PWM signal is still holding high. Since all three phases or 6 FETs share a single timer, if more than one FET get OC, the FETs will not be back to normal until the all FETs that have OC event pass 64µs.
     - If PWM signal is toggled for this FET during timer running period, device will resume normal operation for this toggled FET. So real off-time could be less than 64uS in this case.
     - If two FETs get OC and one FET's PWM signal gets toggled during timer running period, this FET will be back to normal, and the other FET will be off till timer end (unless its PWM is also toggled)

2. OC latch shut down mode

   When OC occurs, device will turn off both high side and low side FETs in the same phase if any of the FETs in that phase has OC.

3. Report only mode

   No protection action will be performance in this mode. OC detection will be reported through OCTW pin and SPI status register. External MCU should take actions based on its own control algorithm. A pulse stretching of 64µS will be implemented on OCTW pin so controller can have enough time to sense the OC signal.

4. OC disable mode

   Device will ignore all the OC detections and will not report them either.

Under-Voltage Protection (UVP)

To protect the power output stage during startup, shutdown and other possible under-voltage conditions, the DRV8301-Q1 provides power stage under-voltage protection by driving its outputs low whenever PVDD is below 6V (PVDD_UV) or GVDD is below 7.5V (GVDD_UV). When UVP is triggered, the DRV8301-Q1 outputs are driven low and the external MOSFETs will go to a high impedance state.

Over-Voltage Protection (GVDD_OV)

Device will shut down both gate driver and charge pump if GVDD voltage exceeds 16V to prevent potential issue related to GVDD or charge pump (e.g. short of external GVDD cap or charge pump). The fault is a latched fault and can only be reset through a transition on EN_GATE pin.

Over-Temperature Protection

A two-level over-temperature detection circuit is implemented:

- Level 1: over temperature warning (OTW)
  OTW is reported through $\overline{\text{OCTW}}$ pin (over-current-temperature warning) for default setting. OCTW pin can be set to report OTW or OCW only through SPI command. See SPI Register section.
- Level 2: over temperature (OT) latched shut down of gate driver and charge pump (OTSD_GATE)
  Fault will be reported to $\overline{\text{FAULT}}$ pin. This is a latched shut down, so gate driver will not be recovered automatically even OT condition is not present anymore. An EN_GATE reset through pin or SPI (RESET_GATE) is required to recover gate driver to normal operation after temperature goes below a preset value, t_{OTSD_CLR}.

SPI operation is still available and register settings will be remaining in the device during OTSD operation as long as PVDD is still within defined operation range.

Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event with shut down has occurred such as over-current, over-temperature, over-voltage, or under-voltage. Note that $\overline{\text{FAULT}}$ is an open-drain signal. $\overline{\text{FAULT}}$ will go high when gate driver is ready for PWM signal (internal EN_GATE goes high) during start up.

The $\overline{\text{OCTW}}$ pin indicates over current event and over temperature event that not necessary related to shut down.

Following is the summary of all protection features and their reporting structure:

Table 1. Fault and Warning Reporting and Handling

EVENT	ACTION	LATCH	REPORTING ON $\overline{\text{FAULT}}$ PIN	REPORTING ON $\overline{\text{OCTW}}$ PIN	REPORTING IN SPI STATUS REGISTER
PVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output	N	Y	N	Y
DVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output; When recovering, reset all status registers	N	Y	N	N
GVDD undervoltage	External FETs HiZ; Weak pull down of all gate driver output	N	Y	N	Y
GVDD overvoltage	External FETs HiZ; Weak pull down of all gate driver output Shut down the charge pump Won't recover and reset through SPI reset command or quick EN_GATE toggling	Y	Y	N	Y
OTW	None	N	N	Y (in default setting)	Y
OTSD_GATE	Gate driver latched shut down. Weak pull down of all gate driver output to force external FETs HiZ Shut down the charge pump	Y	Y	Y	Y
OTSD_BUCK	OTSD of Buck	Y	N	N	N
Buck output undervoltage	UVLO_BUCK: auto-restart	N	Y, in PWRGD pin	N	N
Buck overload	Buck current limiting (HiZ high side until current reaches zero and then auto-recovering)	N	N	N	N
External FET overload – current limit mode	External FETs current Limiting (only OC detected FET)	N	N	Y	Y, indicates which phase has OC
External FET overload – Latch mode	Weak pull down of gate driver output and PWM logic "0" of LS and HS in the same phase. External FETs HiZ	Y	Y	Y	Y
External FET overload – reporting only mode	Reporting only	N	N	Y	Y, indicates which phase has OC

PIN CONTROL FUNCTIONS

Table 2. Device Truth Table

INH_X	INL_X	GH_X	GL_X
1	1	L	L
1	0	H	L
0	1	L	H
0	0	L	L

EN_GATE

EN_GATE low is used to put gate driver, charge pump, current shunt amplifier, and internal regulator blocks into a low power consumption mode to save energy. SPI communication is not supported during this state. Device will put the MOSFET output stage to high impedance mode as long as PVDD is still present.

When EN_GATE pin goes to high, it will go through a power up sequence, and enable gate driver, current amplifiers, charge pump, internal regulator, etc and reset all latched faults related to gate driver block. It will also reset status registers in SPI table. All latched faults can be reset when EN_GATE is toggled after an error event unless the fault is still present.

When EN_GATE goes from high to low, it will shut down gate driver block immediately, so gate output can put external FETs in high impedance mode. It will then wait for 10us before completely shutting down the rest of the blocks. A quick fault reset mode can be done by toggling EN_GATE pin for a very short period (less than 10µS). This will prevent device to shut down other function blocks such as charge pump and internal regulators and bring a quicker and simple fault recovery. SPI will still function with such a quick EN_GATE reset mode.

The other way to reset all the faults is to use SPI command (RESET_GATE), which will only reset gate driver block and all the SPI status registers without shutting down other function blocks.

One exception is to reset a GVDD_OV fault. A quick EN_GATE quick fault reset or SPI command reset won't work with GVDD_OV fault. A complete EN_GATE with low level holding longer than 10µS is required to reset GVDD_OV fault. It is highly recommended to inspect the system and board when GVDD_OV occurs.

EN_BUCK

Buck enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable.

DTC

Dead time can be programmed through DTC pin. A resistor should be connected from DTC to ground to control the dead time. Dead time control range is from 50ns to 500ns. Short DTC pin to ground will provide minimum dead time (50ns). Resistor range is 0 to 150kΩ. Dead time is linearly set over this resistor range.

Current shoot through prevention protection will be enabled in the device all time independent of dead time setting and input mode setting.

VDD_SPI

VDD_SPI is the power supply to power SDO pin. It has to be connected to the same power supply (3.3V or 5V) that MCU uses for its SPI operation.

During power up or down transient, VDD_SPI pin could be zero voltage shortly. During this period, no SDO signal should be present at SDO pin from any other devices in the system since it causes a parasitic diode in the DRV8301-Q1 conducting from SDO to VDD_SPI pin as a short. This should be considered and prevented from system power sequence design.

DC_CAL

When DC_CAL is enabled, device will short inputs of shunt amplifier and disconnect from the load, so external microcontroller can do a DC offset calibration. DC offset calibration can be also done with SPI command. If using SPI exclusively for DC calibration, the DC_CAL pin can connected to GND.

SPI Pins

SDO pin has to be 3-state, so a data bus line can be connected to multiple SPI slave devices. SCS pin is active low. When SCS is high, SDO is at high impendence mode.

STARTUP AND SHUTDOWN SEQUENCE CONTROL

During power-up all gate drive outputs are held low. Normal operation of gate driver and current shunt amplifiers can be initiated by toggling EN_GATE from a low state to a high state. If no errors are present, the DRV8301-Q1 is ready to accept PWM inputs. Gate driver always has control of the power FETs even in gate disable mode as long as PVDD is within functional region.

There is an internal diode from SDO to VDD_SPI, so VDD_SPI is required to be powered to the same power level as other SPI devices (if there is any SDO signal from other devices) all the time. VDD_SPI supply should be powered up first before any signal appears at SDO pin and powered down after completing all communications at SDO pin.

SPI COMMUNICATION

SPI Interface

SPI interface is used to set device configuration, operating parameters and read out diagnostic information. The DRV8301-Q1 SPI Interface operates in the slave mode.

The SPI input data (SDI) word consists of 16bit word, with 11 bit data and 5 bit (MSB) command. The SPI output data (SDO) word consists of 16bit word, with 11 bit register data and 4 bit MSB address data and 1 frame fault bit (active 1). When a frame is not valid, frame fault bit will set to 1, and rest of SDO bit will shift out zeros.

A valid frame has to meet following conditions:

1. Clock must be low when /SCS goes low.
2. We should have 16 full clock cycles.
3. Clock must be low when /SCS goes high.

When SCS is asserted high, any signals at the SCLK and SDI pins are ignored, and SDO is forced into a high impedance state. When SCS transitions from HIGH to LOW, SDO is enabled and the SPI response word loads into the shift register based on 5 bit command in SPI at previous clock cycle.

The SCLK pin must be low when SCS transitions low. While SCS is low, at each rising edge of the clock, the response bit is serially shifted out on the SDO pin with MSB shifted out first.

While SCS is low, at each falling edge of the clock, the new control bit is sampled on the SDI pin. The SPI command bits are decoded to determine the register address and access type (read or write). The MSB will be shifted in first. If the word sent to SDI is less than 16 bits or more than 16 bits, it is considered a frame error. If it is a write command, the data will be ignored. The fault bit in SDO (MSB) will report 1 at next 16 bit word cycle.

After the 16th clock cycle or when SCS transitions from LOW to HIGH, in case of write access type, the SPI receive shift register data is transferred into the latch where address matches decoded SPI command address value. Any amount of time may pass between bits, as long as SCS stays active low. This allows two 8-bit words to be used.

For a read command (Nth cycle) in SPI, SP0 will send out data in the register with address in read command in next cycle (N+1).

For a write command in SPI, SPO will send out data in the status register 0x00h in next 16 bit word cycle (N+1). For most of the time, this feature will maximize SPI communication efficiency when having a write command, but still get fault status values back without sending extra read command.

SPI Format

SPI input data control word is 16-bit long, consisting of:

- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

SPI output data response word is 16-bit long, and its content depends on the given SPI command (SPI Control Word) in the previous cycle. When a SPI Control Word is shifted in, the SPI Response Word (that is shifted out during the same transition time) is the response to the previous SPI Command (shift in SPI Control Word "N" and shift out SPI Response Word "N-1").

Therefore, each SPI Control / Response pair requires two full 16-bit shift cycles to complete.

Table 3. SPI Input Data Control Word Format

	R/W	Address				Data										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 4. SPI Output Data Response Word Format

	R/W	Data														
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	F0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SPI Control and Status Registers

Read / Write Bit

The MSB bit of SDI word (W0) is read/write bit. When W0 = 0, input data is a write command; when W0 = 1, input data is a read command, and the register value will send out on the same word cycle from SDO from D10 to D0.

Address Bits

Table 5. Register Address

Register Type	Address [A3..A0]				Register Name	Description	Read and Write Access
Status Register	0	0	0	0	Status Register 1	Report occurred faults after previous reading	R (auto reset to default values after read)
	0	0	0	1	Status Register 2	Device ID and report occurred faults after previous reading	Device ID: R Fault report: R (auto reset to default values after read)
Control Register	0	0	1	0	Control Register 1		R/W
	0	0	1	1	Control Register 2		R/W

SPI Data Bits

Status Registers

Table 6. Status Register 1 (Address: 0x00) (all default values are zero)

Address	Register Name	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Status Register 1	FAULT	GVDD_UV	PVDD_UV	OTSD	OTW	FETHA_OC	FETLA_OC	FETHB_OC	FETLB_OC	FETHC_OC	FETLC_OC

Table 7. Status Register 2 (Address: 0x01) (all default values are zero)

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0x01	Status Register 2	GVDD_OV				Device ID			
						0	0	0	0

- All status register bits are in latched mode. Read each status register will reset the bits in this register. Read fault register twice to get an updated status condition.
- EN_GATE toggling with “low” level holding longer than 10µS will force a shut down and start up sequence and reset all values in status registers including GVDD_OV fault.
- EN_GATE toggling (quick fault reset) with low level holding less than 10uS or GATE_RESET high (in SPI) will reset all values in status registers except GVDD_OV fault which will still be latched as a fault.
- FAULT is high when any fault occurs to cause a shut down (GVDD_UV, PVDD_UV, OTSD, OCSD, GVDD_OV), which is opposite to $\overline{\text{FAULT}}$ hardware pin.

Control Registers

Table 8. Control Register 1 for Gate Driver Control (Address: 0x02)(1)

Address	Name	Description	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x02	GATE_CURRENT	Gate driver peak current 1.7A (for slew rate control)										0	0
		Gate driver peak current 0.7A										0	1
		Gate driver peak current 0.25A										1	0
		Reserved										1	1
	GATE_RESET	Normal mode									**0**		
		Reset all latched faults related to gate driver, reset gate driver back to normal operation, reset status register values to default GATE_RESET value will automatically reset to zero after gate driver completes reset									1		
	PWM_MODE	PWM with six independent inputs								**0**			
		PWM with three independent inputs. PWM control high side gates only. Low side is complementary to high side gates with minimum internal dead time.								1			
	OC_MODE (gate driver only)	Current limiting when OC detected						**0**	**0**				
		Latched shut down when OC detected						0	1				
		Report only (no current limiting or shut down) when OC detected						1	0				
		OC protection disabled (no OC sensing and reporting)						1	1				
	OC_ADJ_SET	See OC_ADJ_SET table	X	X	X	X	X						

(1) **Bold** is default value

Table 9. Control Register 2 for Current Shunt Amplifiers and Misc Control (Address: 0x03)(1)

Address	Name	Description	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x03	OCTW_SET	Report both OT and OC at /OCTW pin										**0**	**0**
		Report OT only										0	1
		Report OC only										1	0
		Report OC Only (Reserved)										1	1
	GAIN	Gain of shunt amplifier: 10V/V								**0**	**0**		
		Gain of shunt amplifier: 20V/V								0	1		
		Gain of shunt amplifier: 40V/V								1	0		
		Gain of shunt amplifier: 80V/V								1	1		
	DC_CAL_CH1	Shunt amplifier 1 connects to load through input pins							**0**				
		Shunt amplifier 1 shorts input pins and disconnected from load for external calibration							1				
	DC_CAL_CH2	Shunt amplifier 2 connects to load through input pins						**0**					
		Shunt amplifier 2 shorts input pins and disconnected from load for external calibration						1					
	OC_TOFF	Normal CBC operation (recovering at next PWM cycle)					**0**						
		Off time control during OC					1						
	Reserved												

(1) **Bold** value is default value

Over Current Adjustment

When external MOSFET is turned on, the output current flows the MOSFET, which creates a voltage drop V_{DS}. The overcurrent protection event will be enabled when the V_{DS} exceeds a pre-set value IOC. The OC tripped value can be programmed through SPI command. Assuming the on resistance of MOSFET is $R_{DS(on)}$, the Vds can be calculated as:

$$V_{DS} = I_{OC} \times R_{DS(on)}$$

V_{DS} is measured across the SL_x and SH_x pins for the low-side MOSFET. For the high-side MOSFET, V_{DS} is measured across PVDD1 (internally) and SH_x. Therefore, it is important to limit the ripple on the PVDD1 supply for accurate high-side current sensing.

It is also important to note that there can be up to a 20% tolerance across channels for the OC trip point. This is meant for protection and not to be used for regulating current in a motor phase.

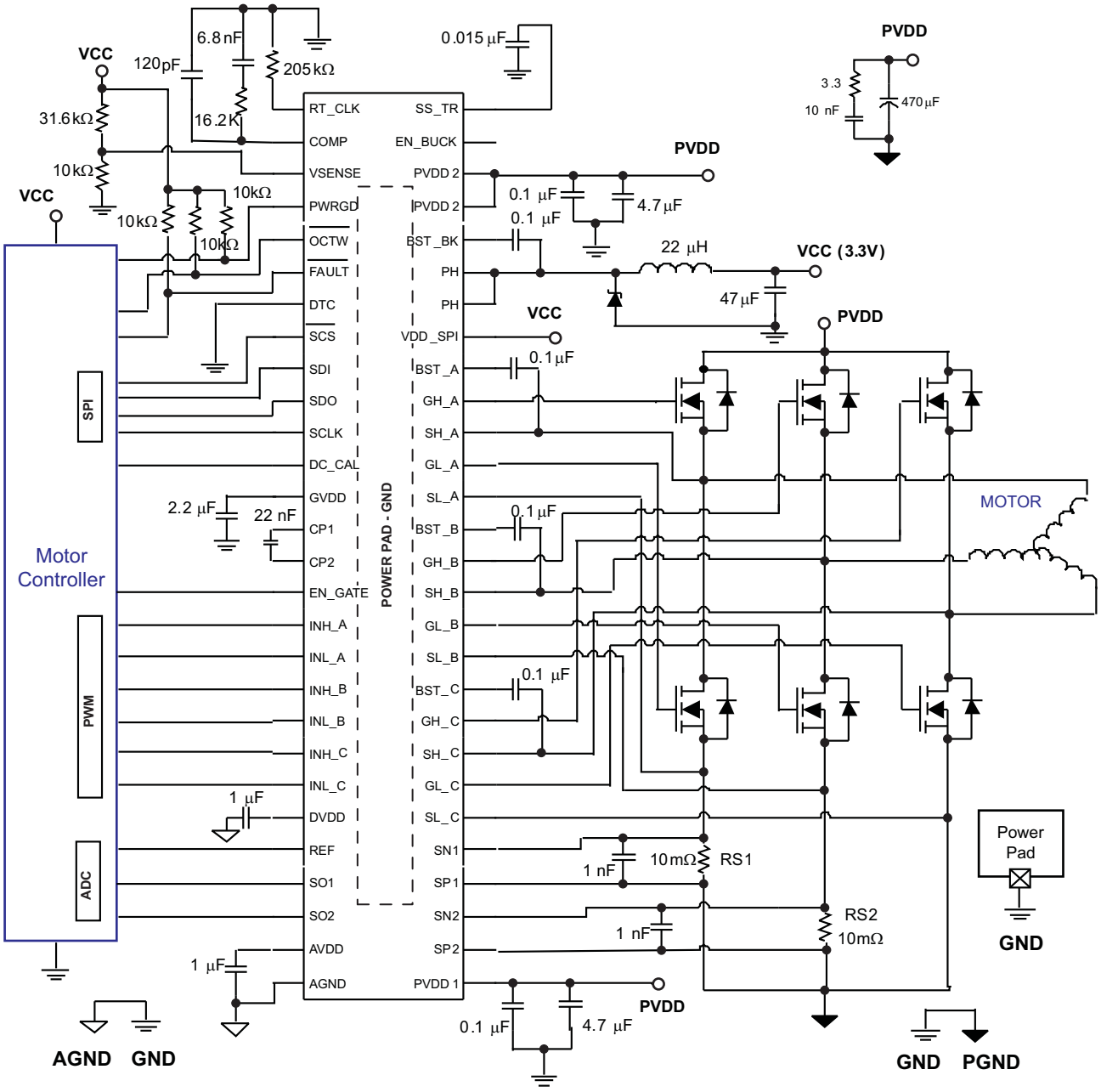
Table 10. OC_ADJ_SET Table

Control Bit (D6–D10) (0xH)	0	1	2	3	4	5	6	7
Vds (V)	0.060	0.068	0.076	0.086	0.097	0.109	0.123	0.138
Control Bit (D6–D10) (0xH)	8	9	10	11	12	13	14	15
Vds (V)	0.155	0.175	0.197	0.222	0.250	0.282	0.317	0.358
Control Bit (D6–D10) (0xH)	16	17	18	19	20	21	22	23
Vds (V)	0.403	0.454	0.511	0.576	0.648	0.730	0.822	0.926
Code Number (0xH)	24	25	26	27	28	29	30	31
Vds (V)	1.043	1.175	1.324	1.491	1.679(1)	1.892(1)	2.131(1)	2.400(1)

(1) Do not use settings 28, 29, 30, 31 for V_{DS} sensing if the IC is expected to operate in the 6V – 8V range.

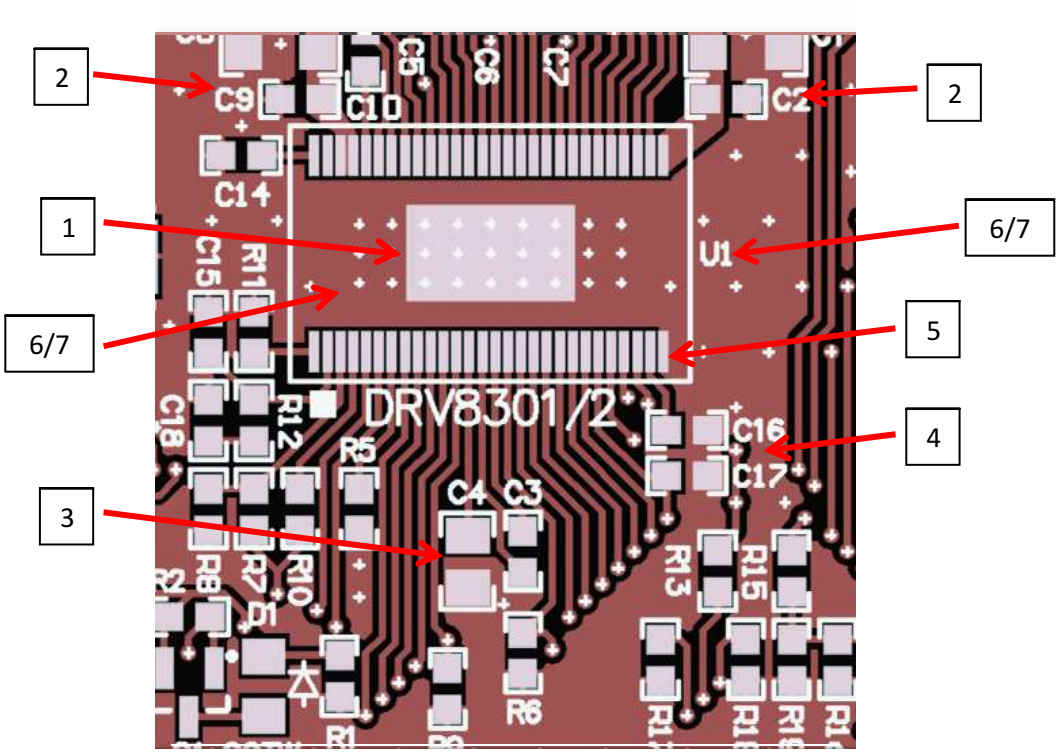
Application Schematic Example

Example:
Buck: PVDD= 3.5V – 40V, Iout_max = 1.5A, Vo = 3.3V, Fs = 570 kHz



PCB LAYOUT RECOMMENDATIONS

Below are a few layout recommendations to utilize when designing a PCB for the DRV8301-Q1.



1. The DRV8301-Q1 makes an electrical connection to GND through the PowerPAD. Always check to ensure that the PowerPAD has been properly soldered (See PowerPAD application report, SLMA002).
2. C1/C2/C8/C9, PVDD decoupling capacitors should be placed close to their corresponding pins with a low impedance path to device GND (PowerPAD).
3. C4, GVDD capacitor should be placed close its corresponding pin with a low impedance path to device GND (PowerPAD).
4. C16/C17, AVDD & DVDD capacitors should be placed close to their corresponding pins with a low impedance path to the AGND pin. It's preferable to make this connection on the same layer.
5. AGND should be tied to device GND (PowerPAD) through a low impedance trace/copper fill.
6. Add stitching vias to reduce the impedance of the GND path from the top to bottom side.
7. Try to clear the space around and underneath the DRV8301-Q1 to allow for better heat spreading from the PowerPAD.

Table 11. Recommended Values

DESIGNATOR	PIN	RECOMMENDED VALUE	DESCRIPTION
C1	PVDD1 – pin 29	2.2uF	CAP CER 2.2UF 100V 10% X7R
C2	PVDD1 – pin 29	0.1uF	CAP CER 0.1UF 100V 10% X7R
C8	PVDD2 – pins 53 & 54	2.2uF	CAP CER 2.2UF 100V 10% X7R
C9	PVDD2 – pins 53 & 54	0.1uF	CAP CER 0.1UF 100V 10% X7R
C4	GVDD – pin 13	2.2uF	CAP CER 2.2UF 25V 10% X7R
C16	AVDD – pin 27	1.0uF	CAP CER 1UF 25V 10% X7R
C17	DVDD – pin 23	1.0uF	CAP CER 1UF 25V 10% X7R

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8301QDCAQ1	NRND	HTSSOP	DCA	56	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q	
DRV8301QDCARQ1	NRND	HTSSOP	DCA	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8301Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

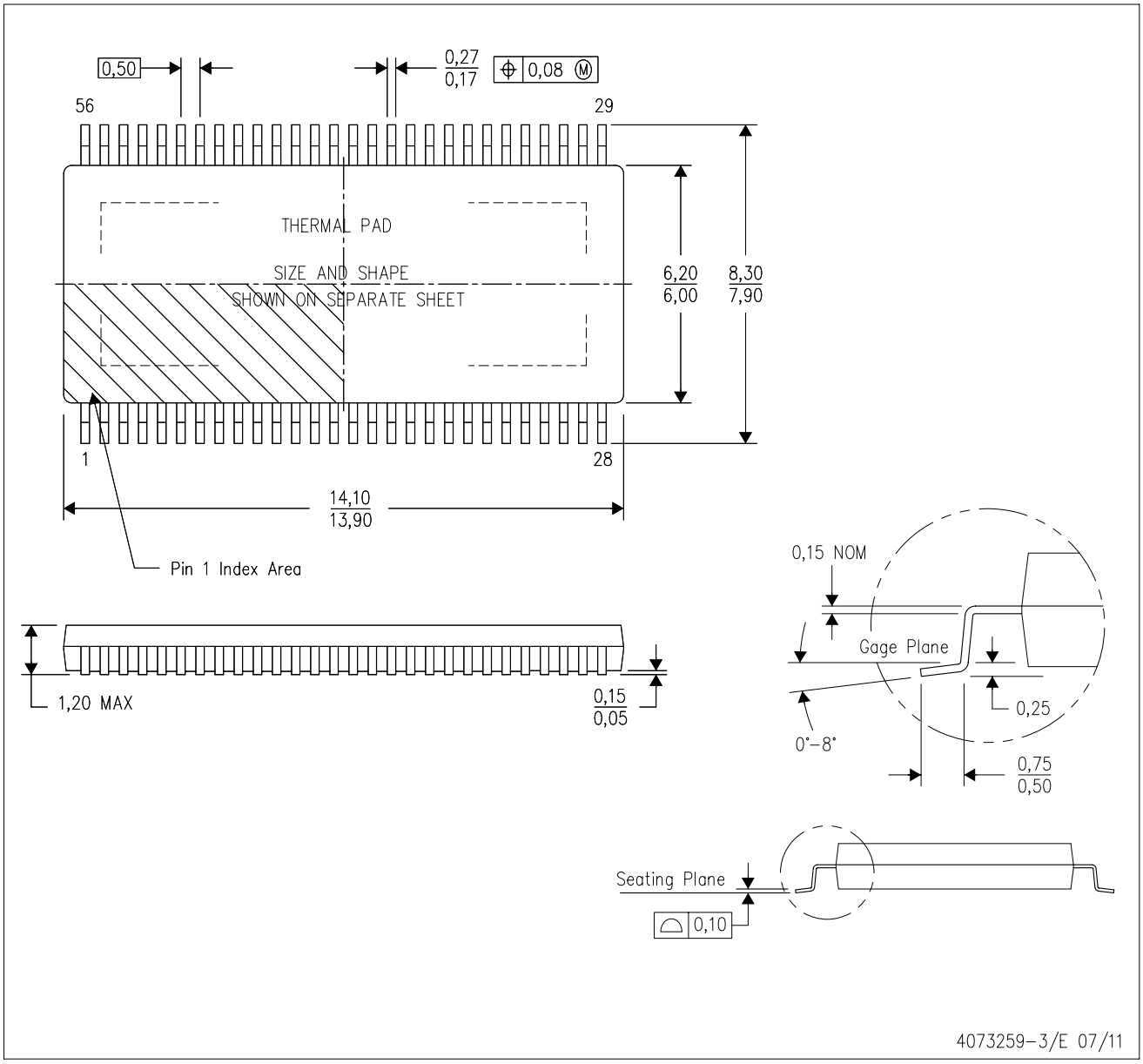
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

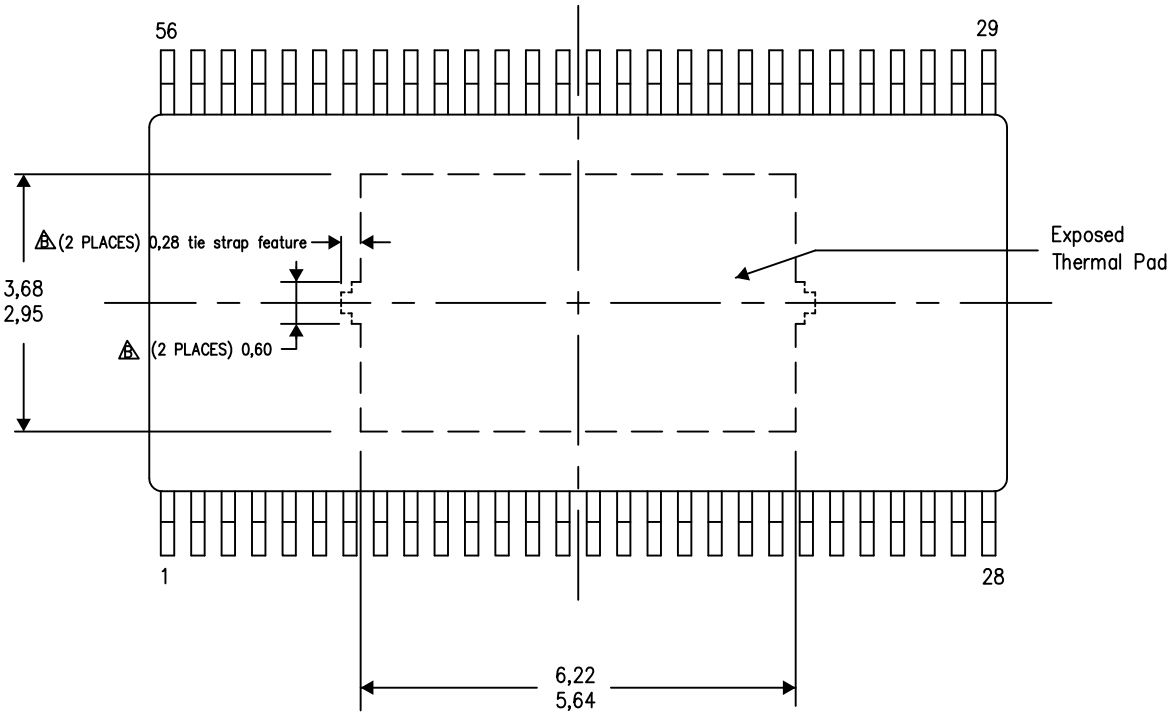
DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

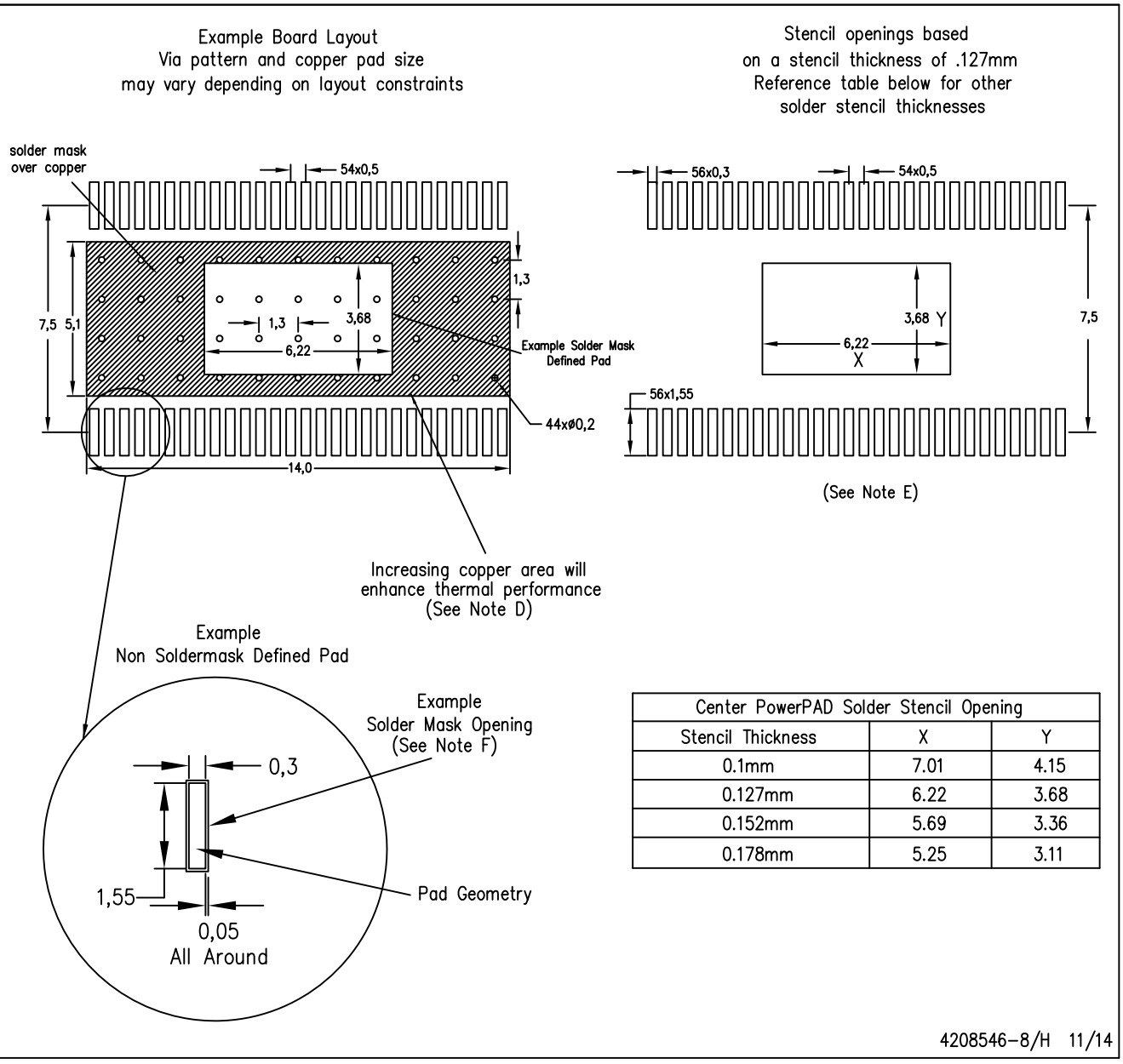
4206320–13/S 11/14

NOTES: A. All linear dimensions are in millimeters

B. Keep–out features are identified to prevent board routing interference.
These exposed metal features may vary within the identified area or completely absent on some devices.

PowerPAD is a trademark of Texas Instruments.

DCA (R–PDSO–G56) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.01	4.15
0.127mm	6.22	3.68
0.152mm	5.69	3.36
0.178mm	5.25	3.11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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