适用于汽车显示的 DLP3034-Q1 0.3 英寸 WVGA 405nm DMD

1 特性

- 通过汽车认证
  - DMD 阵列工作温度范围 -40°C 至 105°C
- 支持 405nm 照明源
- 0.3 英寸对角线微镜阵列
  - 7.6µm 微镜间距
  - ±12° 微镜倾斜角（相对于平面）
  - 采用侧面照明以提高效率
- WVGA (864 × 480) 分辨率
- 偏振无关型空间光调制器
  - 与 LED 或激光光源兼容
- 低功耗：105mW（典型值）
- 工作温度范围：-40°C 至 105°C
- 具有 2.5°C/W 热效率的密封封装
- 可实现系统内验证的 JTAG 边界扫描
- 与 DLPC120-Q1 汽车 DMD 控制器兼容
- 78MHz DDR DMD 接口

2 应用

- 适用于汽车前窗、侧窗和后窗的透明窗口显示

3 说明

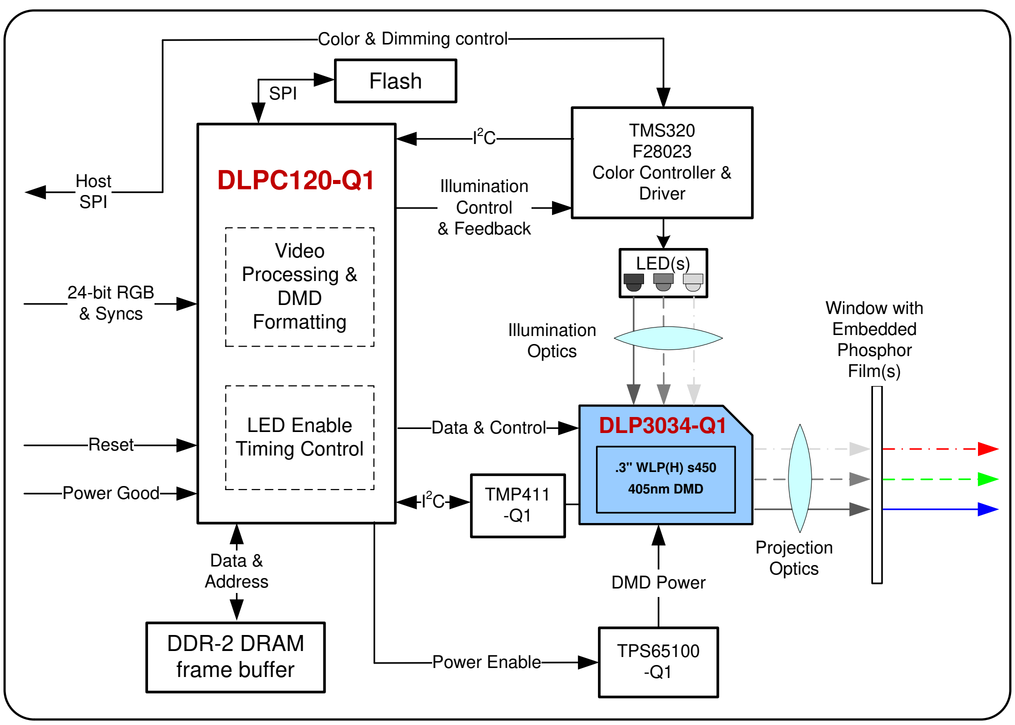
DLP3034-Q1 汽车 DMD 主要针对透明窗口显示 应用。该芯片组可与光学投影系统中的 405nm 照明源（例如 LED 或激光）配合使用，从而在嵌入放射性荧光膜的窗口上投影。当这些透明的放射性膜接收到 DLP3034-Q1 投影仪发出的 405nm 光线时，窗口将发出可见光谱范围内的光线。此外，该芯片组可以凭借宽动态范围和快速开关功能（不随温度的变化而变化）实现高功率光学系统。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
DLP3034-Q1	FYJ (149)	22.30mm × 32.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

DLP®DLP3034-Q1 系统框图



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4 修订历史记录

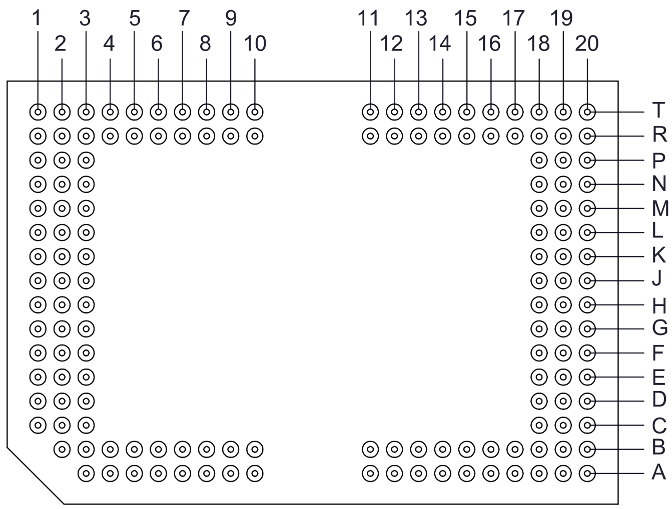
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2019) to Revision A **Page**

- 已更改 将器件状态从*高级信息* 更改为*生产数据* ... 1
- Changed illumination power density specifications between 395-nm and 420-nm in the *Recommended Operating Conditions* ... 7
- Added *Illumination Mission Profile Considerations* section to mention TI's testing at 405-nm wavelengths to be considered in final implementation ... 29

5 Pin Configuration and Functions

FYJ Package
149-Pin CPGA
Bottom View



Pin Configurations and Functions

PIN		I/O	DESCRIPTION	TRACE, mm(1)
NAME	**NO.**			
DATA(0)	F18	LVCMOS input	Data bus. Synchronous to rising edge and falling edge of DCLK.	8.059
DATA(1)	F20			
DATA(2)	G20			
DATA(3)	G19			
DATA(4)	H19			
DATA(5)	G18			
DATA(6)	J20			
DATA(7)	H20			
DATA(8)	J19			
DATA(9)	K18			
DATA(10)	K19			
DATA(11)	L20			
DATA(12)	L18			
DATA(13)	K20			
DATA(14)	M18			
DCLK	N18		Data clock.	
LOADB	M20		Parallel latch load enable. Synchronous to rising edge and falling edge of DCLK.	10.939
SCTRL	N19		Serial control (sync). Synchronous to rising edge and falling edge of DCLK.	6.596
TRC	M19		Toggle rate control. Synchronous to rising edge and falling edge of DCLK.	8.617
DAD_BUS	A7		Reset control serial bus. Synchronous to rising edge of SAC_CLK.	10.413
RESET_OEZ	A5		Active low. Output enable signal for internal reset driver circuitry.	13.37
RESET_STROBE	A10		Rising edge on RESET_STROBE latches in the control signals.	13.329
SAC_BUS	B9		Stepped address control serial bus. Synchronous to rising edge of SAC_CLK.	12.586
SAC_CLK	A8		Stepped address control clock.	12.668
TCK	M2		JTAG clock.	10.489
TDI	N3		JTAG data input. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.	11.04
TDO	M3	LVCMOS output	JTAG data output. Synchronous to falling edge of TCK. Tri-state failsafe output buffer.	10.067
TMS	R5	LVCMOS input	JTAG mode select. Synchronous to rising edge of TCK. Bond pad connects to internal pull up resistor.	10.413
TEMP_MINUS	T10	Analog Input	Calibrated temperature diode used to assist accurate temperature measurements of DMD die.	N/A
TEMP_PLUS	T11			N/A
No Connect (Unused)	A3, A18, A19, A20, B2, B10, B18, B19, B20, C1, C20, D18, D19, D20, E18, E19, E20, N20, P20, R18, R19, R20, T18, T19, T20	N/A	N/A	N/A

(1) Propagation delay is 10.24 ps/mm for the DMD Series 450 ceramic package trace lengths.

Pin Configurations and Functions (continued)

PIN		I/O	DESCRIPTION	TRACE, mm[1]
NAME	NO.			
V_{BIAS}[2]	F3, K3, L3	Power	Power supply for positive bias level of mirror reset signal.	N/A
V_{CC}[2]	A9, A12, A14, A16, B13, B16, R12, R13, R16, R17, T13, T14, T16	Power	Power supply for low voltage CMOS logic. Power supply for normal high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal during power down.	N/A
V_{CCH}	P3, R3, T3, T4, T5, T6	Connect to GND	Reserved pin.	N/A
V_{OFFSET}[2]	D1, E1, M1, N1	Power	Power supply for high voltage CMOS logic. Power supply for stepped high voltage at mirror address electrodes. Power supply for offset level of mirror reset signal.	N/A
V_{REF}[2]	B11, B12	Power	Power supply for low voltage CMOS DDR interface.	N/A
V_{RESET}[2]	B3, C3, E3	Power	Power supply for negative reset level of mirror reset signal.	N/A
V_{SS}[2]	A6, A11, A13, A15, A17, B4, B5, B8, B14, B15, B17, C2, C18, C19, F1, F2, F19, H1, H2, H3, H18, J18, K1, K2, L19, N2, P18, P19, R4, R14, R15, T7, T9, T12, T15, T17	Power	Common return for all power.	N/A
V_{SSH}	P1, P2, R1, R2, T1, T2	Connect to GND	Reserved pin.	N/A
RESERVED_BIM	T8	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_DT	R7	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RM	E2	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_R(0)	G1	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(1)	G2	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(2)	G3	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(3)	J1	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(4)	J2	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(5)	J3	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(6)	L1	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_R(7)	L2	Do not connect	Bond pad connects to 250k pull down resistor. Manufacturing test.	N/A
RESERVED_PFE	R6	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RA(0)	B6	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RA(1)	D3	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RA(2)	B7	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RS(0)	A4	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_RS(1)	D2	Connect to GND	Bond pad connects to internal pull down resistor.	N/A
RESERVED_SO	R9	Do not connect	Tri-state failsafe output buffer.	N/A
RESERVED_TP(0)	R8	Connect to GND	Manufacturing test.	N/A
RESERVED_TP(1)	R10	Connect to GND	Manufacturing test.	N/A
RESERVED_TP(2)	R11	Connect to GND	Manufacturing test.	N/A

(2) The following power supplies are required to operate the DMD: V_{BIAS}, V_{CC}, V_{OFFSET}, V_{REF}, V_{RESET}, V_{SS}.

6 Specifications

6.1 Absolute Maximum Ratings

See [(1)]

		MIN	MAX	UNIT
SUPPLY VOLTAGE				
V_{REF}	LVCMOS logic supply voltage[(2)]	–0.5	4	V
V_{CC}	LVCMOS logic supply voltage[(2)]	–0.5	4	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage[(2)]	–0.5	8.75	V
V_{BIAS}	Mirror electrode voltage	–0.5	17	V
$\|V_{BIAS} – V_{OFFSET}\|$	Supply voltage delta[(3)]		8.75	V
V_{RESET}	Mirror electrode voltage	–11	0.5	V
Input voltage: other Inputs	See [(2)]	–0.5	V_{REF} + 0.3	V
f_{DCLK}	Clock frequency	60	80	MHz
I_{TEMP_DIODE}	Temperature diode current		500	µA
ENVIRONMENTAL				
T_{ARRAY}	Operating DMD array temperature[(4)]	–40	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Unless otherwise indicated, these are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND (V_{SS}). V_{BIAS}, V_{CC}, V_{OFFSET}, V_{REF}, V_{RESET}, and V_{SS} are required to operate the DMD.
(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than or equal to 8.75 V.
(4) See *Micromirror Array Temperature Calculation* section.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	125	°C

6.3 ESD Ratings[(1)]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(2)]		±2000	V
		Charged-device model (CDM), per JESD22-C101[(3)]	All pins	±500	
			Corner pins	±750	

(1) All CMOS devices require proper electrostatic discharge (ESD) handling procedures.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE						
V_{REF}	LVCMOS interface power supply voltage[1]		1.65	1.8	1.95	V
V_{CC}	LVCMOS logic power supply voltage[1]		2.25	2.5	2.75	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage[1]		8.25	8.5	8.75	V
V_{BIAS}	Mirror electrode voltage		15.5	16	16.5	V
$\|V_{BIAS} – V_{OFFSET}\|$	Supply voltage delta[2]				8.75	V
V_{RESET}	Mirror electrode voltage		–9.5	–10	–10.5	V
V_P VT+	Positive going threshold voltage		0.4 × V_{REF}		0.7 × V_{REF}	V
V_N VT–	Negative going threshold voltage		0.3 × V_{REF}		0.6 × V_{REF}	V
V_H ΔVT	Hysteresis voltage (Vp – Vn)		0.1 × V_{REF}		0.4 × V_{REF}	V
I_{OH_TDO}	High level output current @ Voh = 2.25 V, TDO, Vcc = 2.25 V				–2	mA
I_{OL_TDO}	Low level output current @ Vol = 0.4 V, TDO, Vcc = 2.25 V				2	mA
TEMPERATURE DIODE						
I_{TEMP_DIODE}	Max current source into temperature diode[3]				120	µA
ENVIRONMENTAL						
T_{ARRAY}	Operating DMD array temperature[4]		–40		105	°C
$ILL_{sub-385nm}$	Illumination, wavelength < 385 nm				2.0	mW/cm^2
$ILL_{385-to-395nm}$	Illumination, 385 nm < wavelength < 395 nm				250	mW/cm^2
$ILL_{395-to-400nm}$	Illumination, 395 nm < wavelength < 400 nm				800	mW/cm^2
$ILL_{400-to-420nmnm}$	Illumination, 400 nm < wavelength < 420 nm				8.0	W/cm^2
ILL_{VIS}	Illumination, 420 nm < wavelength < 800 nm				Thermally limited[5]	W/cm^2
$ILL_{OVERFILL}$	Illumination overfill maximum heat load in areas shown in Figure 1[6]	$T_{ARRAY} \le 75°C$			26	mW/mm^2
	Illumination overfill maximum heat load in areas shown in Figure 1[6]	$T_{ARRAY} > 75°C$			20	mW/mm^2

(1) V_{BIAS}, V_{CC}, V_{OFFSET}, V_{REF}, V_{RESET}, V_{SS} are required to operate the DMD.
(2) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than or equal to 8.75 V.
(3) Temperature Diode is to allow accurate measurement of the DMD array temperature during operation.
(4) DMD active array temperature can be calculated as shown in *Micromirror Array Temperature Calculation* section. Additionally, the DMD array temperature is monitored in the system using the TMP411-Q1 and DLPC120-Q1 as shown in the system block diagram.
(5) Limited by the resulting micromirror array temperature. Refer to the calculation example in *Micromirror Array Temperature Calculation* section.
(6) The active area of the DLP303x-Q1 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

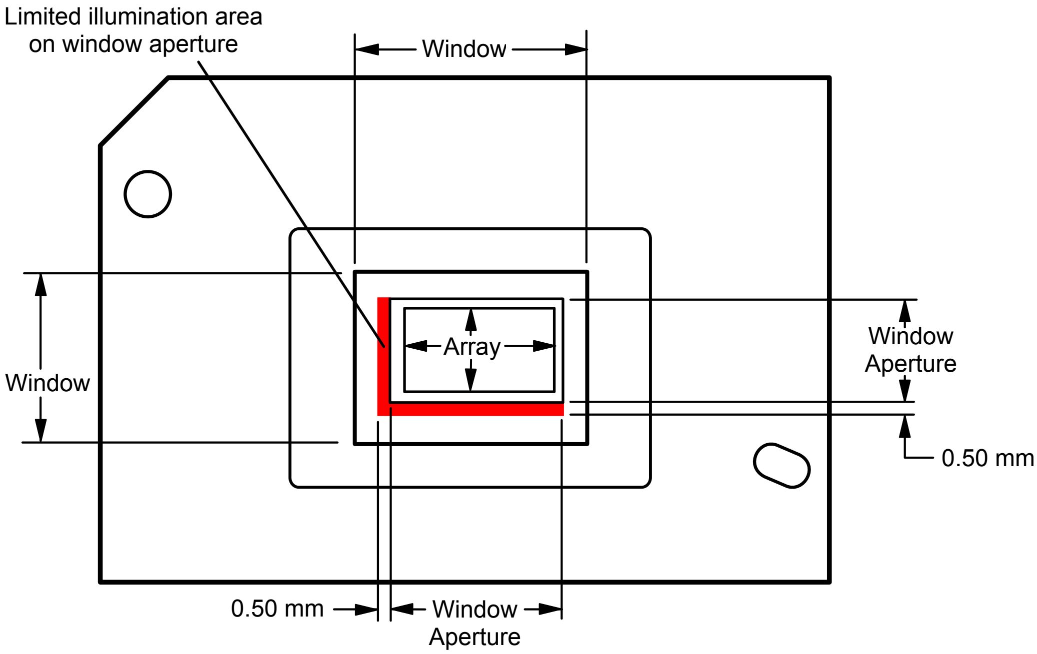


Figure 1. Illumination Overfill Diagram

6.5 Thermal Information

THERMAL METRIC[1]		DLP3034-Q1 FYJ (CPGA) 149 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)[1]	2.5	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	VCC = 2.25 V I_{OH} = –8 mA	1.7			V
V_{OH2}	High level output voltage[3]	VREF = 1.8 V I_{OH} = –2 mA	1.44			V
V_{OL}	Low level output voltage	VCC = 2.75 V I_{OL} = 8 mA			0.4	V
V_{OL2}	Low level output voltage[3]	VREF = 1.8 V I_{OL} = 2 mA			0.36	V
I_{OZ}	Output high impedance current	VREF = 1.95 V V_{OL} = 0 V	–10			µA
		VREF = 1.95 V V_{OH} = VREF			10	
I_{IL}	Low level input current[4]	VREF = 1.95 V V_I = 0 V	–5			µA
I_{IH}	High level input current[4]	VREF = 1.95 V V_I = VREF			6	µA
I_{IL2}	Low level input current[5]	VREF = 1.95 V V_I = 0 V	–785			µA
I_{IH2}	High level input current[5]	VREF = 1.95 V V_I = VREF			6	µA
I_{IL3}	Low level input current[6]	VREF = 1.95 V V_I = 0 V	–5			µA
I_{IH3}	High level input current[6]	VREF = 1.95 V V_I = VREF			785	µA
CURRENT						
I_{REF}	Current at V_{REF} = 1.95 V	f_{DCLK} = 80 MHz			2.80	mA
I_{cc}	Current at V_{CC} = 2.75 V	f_{DCLK} = 80 MHz			59.90	mA
I_{OFFSET}	Current at V_{OFFSET} = 8.75 V				2.93	mA
I_{BIAS}	Current at V_{BIAS} = 16.5 V				2.30	mA
I_{RESET}	Current at V_{RESET} = –10.5 V				–2.00	mA

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) Specification is for LVCMOS JTAG output pin TDO.
(4) Specification is for LVCMOS input pins, which do not have pull up or pull down resistors. See *Pin Configuration and Functions* section.
(5) Specification is for LVCMOS input pins which do have pull up resistors (JTAG: TDI, TMS). See *Pin Configuration and Functions* section.
(6) Specification is for LVCMOS input pins which do have pull down resistors. See *Pin Configuration and Functions* section.

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
POWER(7)						
P_{REF}	Power at V_{REF} = 1.95 V	f_{DCLK} = 80 MHz			5.46	mW
P_{CC}	Power at V_{CC} = 2.75 V	f_{DCLK} = 80 MHz			164.73	mW
P_{OFFSET}	Power at V_{OFFSET} = 8.75 V				25.64	mW
P_{BIAS}	Power at V_{BIAS} = 16.5 V				37.95	mW
P_{RESET}	Power at V_{RESET} = –10.5 V				21.00	mW
P_{TOTAL}	Total power at nominal conditions	f_{DCLK} = 80 MHz		105	254.77	mW
CAPACITANCE						
C_{IN}	Input pin capacitance	f = 1 MHz			20	pF
C_A	Analog pin capacitance (TEMP_PLUS and TEMP_MINUS pins)	f = 1 MHz			65	pF
C_o	Output pin capacitance	f = 1 MHz			20	pF

(7) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.

6.7 Timing Requirements

Over *Recommended Operating Conditions* unless otherwise noted.

		MIN	NOM	MAX	UNIT
DMD MIRROR AND SRAM CONTROL LOGIC SIGNALS					
t_{SU}	Setup time SAC_BUS low before SAC_CLK↑	1.0			ns
t_H	Hold time SAC_BUS low after SAC_CLK↑	1.0			ns
t_{SU}	Setup time DAD_BUS high before SAC_CLK↑	1.0			ns
t_H	Hold time DAD_BUS after SAC_CLK↑	1.0			ns
t_C	Cycle time SAC_CLK	12.5		16.67	ns
t_W	Pulse width 50% to 50% reference points: SAC_CLK high or low	5.0			ns
t_R	Rise time 20% to 80% reference points: SAC_CLK			2.5	ns
t_F	Fall time 80% to 20% reference points: SAC_CLK			2.5	ns
DMD DATA PATH AND LOGIC CONTROL SIGNALS					
t_{SU}	Setup time DATA(14:0) before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time DATA(14:0) after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time SCTRL before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time SCTRL after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time TRC before DCLK↑ or DCLK↓	1.0			ns
t_H	Hold time TRC after DCLK↑ or DCLK↓	1.0			ns
t_{SU}	Setup time LOADB low before DCLK↑	1.0			ns
t_H	Hold time LOADB low after DCLK↓	1.0			ns
t_{SU}	Setup time RESET_STROBE high before DCLK↑	1.0			ns
t_H	Hold time RESET_STROBE after DCLK↑	3.5			ns
t_C	Cycle time DCLK	12.5		16.67	ns
t_W	Pulse width 50% to 50% reference points: DCLK high or low	5.0			ns
$t_W(L)$	Pulse width 50% to 50% reference points: LOADB low	7.0			ns
$t_W(H)$	Pulse width 50% to 50% reference points: RESET_STROBE high	7.0			ns
t_R	Rise time 20% to 80% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
t_F	Fall time 80% to 20% reference points: DCLK, DATA, SCTRL, TRC, LOADB			2.5	ns
JTAG BOUNDARY SCAN CONTROL LOGIC SIGNALS					
f_{TCK}	Clock frequency TCK			10	MHz
t_C	Cycle time TCK	100			ns
t_W	Pulse width 50% to 50% reference points: TCK high or low	10			ns
t_{SU}	Setup time TDI valid before TCK↑	5			ns
t_H	Hold time TDI valid after TCK↑	25			ns
t_{SU}	Setup time TMS valid before TCK↑	5			ns
t_H	Hold time TMS valid after TCK↑	25			ns
t_R	Rise time 20% to 80% reference points: TCK, TDI, TMS			2.5	ns
t_R	Fall time 80% to 20% reference points: TCK, TDI, TMS			2.5	ns

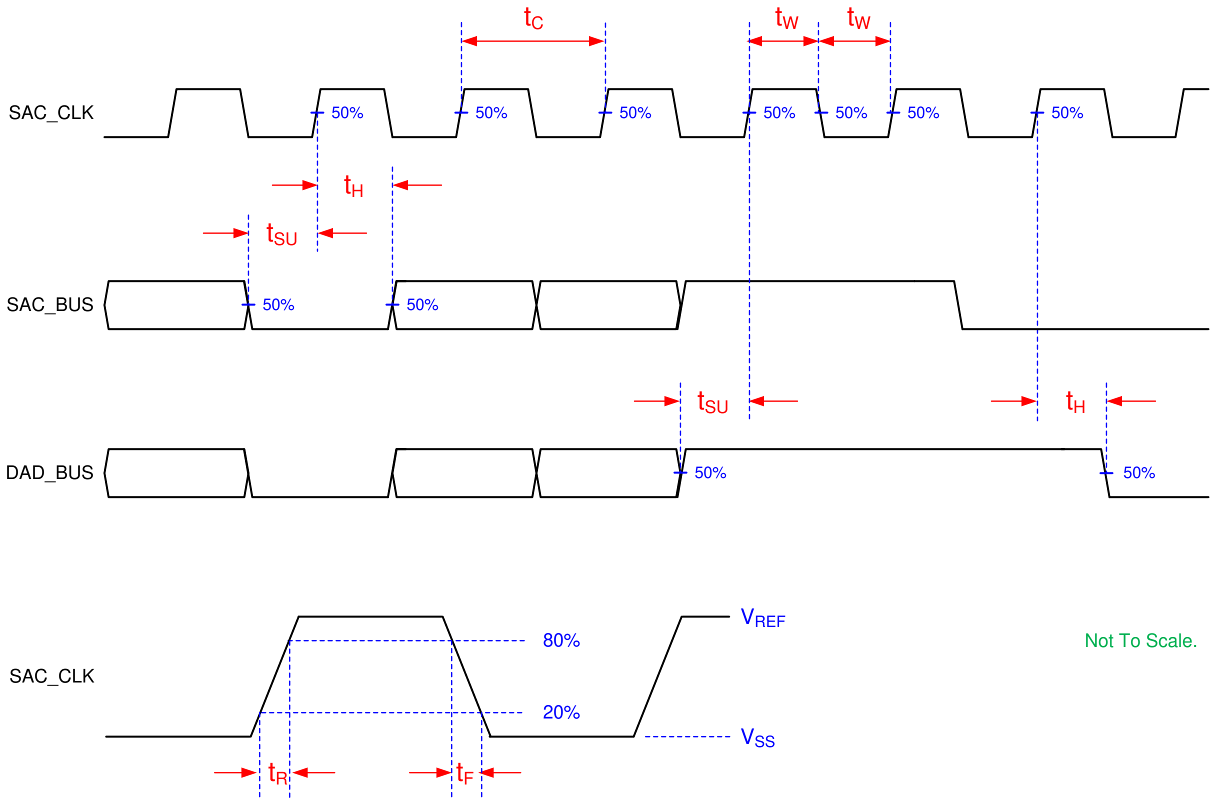


Figure 2. DMD Mirror and SRAM Control Logic Timing Requirements

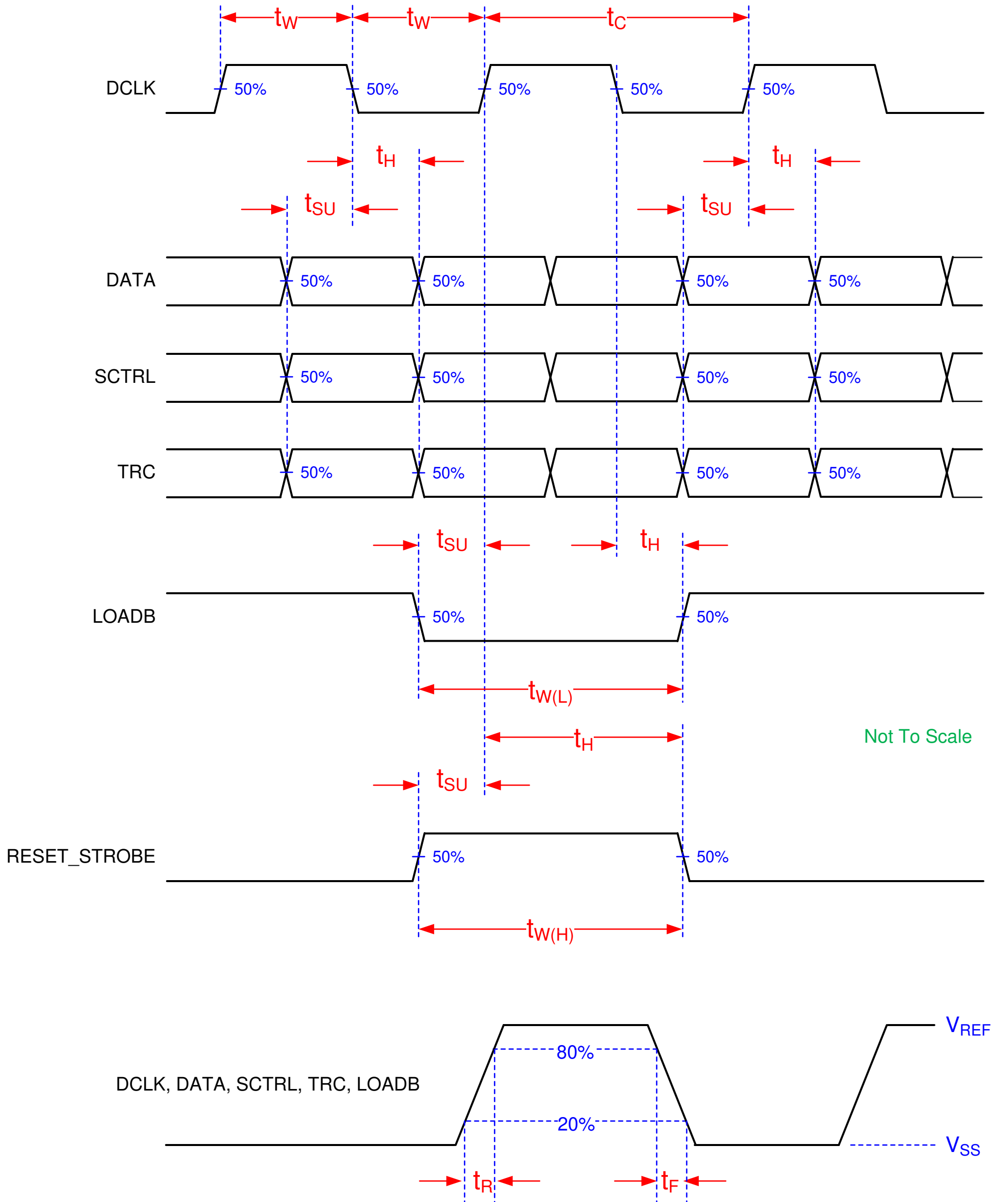


Figure 3. DMD Data Path and Control Logic Timing Requirements

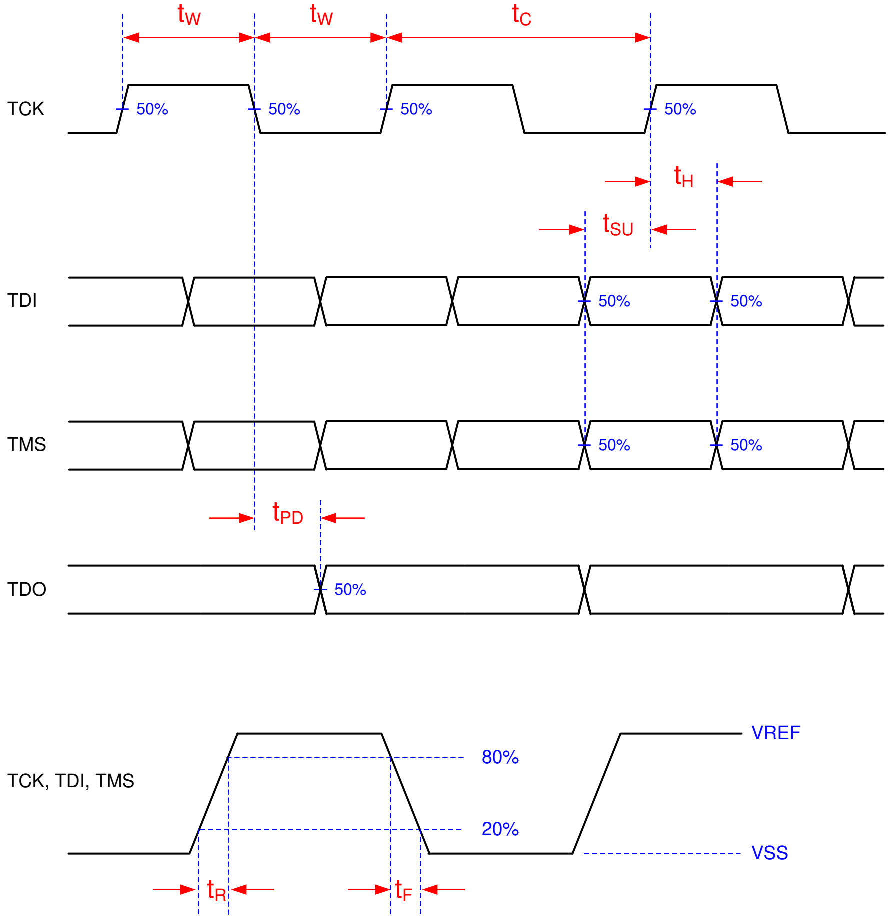


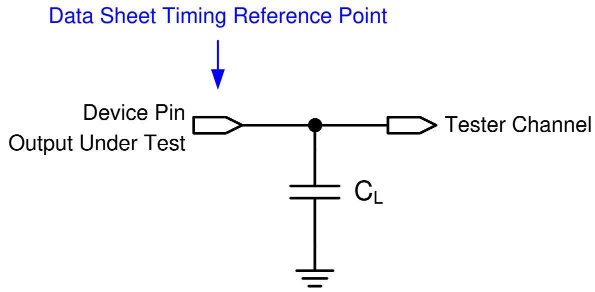
Figure 4. JTAG Boundary Scan Control Logic Timing Requirements

6.8 Switching Characteristics[1]

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q (see Figure 4)	C_L = 11 pF, from (Input) falling edge of TCK to (Output) TDO. See Figure 4.	3		25	ns

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.



See *Micromirror Array* section for more information.

Figure 5. Test Load Circuit for Output Propagation Measurement

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1:				
Uniformly distributed within the Thermal Interface Area shown in Figure 6			11.30	kg
Uniformly distributed within the Electrical Interface Area shown in Figure 6			11.34	kg
Condition 2:				
Uniformly distributed within the Thermal Interface Area shown in Figure 6			0	kg
Uniformly distributed within the Electrical Interface Area shown in Figure 6			22.64	kg

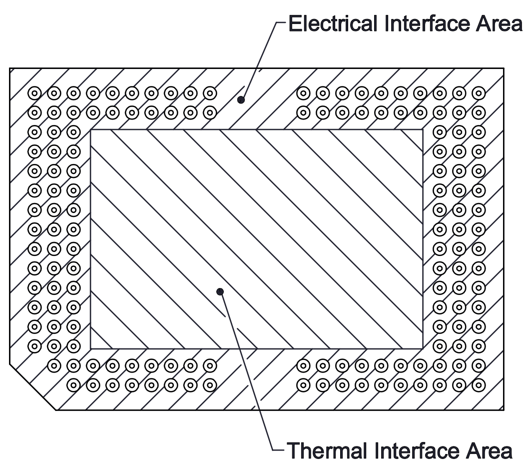


Figure 6. System Interface Loads

6.10 Physical Characteristics of the Micromirror Array

PARAMETER		VALUE	UNIT
N Number of active columns	See Figure 7	684	micromirrors
M Number of active rows	See Figure 7	608	micromirrors
ε Micromirror (pixel) pitch – diagonal	See Figure 8	7.6	µm
P Micromirror (pixel) pitch – horizontal and vertical	See Figure 8	10.8	µm
Micromirror active array width	P × M + P / 2; see Figure 7	6.5718	mm
Micromirror active array height	(P × N) / 2 + P / 2; see Figure 7	3.699	mm
Micromirror active border	Pond of micromirror (POM)(1)	10	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

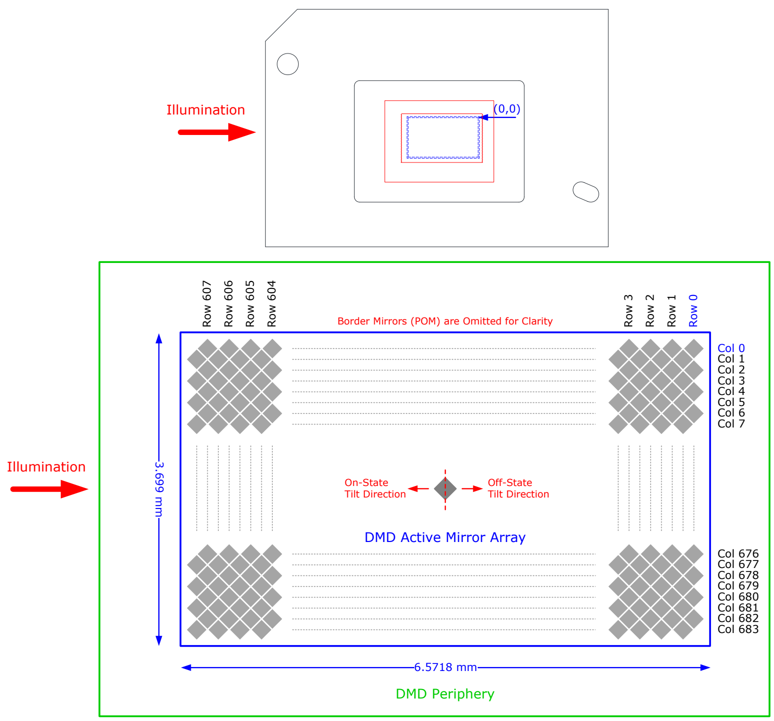


Figure 7. Micromirror Array Physical Characteristics

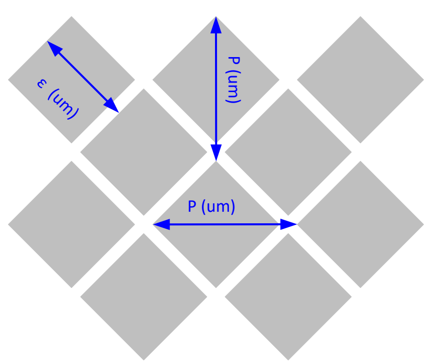


Figure 8. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

Table 1. Optical Parameters[1]

	PARAMETER		MIN	NOM	MAX	UNIT
α	Micromirror Tilt Angle, landed (on-state or off-state) (see [2] and Figure 9)			12		°
β	Micromirror Tilt Angle Variation, device to device (see [2] and Figure 9)		–1		1	°
	DMD Efficiency, 400 nm – 680 nm (see [3])			66%		
	Number of non-operational micromirrors[4]	Adjacent micromirrors			0	micromirrors
		Non-adjacent micromirrors			10	micromirrors

(1) Optical parameters are characterized at 25°C.
(2) Mirror Tilt: Limits on variability of mirror tilt are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image especially at higher system F/#. Variations in the average tilt angle between devices may result in colorimetry, brightness, and system contrast variations.
(3) DMD efficiency is measured photopically under the following conditions: 24° illumination angle, F/2.4 illumination and collection apertures, uniform source spectrum (halogen), uniform pupil illumination, the optical system is telecentric at the DMD, and the efficiency numbers are measured with 100% electronic mirror duty cycle and do not include system optical efficiency or overfill loss. Note that this number is measured under conditions described above and deviations from these specified conditions could result in a different efficiency value in a different optical sytem. The factors that can inclueence the DMD efficiency related to system application include: light source spectral distribution and diffraction efficiency at those wavelengths (especially with discrete light sources such as LEDs or lasers), and illumination and collection apertures (F/#) and diffraction efficiency. The interaction of these system factors as well as the DMD efficiency factors that are not system dependent are described in detail in the *DMD Optical Efficiency Application Note*, which can be accessed by contacting TI Applications Engineering.
(4) A non-operational micromirror is defined as a micromirror that is unable to transition between the on-state and off-state positions.

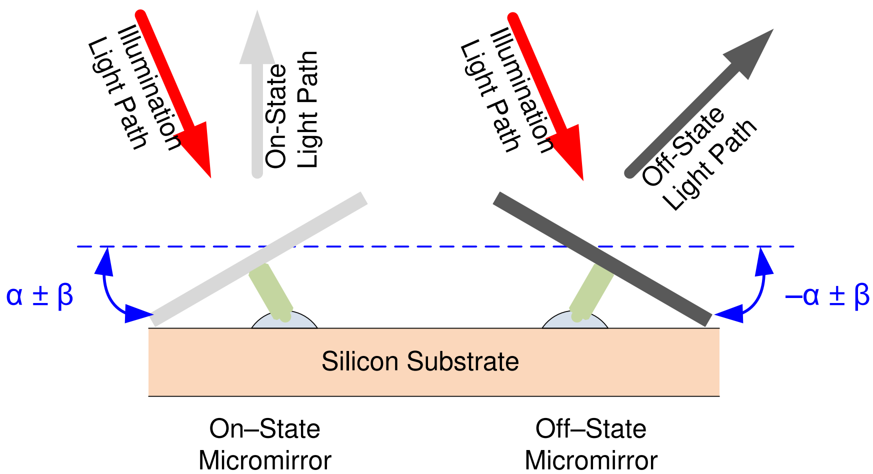


Figure 9. Micromirror Tilt Angle

6.12 Window Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture (1)				See (1)	

(1) See the package mechanical ICD for details regarding the size and location of the window aperture.

6.13 Chipset Component Usage Specification

The DLP3034-Q1 DMD is a component of the DLP® chipset including the DLPC120-Q1 DMD controller. Reliable function and operation of the DMD requires that it be used in conjunction with DLPC120-Q1 controller.

NOTE

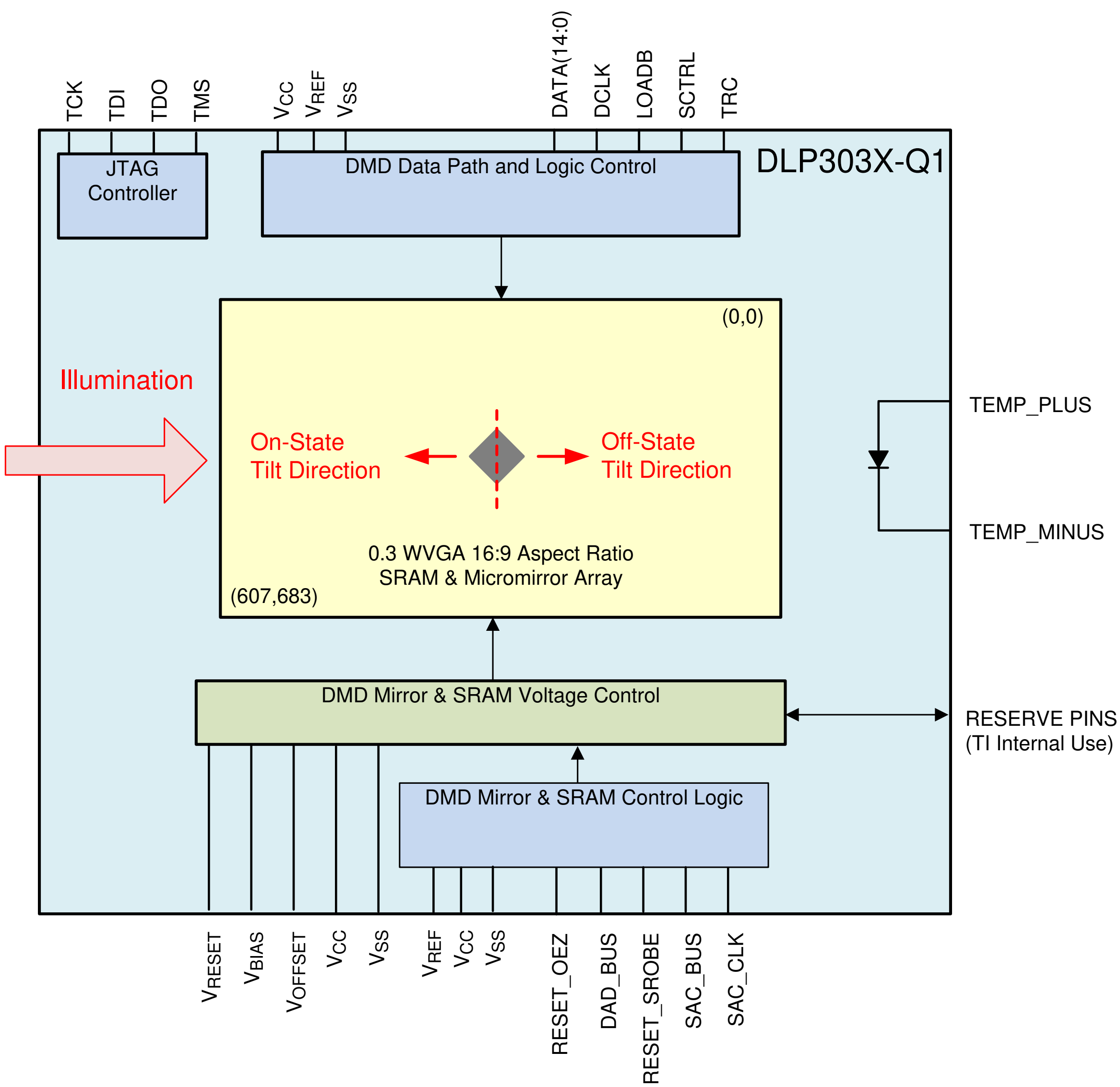
TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously

7 Detailed Description

7.1 Overview

The DLP3034-Q1 DMD has a resolution of 608 × 684 mirrors configured in a diamond format that results in an aspect ratio of 16:9, which combined with the DLPC120-Q1 image processing creates an effective resolution of 864 × 480 square pixels. By configuring the pixels in a diamond format, the illumination input to the DMD enters from the side allowing for smaller mechanical packaging of the optical system. Additionally, side illumination can also enable increased optical efficiency compared to a corner illuminated square pixel design.

7.2 Functional Block Diagram



7.3 Feature Description

To ensure reliable operation, the DLP3034-Q1 DMD must be used with the DLPC120-Q1 DMD Display controller.

Feature Description (continued)

7.3.1 Micromirror Array

The DLP3034-Q1 DMD consists of a two-dimensional array of 1-bit CMOS memory cells that determine the state of the each of the 608 × 684 micromirrors in the array. Refer to Physical Characteristics of the Micromirror Array for a calculation of how the 608 × 684 micromirror array represents a 16:9 dimensional aspect ratio to the user. Each micromirror is either “ON” (tilted +12°) or “OFF” (tilted –12°). Combined with appropriate projection optical system the DMD can be used to create clear, colorful, and vivid digital images.

7.3.2 Double Data Rate (DDR) Interface

Each DMD micromirror and its associated SRAM memory cell is loaded with data from the DLPC120-Q1 via the DDR interface (DATA(14:0), DCLK, LOADB, SCRTL, and TRC). These signals are low voltage CMOS nominally operating at 1.8-V level to reduce power and switching noise. This high speed data input to the DMD allows for a maximum update rate of the entire micromirror array to be nearly 5 kHz, enabling the creation of seamless digital images using Pulse Width Modulation (PWM).

7.3.3 Micromirror Switching Control

Once data is loaded onto the DMD, the mirrors are caused to switch position (+12° or –12°) based on the timing signal sent to the DMD Mirror and SRAM control logic. The DMD mirrors will be switched from OFF to ON or ON to OFF, or stay in the same position based on control signals DAD_BUS, RESET_STROBE, SAC_BUS, and SAC_CLK, which are coordinated with the data loading by the DLPC120-Q1. In general, the DLPC120-Q1 loads the DMD SRAM memory cells over the DDR interface, and then commands to the micromirrors to switch position.

At power down, the DMD Mirrors are commanded by the DLPC120-Q1 to move to a near flat (0°) position as shown in *Power Supply Recommendations* section. The flat state position of the DMD mirrors are referred to as the “Parked” state. To maintain long term DMD reliability, the DMD must be properly “Parked” prior to every power down of the DMD power supplies. Refer to the *DLPC120-Q1 Programmer's Guide* for information about properly parking the DMD.

7.3.4 DMD Voltage Supplies

The micromirrors switching requires unique voltage levels to control the mechanical switching. These voltages levels are nominally 16 V, 8.5 V, and –10 V (V_{BIAS}, V_{OFFSET}, and V_{RESET}). The specification values for V_{BIAS}, V_{OFFSET}, and V_{RESET} are shown in *Recommended Operating Conditions*.

7.3.5 Logic Reset

Reset of the DMD is required and controlled by the DLPC120-Q1.

7.3.6 Temperature Sensing Diode

The DMD includes a temperature sensing diode designed to be used with the TMP411-Q1 temperature monitoring device. The DLPC120-Q1 monitors the DMD array temperature via the TMP411-Q1 and temperature sense diode. The DLPC120-Q1 operation of the DMD is based in part on the DMD array temperature, and therefore, this connection is essential to ensure reliable operation of the DMD.

Figure 10 shows the typical connection between the DLPC120-Q1, TMP411-Q1, and the DLP3034-Q1 DMD. The signals to the temperature sense diode are sensitive to system noise, therefore, care should be taken in the routing and implementation of this circuit. See the *TMP411-Q1 Data Sheet* for detailed PCB layout recommendations.

Feature Description (continued)

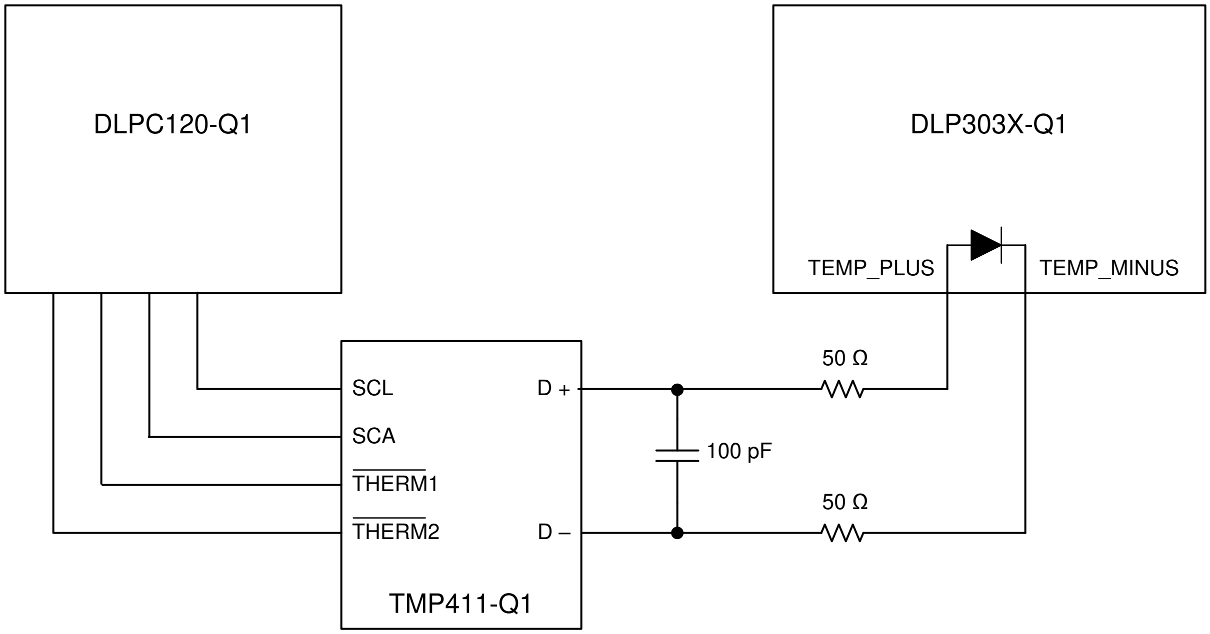


Figure 10. Temperature Sense Diode Typical Circuit Configuration

The DLPC120-Q1 automatically controls the DMD parking based on the temperature measured from the temperature sense diode; however, it is recommended that the host controller manage the parking via the proper methods described in the *DLPC120-Q1 Programmer's Guide*.

7.3.6.1 Temperature Sense Diode Theory

A temperature sensing diode is based on the fundamental current and temperature characteristics of a transistor. The diode is formed by connecting the transistor base to the collector. Two different known currents flow through the diode and the resulting diode voltage is measured in each case. The difference in their base-emitter voltages is proportional to the absolute temperature of the transistor.

Refer to the *TMP411-Q1 Data Sheet* for detailed information about temperature diode theory and measurement. Figure 11 and Figure 12 illustrate the relationship between the current and voltage through the diode.

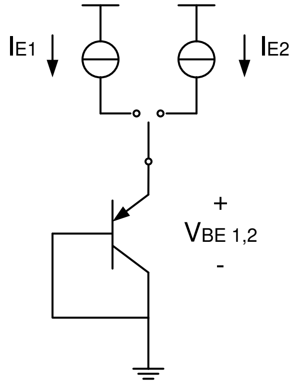


Figure 11. Temperature Measurement Theory

Feature Description (continued)

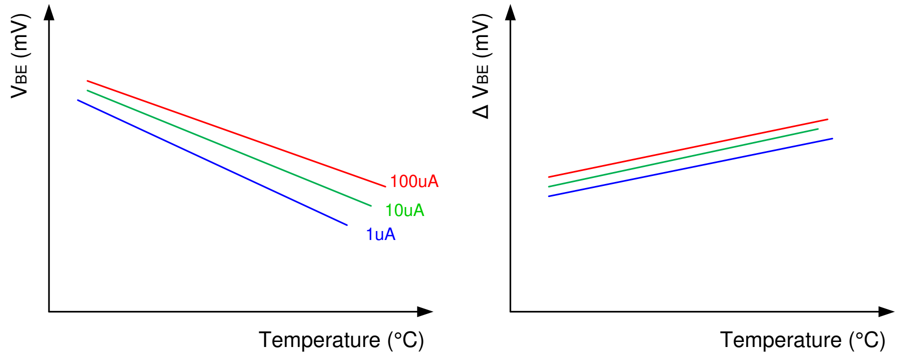


Figure 12. Example of Delta VBE vs Temperature

7.3.7 DMD JTAG Interface

The DMD uses 4 standard JTAG signals for sending and receiving boundary scan test data. TCK is the test clock used to drive an IEEE 1149.1 TAP state machine and logic. TMS directs the next state of the TAP state machine. TDI is the scan data input and TDO is the scan data output.

The DMD does not support IEEE 1149.1 signals TRST (Test Logic Reset) and RTCK (Returned Test Clock). Boundary scan cells on the DMD are Observe-Only. To initiate the JTAG boundary scan operation on the DMD, a minimum of 6 TCK clock cycles are required after TMS is set to logic high.

Refer to Figure 13 for a JTAG system board routing example. The DLPC120-Q1 can be enabled to perform an in system boundary scan test. See *DLPC120-Q1 Programmer's Guide* for information about this test.

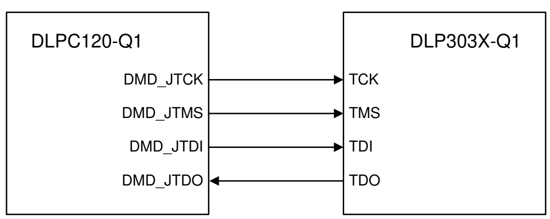


Figure 13. System Interface Connection to DLPC120-Q1

The DMD Device ID can be read via the JTAG interface. The ID and 32-bit shift order is shown in Figure 14.

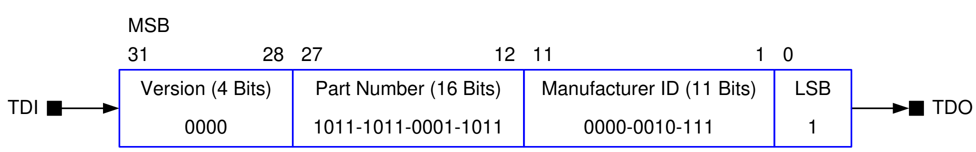


Figure 14. DMD Device ID and 32-bit Shift Order

Refer to Figure 15 for a JTAG boundary scan block diagram for the DMD. These show the pins and the scan order that are observed during the JTAG boundary scan.

Feature Description (continued)

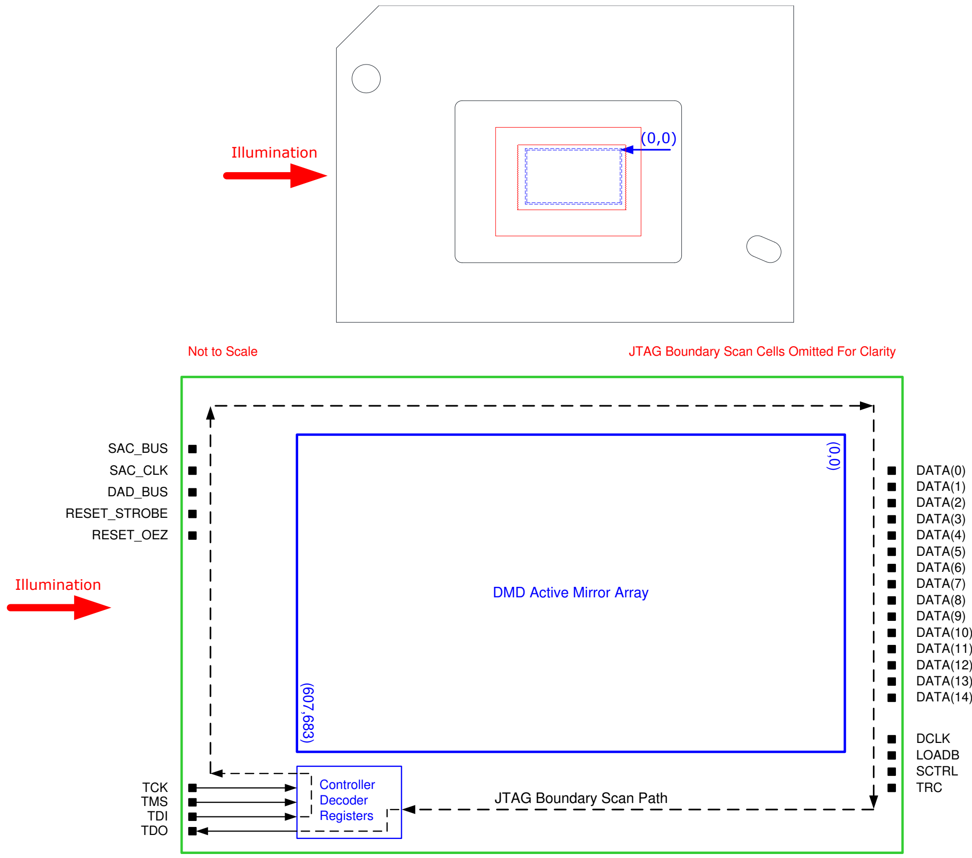


Figure 15. JTAG Boundary Scan Path

Refer to Figure 16 for a functional block diagram of the JTAG control logic.

Feature Description (continued)

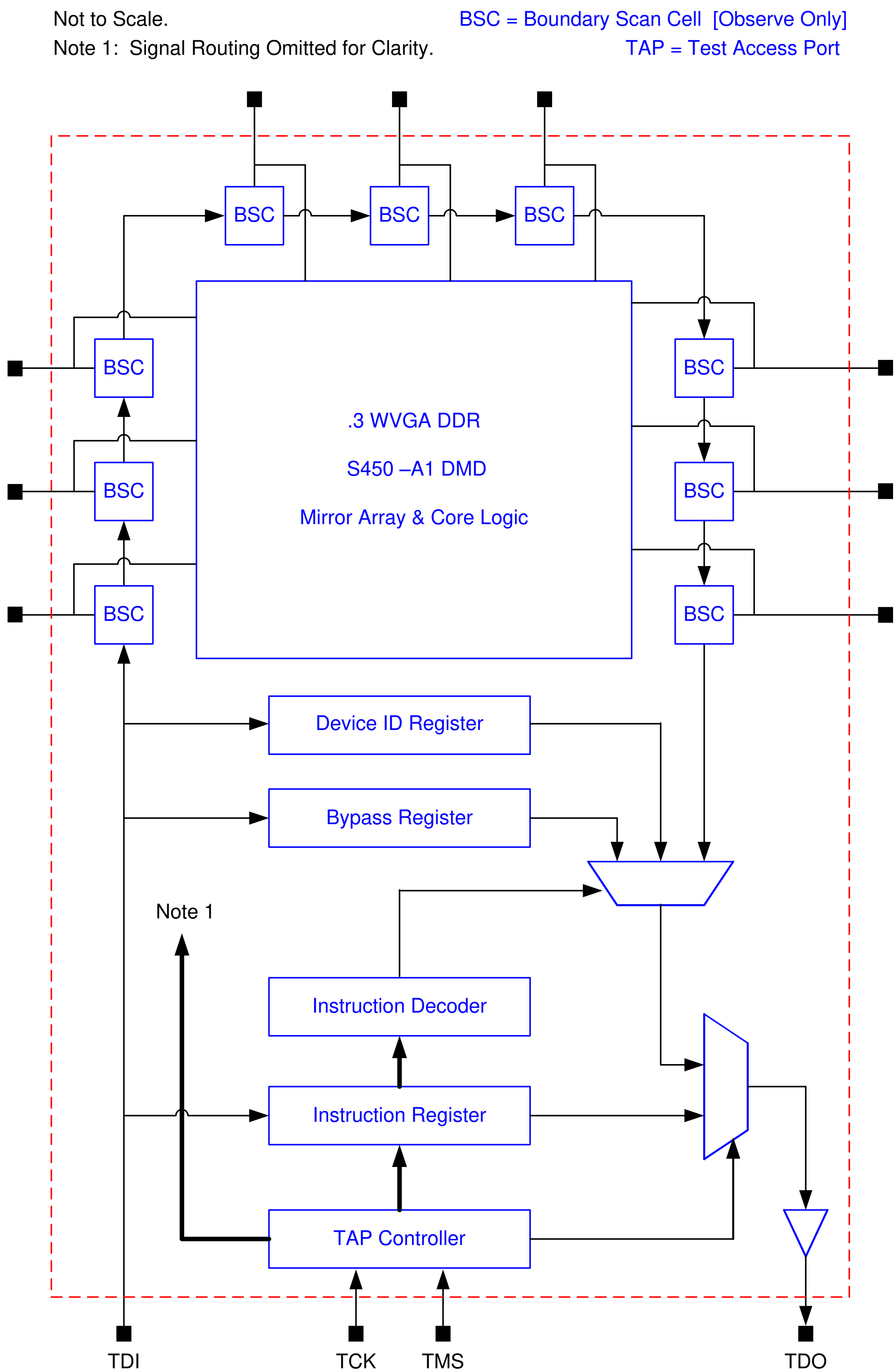


Figure 16. JTAG Functional Block Diagram

7.4 System Optical Considerations

Optimizing system optical performance and image quality strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described below.

7.4.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block flat-state and stray light from passing through the projection lens. The mirror tilt angle defines DMD capability to separate the "On" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast ratio can be reduced and objectionable artifacts in the image border and/or active area could occur.

7.4.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the image border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.4.3 Illumination Overfill and Alignment

Overfill light illuminating the area outside the active array can create artifacts from the mechanical features and other surfaces that surround the active array. These artifacts may be visible in the projected image. The illumination optical system should be designed to minimize light flux incident outside the active array and on the window aperture. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the area outside of the active array may still cause artifacts to be visible. Illumination light and overfill can also induce undesirable thermal conditions on the DMD, especially if illumination light impinges directly on the DMD window aperture or near the edge of the DMD window. Refer to *Recommended Operating Conditions* for a specification on this maximum allowable heat load due to illumination overfill.

NOTE

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

7.5 Micromirror Array Temperature Calculation

Active array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load.

Relationship between array temperature and the reference ceramic temperature (thermocouple location TP1 in Figure 17) is provided by the following equations.

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + (Q_{INCIDENT} \times \text{DMD Absorption Constant})$$

where

- T_{ARRAY} = computed DMD array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (TP1 location in Figure 17) (°C)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = DMD package thermal resistance from array to TP1 (°C/watt) (see *Thermal Information*)
- Q_{ARRAY} = total power, electrical plus absorbed, on the DMD array (watts)
- $Q_{ELECTRICAL}$ = nominal electrical power dissipation by the DMD (watts)
- $Q_{INCIDENT}$ = incident optical power to DMD (watts)
- DMD Absorption Constant = 0.42 (2)

Micromirror Array Temperature Calculation (continued)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies.

Absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source.

Equations shown previous are valid for a 1-chip DMD system with illumination distribution of 83.7% on the active array and 16.3% on the array border.

Sample calculation:

- $Q_{ELECTRICAL}$ = 0.105 W
- $T_{CERAMIC}$ = 55°C
- $Q_{INCIDENT}$ = 3 W

Q_{ARRAY} = 0.105 W + (3 W × 0.42) = 1.37 W (3)

T_{ARRAY} = 55°C + (1.37 W × 2.5°C/W) = 58.4°C (4)

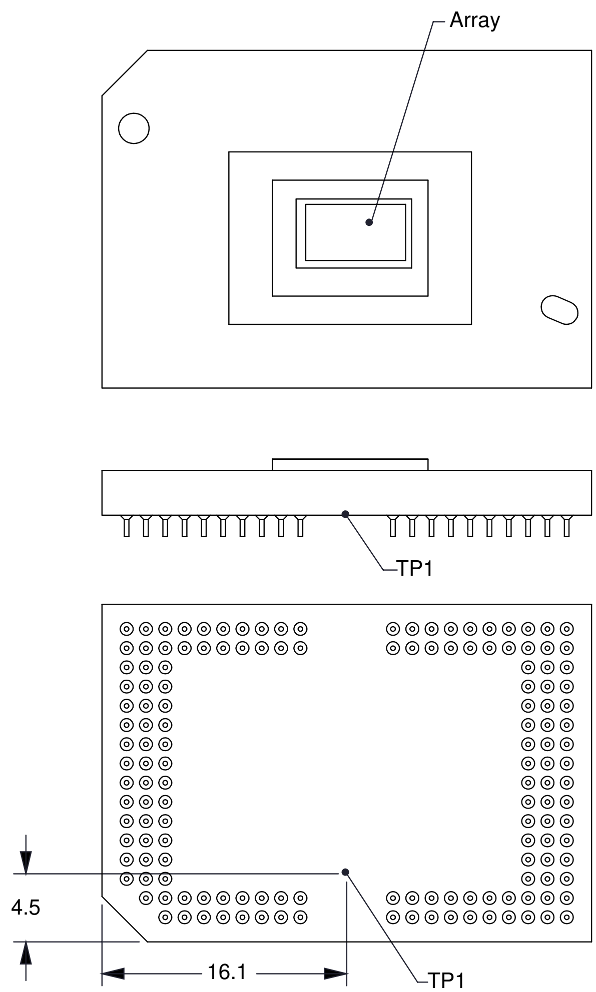


Figure 17. Thermocouple Locations

7.6 Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

As an example, assuming a fully-saturated white pixel, a landed duty cycle of 90/10 indicates that the referenced pixel is in the ON state 90% of the time (and in the OFF state 10% of the time), whereas 10/90 would indicate that the pixel is in the OFF state 90% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLP3034-Q1 DMD was designed to be used in automotive applications such as transparent window displays. The information shown in this section describes the transparent window display application based on the TI reference design. Contact TI application engineer for information on this design.

8.2 Typical Application

The DLP3034-Q1 DMD combined with the DLPC120-Q1 are the primary devices that make up the reference design for a transparent window display system as shown in the block diagram Figure 18.

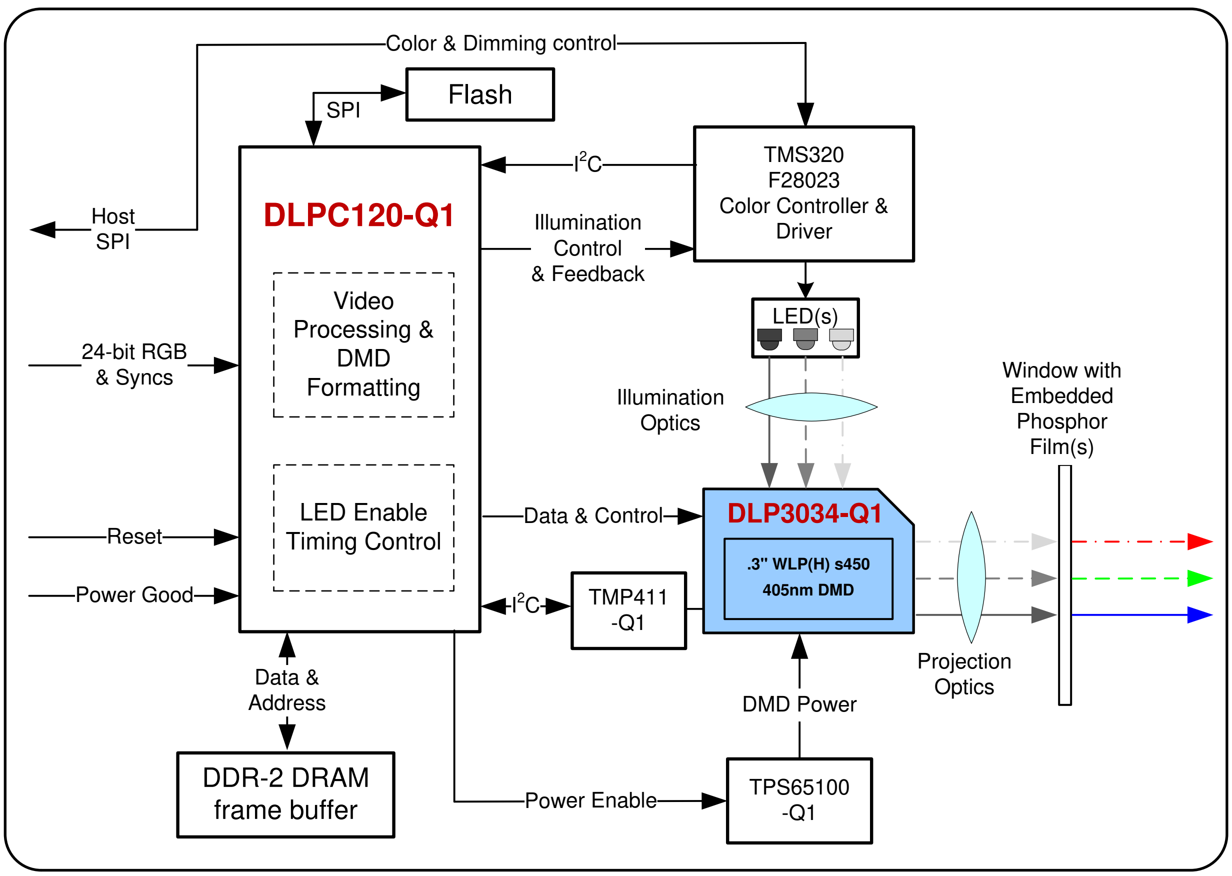


Figure 18. DLP3034-Q1 Reference Design Block Diagram

The DLPC120-Q1 accepts input video over the parallel RGB data interface up to 8 bits per color from a Video Graphics processor. The DLPC120-Q1 then processes the video data (864 × 480 manhattan orientation) by scaling the image to match the DMD resolution (608 × 684 diamond pixel), applies de-gamma correction, bezel adjustment, and then formats the data into DMD bit plane information and stores the data into the DDR2 DRAM. The DMD bit planes are read from DDR2 DRAM, and are then displayed on the DMD using Pulse Width Modulation (PWM) timing. The DLPC120-Q1 synchronizes the DMD bit plane data with the color enable timing for the LED color controller and Driver circuit. Finally, the DMD accepts the bit plane formatted data from the DLPC120-Q1 and displays the data according to the timing controlled by the DLPC120-Q1.

Typical Application (continued)

Due to the mechanical nature of the micromirrors, the latency of the DLP3034-Q1 and DLPC120-Q1 chipset is fixed across all temperature and operating conditions. The observed video latency is one frame, or 16.67 ms at an input frame rate of 60 Hz. However, please note that the use of the DLPC120-Q1 bezel adjustment feature, if enabled by the host controller, requires an additional frame of processing.

The DLPC120-Q1 is configured at power up by data stored in the flash file which stores configuration data, DMD and sequence timing information, LED drive information, and other information related to the system functions. See the *DLPC120-Q1 Programmer's Guide* for information about the this flash configuration data.

The transparent emissive display reference design from TI includes the TMS320F28023 Microcontroller (Piccolo), which is used to adjust the LED current levels in order to control the brightness levels and also the color point for systems with multiple color channels.

8.3 Application Mission Profile Consideration

Each application is anticipated to have different mission profiles, or number of operating hours at different temperatures. To assist in evaluation, the automotive DMD reliability lifetime estimates Application Report may be provided. See the TI Application team for more information.

8.4 Illumination Mission Profile Considerations

TI has performed evaluations at 405-nm illumination wavelengths under certain conditions. These conditions should be considered when evaluating the final application's implementation. Please contact the TI Application team for details about this testing.

9 Power Supply Recommendations

9.1 Power Supply Sequencing Requirements

- V_{BIAS}, V_{CC}, V_{OFFSET}, V_{REF}, V_{RESET}, V_{SS} are required to operate the DMD.

> **CAUTION**
>
> - For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power up and power down procedures may affect device reliability.
> - The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power up and power down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 19. V_{SS} must also be connected.

DMD Power Supply Power Up Procedure:

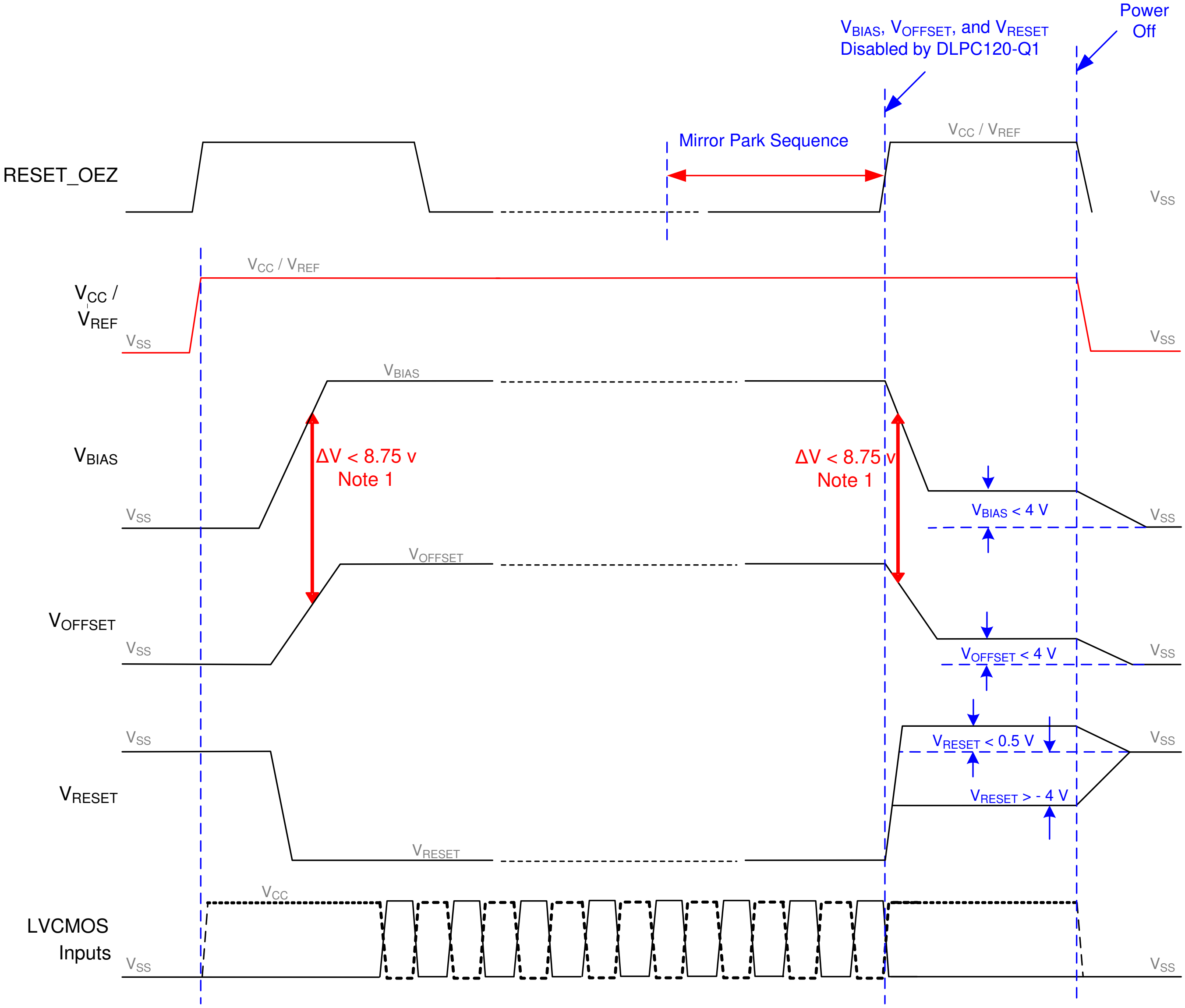
- During power up, V_{CC} and V_{REF} must always start and settle before V_{OFFSET}, V_{BIAS} and V_{RESET} voltages are applied to the DMD.
- During power up, V_{BIAS} does not have to start after V_{OFFSET}. However, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ±8.75 V (refer to Note 1 for Figure 19).
- During power up, the DMD's LVCMOS input pins shall not be driven high until after V_{CC} and V_{REF} have settled at operating voltage.
- During power up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power up are flexible, provided that the transient voltage levels follow the requirements listed above and in *Recommended Operating Conditions* and in Figure 19.

DMD Power Supply Power Down Procedure

- V_{CC} and V_{REF} must be supplied until after V_{BIAS}, V_{RESET} and V_{OFFSET} are discharged to within 4 V of ground.
- During power down it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within ± 8.75 V (refer to Note 1 for Figure 19).
- During power down, the DMD's LVCMOS input pins must be less than V_{REF} + 0.3 V.
- During power down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power down are flexible, provided that the transient voltage levels follow the requirements listed above in *Recommended Operating Conditions* and in Figure 19.

Power Supply Sequencing Requirements (continued)

9.1.1 Power Up and Power Down



(1) ±8.75-V delta, ΔV, shall be considered the max operating delta between V_{BIAS} and V_{OFFSET}. Customers may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power up and to remove V_{BIAS} prior to V_{OFFSET} during power down.

Figure 19. Power Supply Sequencing Requirements (Power Up and Power Down)

10 Layout

10.1 Layout Guidelines

Refer to *DLPC120-Q1 Data Sheet* for specific PCB layout and routing guidelines. For specific DMD PCB guidelines, use the following:

- V_{CC} should have at least one 2.2-µF and four 0.1-µF capacitors evenly distributed among the 13 V_{CC} pins.
- A 0.1-µF, X7R rated capacitor should be placed near every pin for the V_{REF}, V_{BIAS}, V_{RSET}, and V_{OFF}.

10.2 Temperature Diode Pins

The DMD has an internal diode (PN junction) that is intended to be used with an external TI TMP411-Q1 temperature sensing IC. PCB traces from the DMD's temperature diode pins to the TMP411-Q1 are sensitive to noise. See the *TMP411-Q1 Data Sheet* for specific routing recommendations.

Avoid routing the temperature diodes signals near other traces to avoid coupling of noise onto these signals.

10.3 Layout Example

Contact TI Application Engineering for access to the complete TI reference design PCB layout.

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

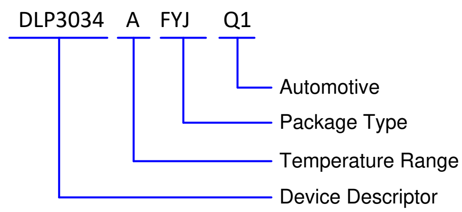


图 **20.** 器件型号 说明

11.1.2 器件标记

下面显示了器件标记。该标记将包括可读信息和一个二维矩阵码。

下面显示了可读信息。二维矩阵码是一个字母数字字符串，其中包含 DMD 部件号、序列号的第 1 部分和第 2 部分。

DMD 序列号（第 1 部分）的第一个字符为制造年份。DMD 序列号（第 1 部分）的第二个字符为制造月份。DMD 序列号（第 2 部分）的最后一个字符为偏置电压二进制字母。

示例： *DLP3034AFYJQ1 GHXXXXX LLLLLLM

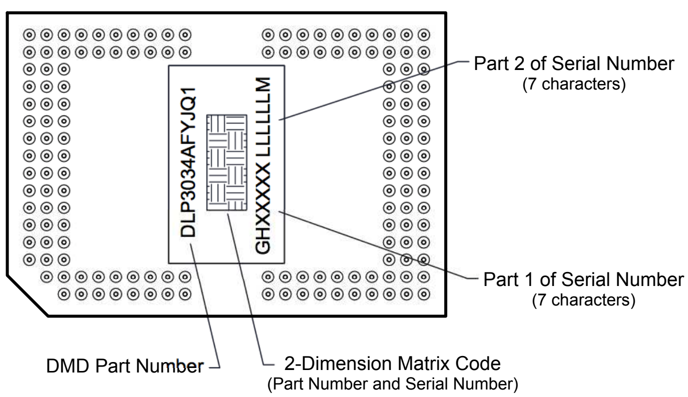


图 **21. DMD** 标记

下面显示了 DLP3034-Q1 器件的三维建模描述。

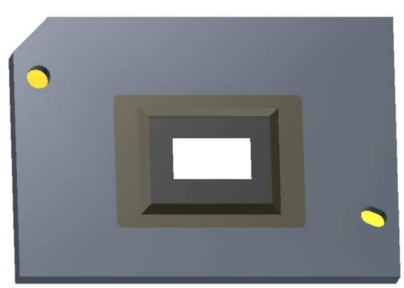


图 **22. DLP3034-Q1**的图像

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅：

- DLPC120-Q1 产品文件夹，以获取 *DLPC120-Q1 数据表*
- *《TMS320F2802x Piccolo™ 微控制器》*
- *《具有 N 因数和串联电阻校正的 TMP411-Q1 ±1°C 远程和本地温度传感器》*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 器件处理

DMD 是光学器件，故应注意避免损坏玻璃窗口。有关正确处理 DMD 的说明，请参阅《DMD 处理应用手册》。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3034AFYJQ1	ACTIVE	CPGA	FYJ	149	33	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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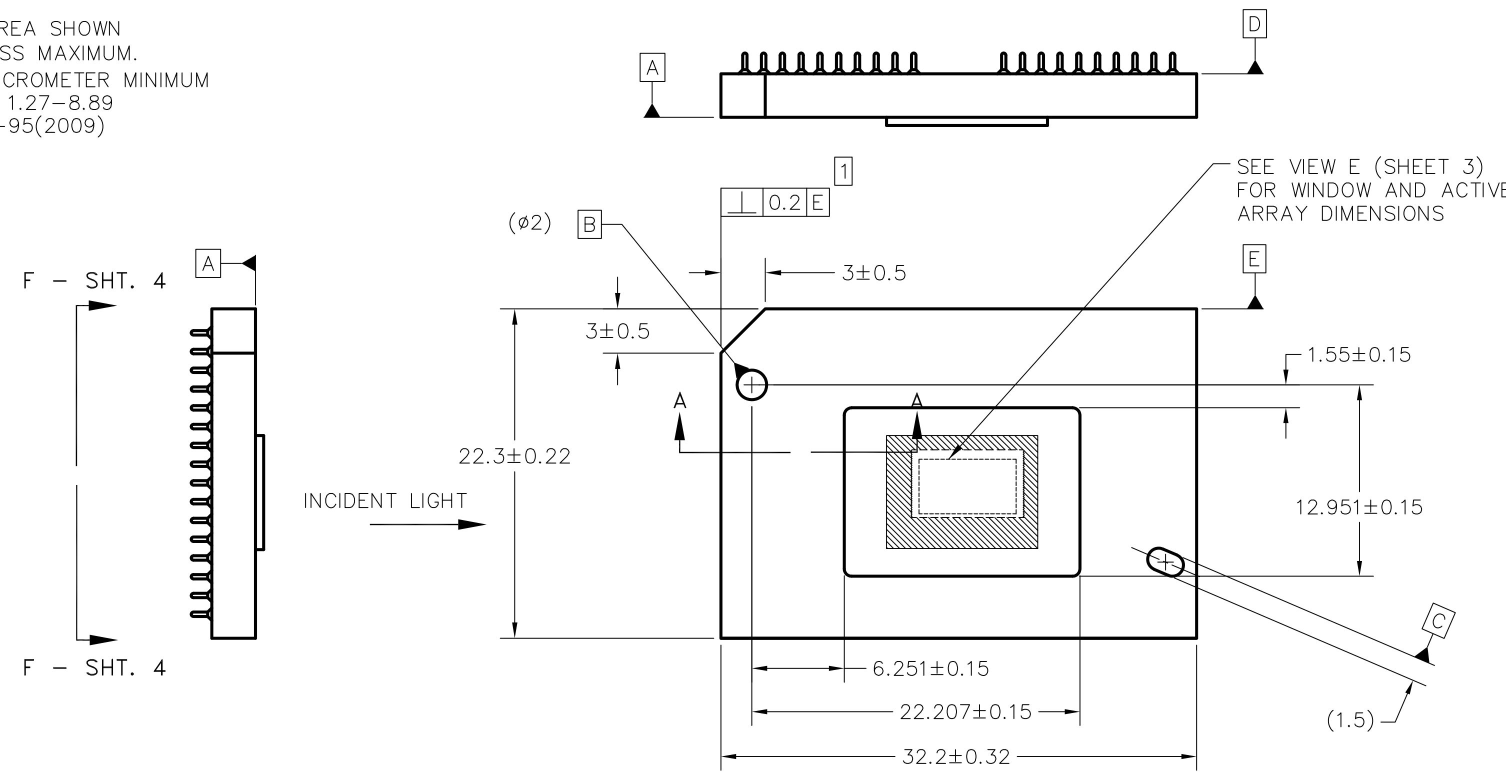
DWG NO 2514100 SH 1

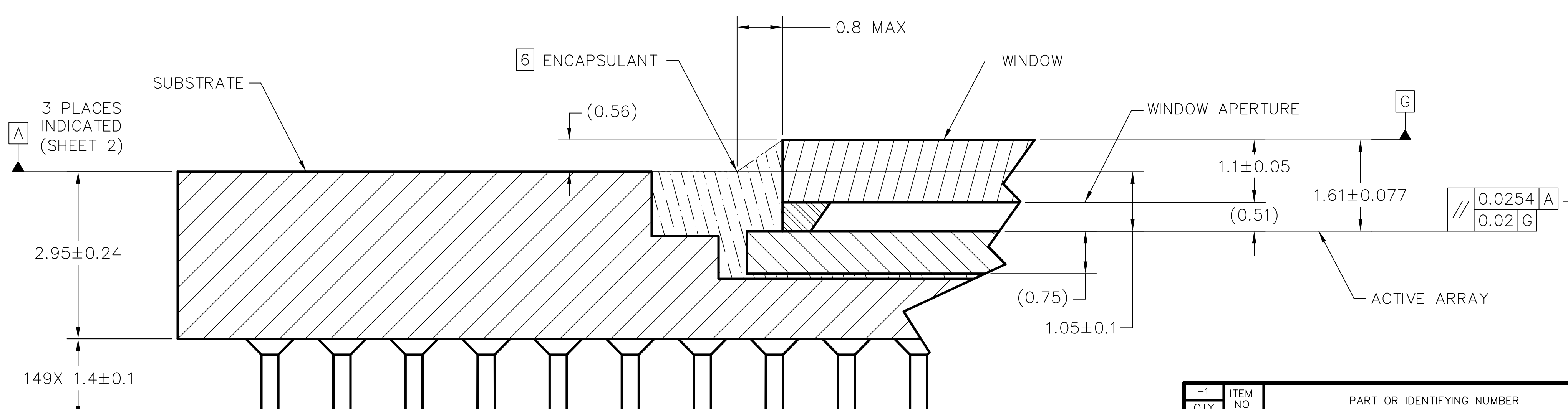
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2142364, INITIAL RELEASE	06/03/2014	M. AVERY
B	ECO 2153319, UPDATE PACKAGE DESIGNATOR IN TITLE BLOCK, NOTE 8 FIXED FOR Ni/Pd/Au, MOVED SUPPLIER CODE IN VIEW F-F.	09/11/2015	M. AVERY
C	ECO 2158233, UPDATE VIEW F-F 3 DIGIT P/N	05/18/2016	M. AVERY
D	ECO 2168572, CHG DIE HEIGHT TOL, WAS ± 0.08	08/25/2017	M. AVERY

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.2 THICKNESS MAXIMUM.
8. INDICATED CERAMIC SUBSTRATE FEATURES TO BE PLATED WITH 0.3 MICROMETER MINIMUM ELECTROLYTIC GOLD OVER 0.1 MICROMETER MINIMUM PALLADIUM OVER 1.27–8.89 MICROMETERS ELECTROLYTIC NICKEL PER ASTM B488-01, ASTM B679-95(2009) AND AMS-QQ-N-290, RESPECTIVELY.





SECTION A–A
SCALE 20/1

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- PARENTHETICAL INFO FOR REF ONLY

		DATE
DWN	M. AVERY	6/3/14
ENGR	M .AVERY	6/3/14
	B. HASKETT	6/5/14
QA	P. KONRAD	6/13/14
	R. LONG	6/20/14
CQE	M. DORAK	6/23/14
	S. SUSI	6/18/14

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON

APPLICATION

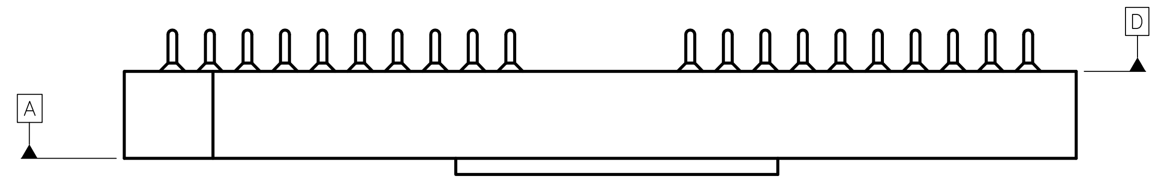
TEXAS INSTRUMENTS
Dallas, Texas

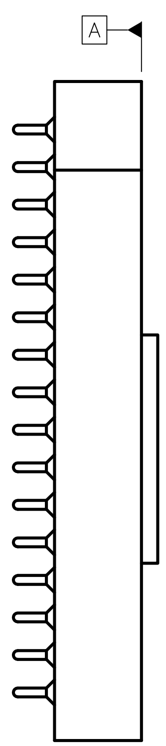
ICD, MECHANICAL, DMD
.3 WVGA DDR SERIES 450 –A1
(FYJ PACKAGE)

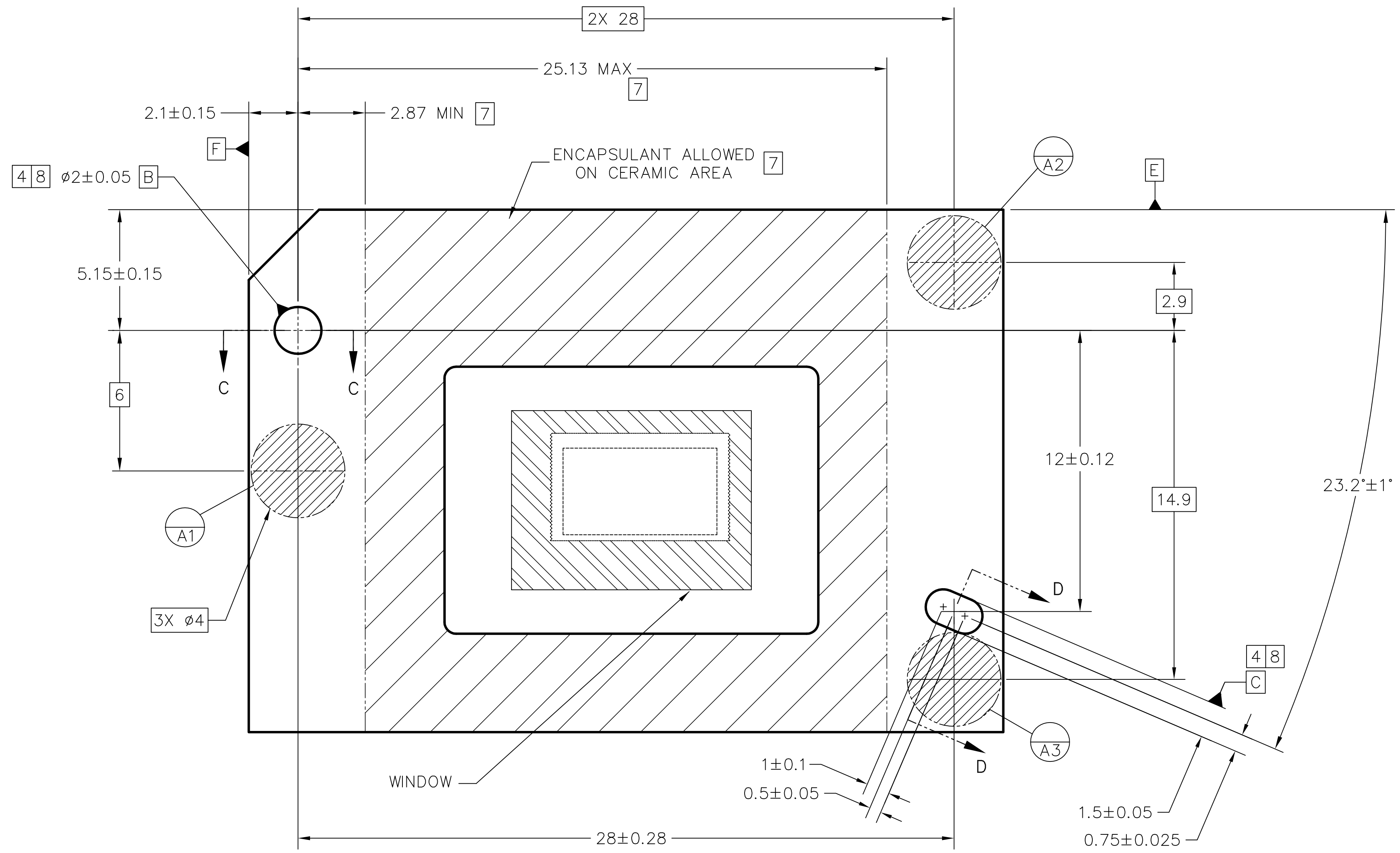
SIZE D — DRAWING NO 2514100 — REV D

SCALE 4/1 — SHEET 1 OF 4

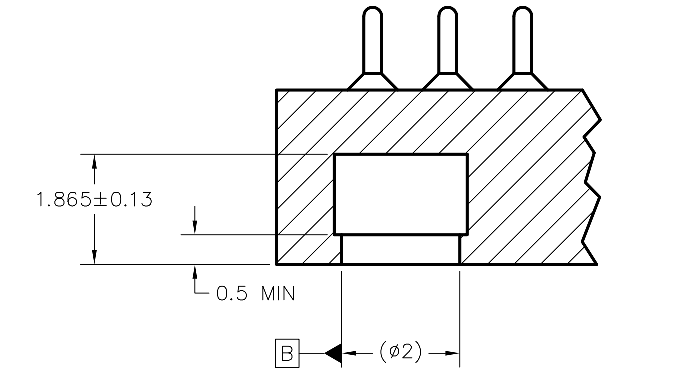
ACED1g



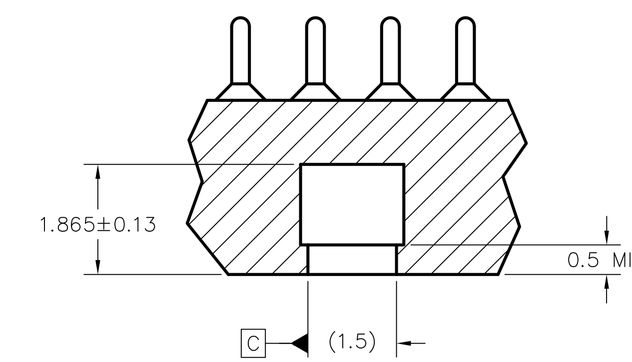




VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



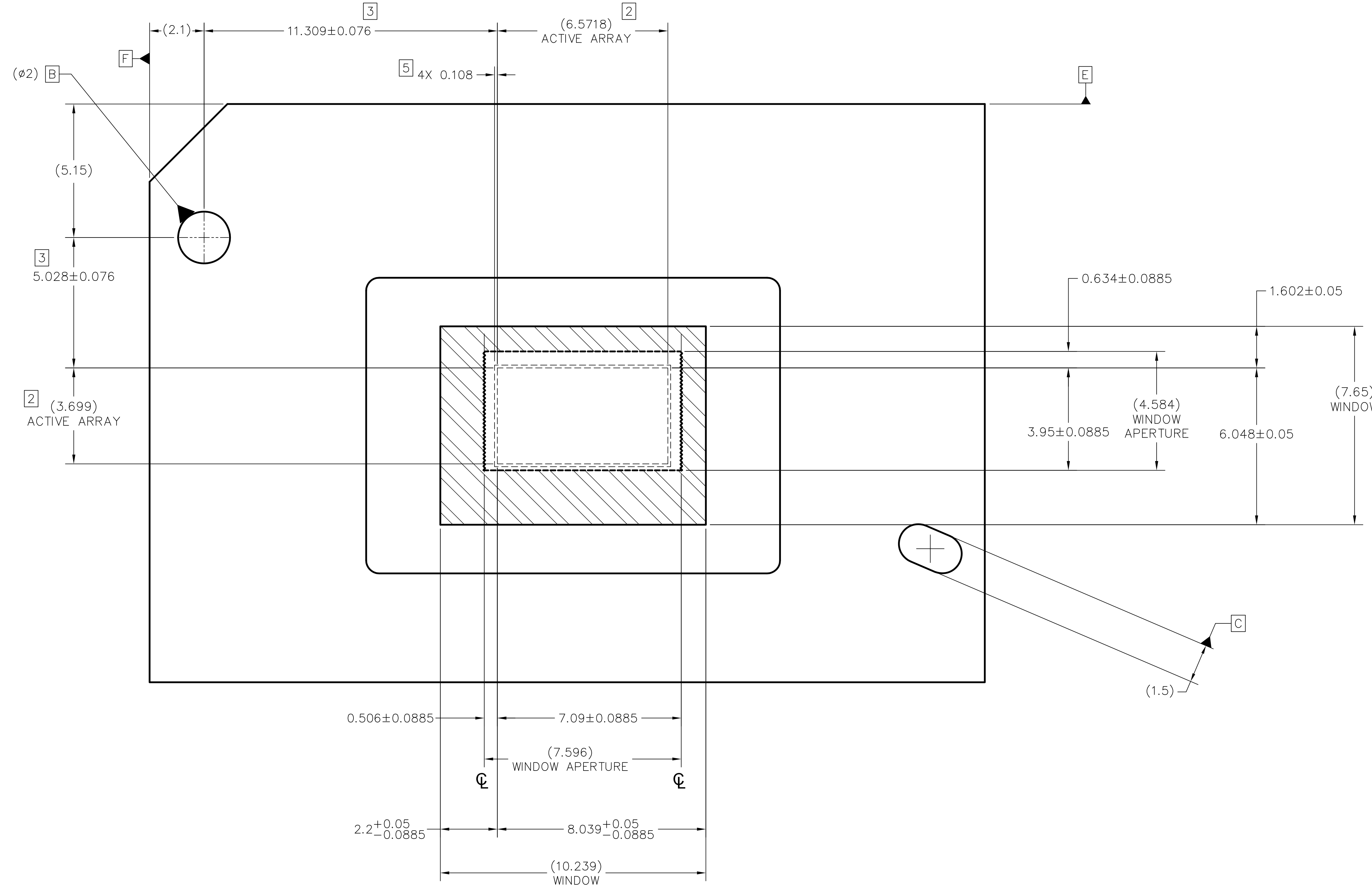
SECTION C–C
DATUM B
SCALE 16/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2514100	REV D
	ISSUE DATE		SCALE 4/1	SHEET 2	

ACED2c

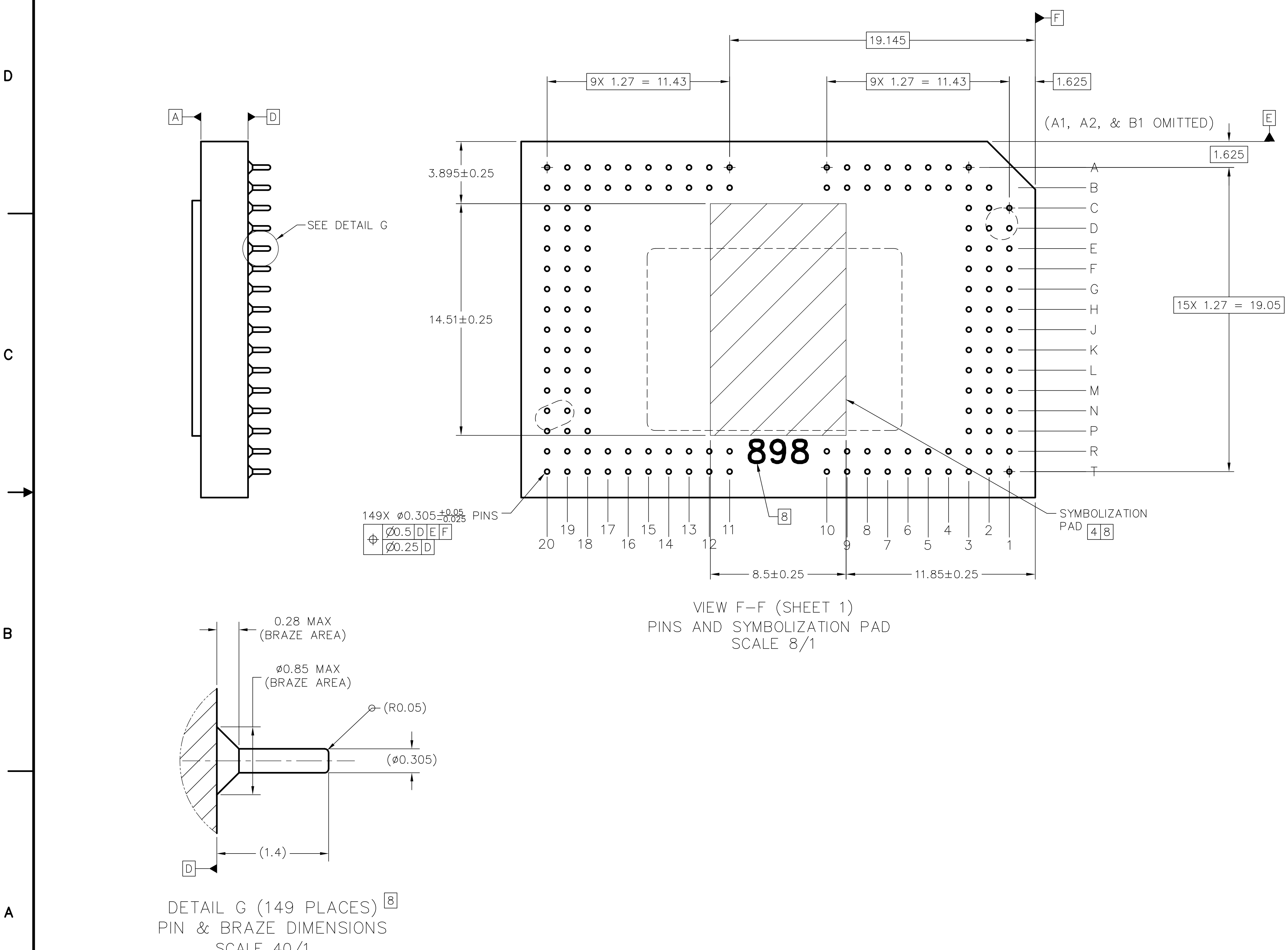


VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

TEXAS INSTRUMENTS Dallas, Texas	DWN / DATE / ISSUE DATE	SIZE D	DRAWING NO 2514100	REV D
		SCALE 4/1	SHEET 3	

DWG NO 2514100 SH 3

ACED2c



TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2514100	REV D
	ISSUE DATE		SCALE 4/1	SHEET 4	

ACED2c

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