DCV010505, DCV010505D, DCV010512, DCV010512D, DCV010515, DCV010515D, DCV011512D, DCV011515D, DCV012405, DCV012415D
ZHCSOO6C – AUGUST 2000 – REVISED AUGUST 2021

DCV01 系列 1W、1500V_{RMS} 隔离式非稳压直流/直流转换器模块

1 特性

- 1.5kV 隔离（运行）：1 秒测试
- 在隔离层中施加连续电压：60VDC/42.5VAC
- UL1950 认证元件
- EN55022 B 类 EMC 性能
- 7 引脚 PDIP 和 7 引脚 SOP 封装
- 输入电压：5V、15V 或 24V
- 输出电压：±5V、±12V 或 ±15V
- 器件间同步
- 过热保护
- 短路保护
- 高效率

2 应用

- 信号路径隔离
- 消除接地环路
- 数据采集
- 工业控制和仪表
- 测试设备

3 说明

DCV01 系列是一个 1W、1500Vrm 隔离式非稳压直流/直流转换器模块系列。DCV01 系列器件具有片上器件保护，只需要很少的外部元件即可提供额外的功能，例如输出禁用和开关频率同步。

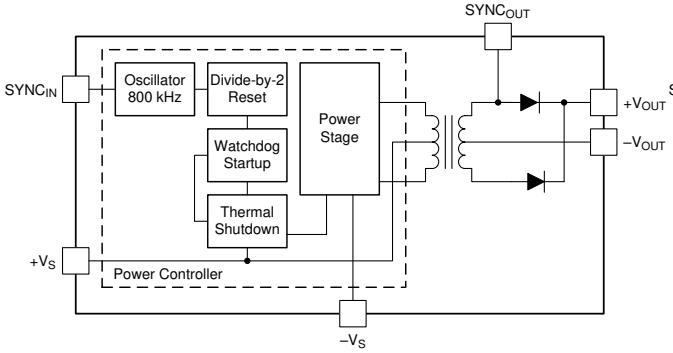
DCV01 系列器件集这些特性和较小的尺寸于一体，非常适合用于各种应用，并且对需要信号路径隔离的应用来说，它是一个易于使用的解决方案。

警告：此产品具有运行隔离功能，仅可用于信号隔离。不可用于需要增强型隔离的安全隔离电路。请参阅 节 8.3 中的定义。

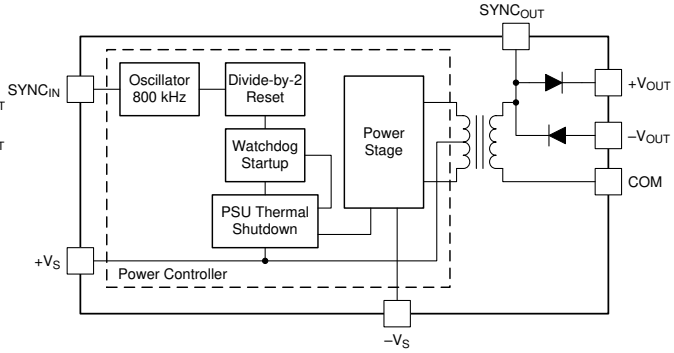
器件信息

器件型号	封装(1)	封装尺寸（标称值）
DCV01xxxx	PDIP (7)	19.18mm × 10.60mm
	SOP (7)	19.18mm × 10.60mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。



单路输出方框图



双路输出方框图

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Changes from Revision B (September 2016) to Revision C (August 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 ... 1
- 更新了 *节 1* ... 1
- 向 *节 2* 添加了链接 ... 1
- Added sentence in *节 8.3.1.3* ... 12
- Added *节 8.3.6* ... 13
- Added *节 8.3.7* ... 13
- Added *节 8.3.10* ... 14

Changes from Revision A (December 2013) to Revision B (September 2016) **Page**

- 更改了 *特性* ... 1
- 更改了 *应用* ... 1
- 添加了 *器件信息* 表、*器件比较* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 ... 1
- Deleted *Electrical Characteristics Per Device* table ... 6
- Added additional graphs to *Typical Characteristics* section ... 7
- Added *Isolation* subsection to *Feature Description* section ... 12
- Deleted *DCH, DCP, DCR, and DCV Series DC-DC Converters* subsection ... 12
- Deleted *Continuous Voltage* subsection ... 12
- Deleted references to DCP, DCR, DCR, and DCH series ... 12
- Added typical application design to *Application Information* section ... 17

5 Device Comparison Table

at T_A = 25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, and C_{OUT} = 0.1 µF (unless otherwise noted)

DEVICE NUMBER	INPUT VOLTAGE V_S (V)			OUTPUT VOLTAGE V_{NOM} at V_S (TYP) (V) 75% LOAD			DEVICE OUTPUT CURRENT (mA)(3)	LOAD REGULATION 10% TO 100% LOAD(1)		NO LOAD CURRENT I_Q (mA) 0% LOAD	EFFICIENCY (%) 100% LOAD	BARRIER CAPACITANCE C_{ISO} (pF) V_{ISO} = 750 Vrms
	MIN	TYP	MAX	MIN	TYP	MAX	MAX	TYP	MAX	TYP	TYP	TYP
DCV010505P DCV010505P-U	4.5	5	5.5	4.75	5	5.25	200	19	31	20	80	3.6
DCV010505DP DCV010505DP-U	4.5	5	5.5	±4.25	±5	±5.75	200(2)	18	32	22	81	3.8
DCV010512P DCV010512P-U	4.5	5	5.5	11.4	12	12.6	83	21	38	29	85	5.1
DCV010512DP DCV010512DP-U	4.5	5	5.5	±11.4	±12	±12.6	83(2)	19	37	40	82	4
DCV010515P DCV010515P-U	4.5	5	5.5	14.25	15	15.75	66	26	42	34	82	3.8
DCV010515DP DCV010515DP-U	4.5	5	5.5	±14.25	±15	±15.75	66(2)	19	41	42	85	4.7
DCV011512DP DCV011512DP-U	13.5	15	16.5	±11.4	±12	±12.6	83 (2)	11	39	19	78	2.5
DCV011515DP DCV011515DP-U	13.5	15	16.5	±14.25	±15	±15.75	66(2)	12	39	20	80	2.5
DCV012405P DCV012405P-U	21.6	24	26.4	4.75	5	5.25	200	13	23	14	77	2.5
DCV012415DP DCV012415DP-U	21.6	24	26.4	±14.25	±15	±15.75	66(2)	10	35	17	76	3.8

(1) Load regulation = (V_{OUT} at 10% load – V_{OUT} at 100%)/V_{OUT} at 75% load
(2) I_{OUT1} + I_{OUT2}
(3) $P_{OUT(max)}$ = 1 W

6 Pin Configuration and Functions

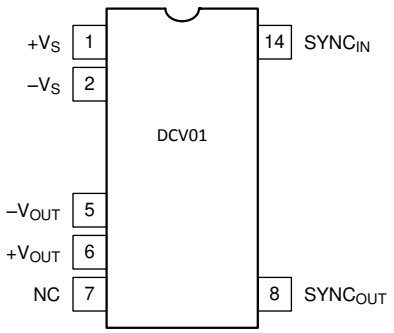


图 6-1. NVA, DUA Package 7-Pin PDIP, SOP (Single-Output) (Top View)

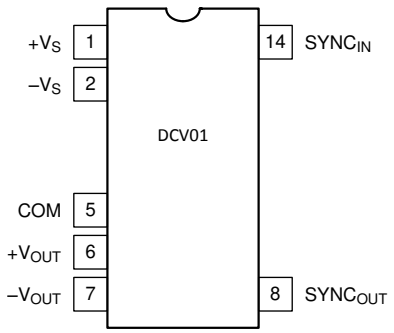


图 6-2. NVA, DUA Package 7-Pin PDIP, SOP (Dual-Output) (Top View)

表 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SINGLE-OUTPUT	DUAL-OUTPUT		
COM	—	5	O	Output side common
NC	7	—	—	No connection
$SYNC_{IN}$	14	14	I	Synchronization. Synchronize multiple devices by connecting the SYNC pins of each. Pulling this pin low disables the internal oscillator.
$SYNC_{OUT}$	8	8	O	Synchronization output. Unrectified transformer output

表 6-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	SINGLE-OUTPUT	DUAL-OUTPUT		
$+V_{OUT}$	6	6	O	Positive output voltage
$+V_S$	1	1	I	Input voltage
$-V_{OUT}$	5	7	O	Negative output voltage
$-V_S$	2	2	I	Input side common

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	5-V input devices			7	V
	15-V input devices			18	
	24-V input devices			29	
Lead temperature	PDIP package	Surface temperature of device body or pins (maximum 10 s)		270	°C
Reflow solder temperature	SOP package	Surface temperature of device body or pins		260	°C
Storage temperature, T_{stg}			–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	5-V input devices	4.5	5	5.5	V
	15-V input devices	13.5	15	16.5	
	24-V input devices	21.6	24	26.4	
Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		DCV01 NVA (PDIP) 7 PINS	DCV01 DVB (SOP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61	61	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	24	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, +V_S = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
P_{OUT}	Output power	I_{LOAD} = 100% (full load)			0.97		W
V_{RIPPLE}	Output voltage ripple	C_{OUT} = 1 µF, I_{LOAD} = 50%			20		mV_{PP}
	Voltage vs temperature	–40°C ≤ T_A ≤ 25°C			0.046%		°C
		25°C ≤ T_A ≤ 85°C			0.016%		°C
INPUT							
V_S	Input voltage			–10%		10%	
ISOLATION							
V_{ISO}	Isolation	1-second flash test	Voltage	1.5			kVrms
			dV/dt			500	V/s
			Leakage current			30	nA
		Continuous working voltage across isolation barrier	DC			60	VDC
			AC			42.5	VAC
LINE REGULATION							
	Output voltage	I_{OUT} ≥ 10% load current and constant, V_S (min) to V_S (typ)			1%	15%	
		I_{OUT} ≥ 10% load current and constant, V_S (typ) to V_S (max)			1%	15%	
RELIABILITY							
	Demonstrated	T_A = 55°C				75	FITS
THERMAL SHUTDOWN							
T_{SD}	Die temperature at shutdown				150		°C
I_{SD}	Shutdown current				3		mA

7.6 Switching Characteristics

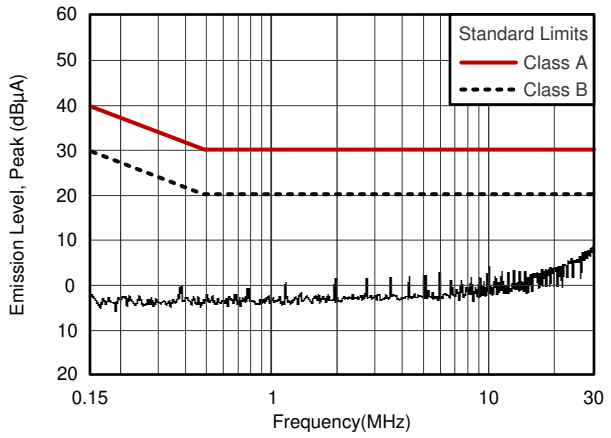
at T_A = 25°C, +V_S = nominal, C_{IN} = 2.2 µF, C_{OUT} = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	f_{SW} = f_{OSC}/2		800		kHz
V_{IL}	Low-level input voltage, SYNC		0		0.4	V
I_{SYNC}	Input current, SYNC	V_{SYNC} = 2 V		75		µA
$t_{DISABLE}$	Disable time			2		µs
C_{SYNC}	Capacitance loading on SYNC pin(1)	External			3	pF

(1) *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes this configuration.

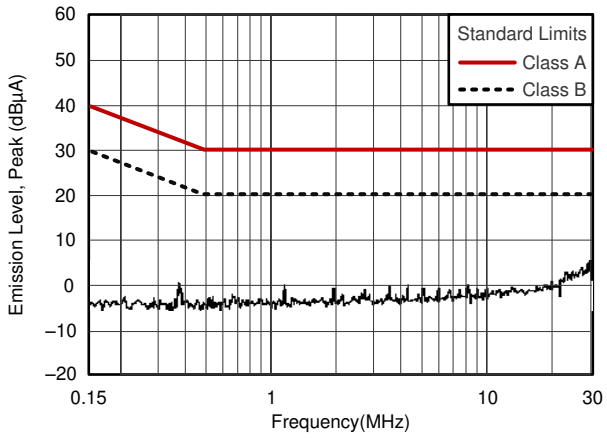
7.7 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



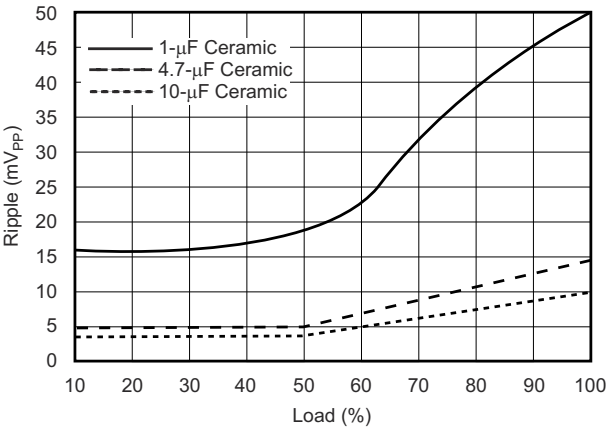
DCV010505 125% Load

图 7-1. Conducted Emissions



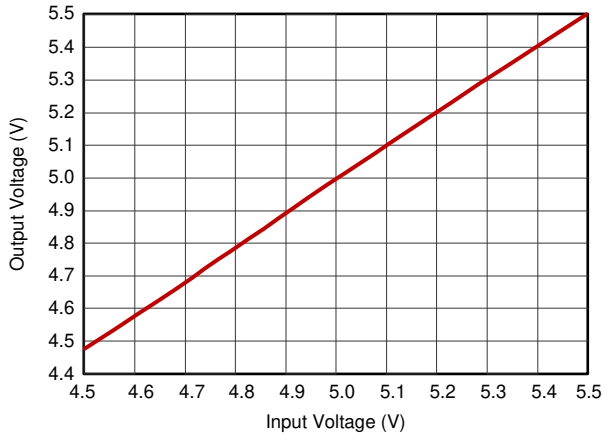
DCV010505 8% Load

图 7-2. Conducted Emissions



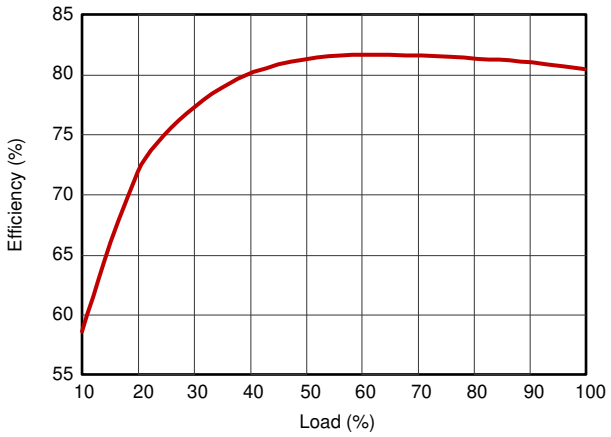
DCV010505 20-MHz BW

图 7-3. Output Ripple versus Load



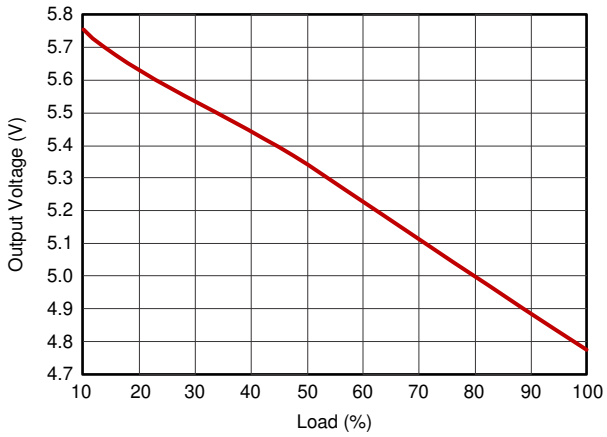
DCV010505

图 7-4. Line Regulation



DCV010505

图 7-5. Efficiency versus Load



DCV010505

图 7-6. Load Regulation

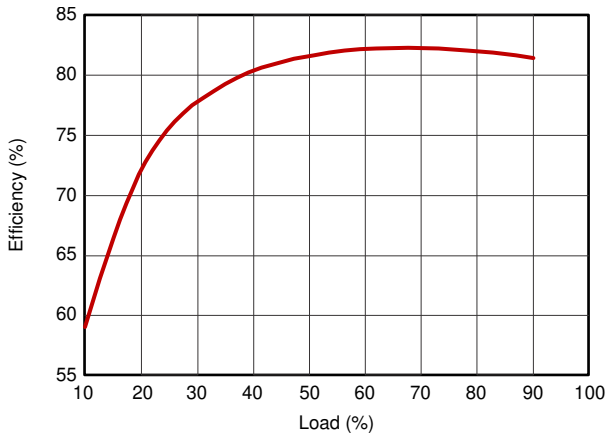


图 7-7. Efficiency versus Load

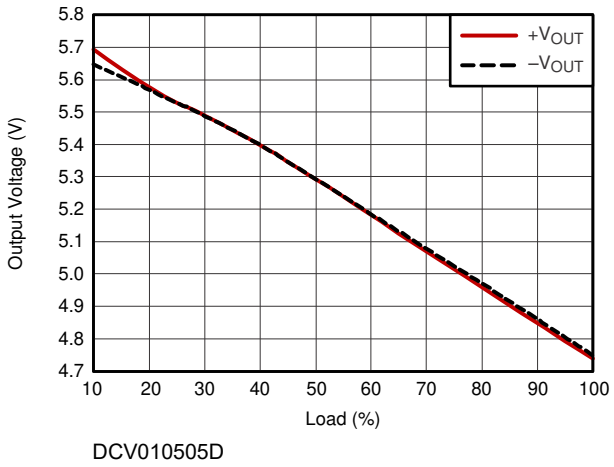


图 7-8. Load Regulation

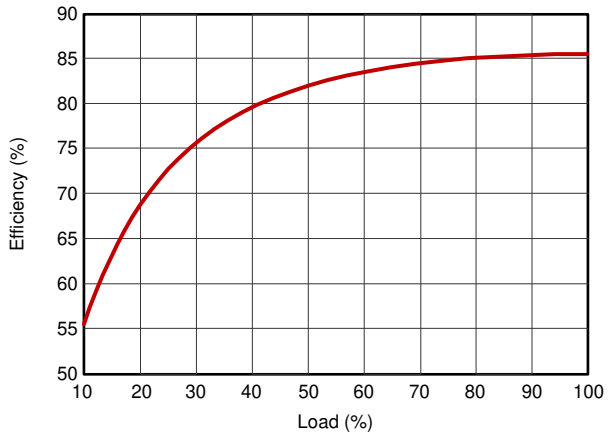


图 7-9. Efficiency versus Load

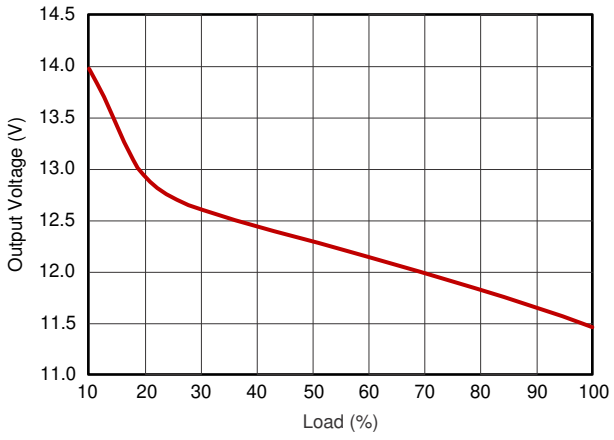


图 7-10. Load Regulation

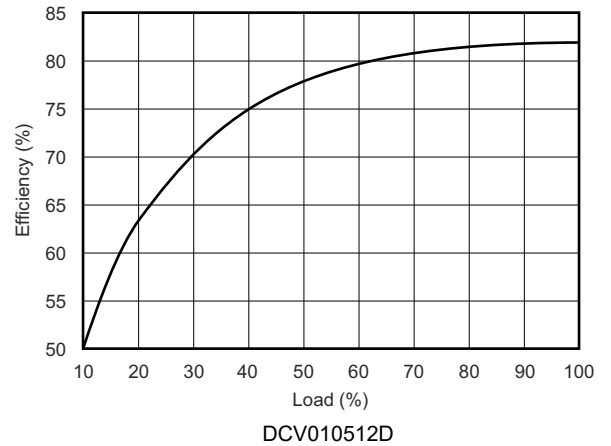


图 7-11. Efficiency versus Load

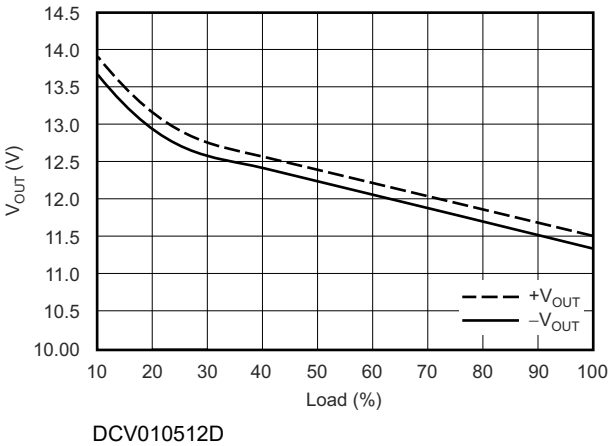


图 7-12. Load Regulation

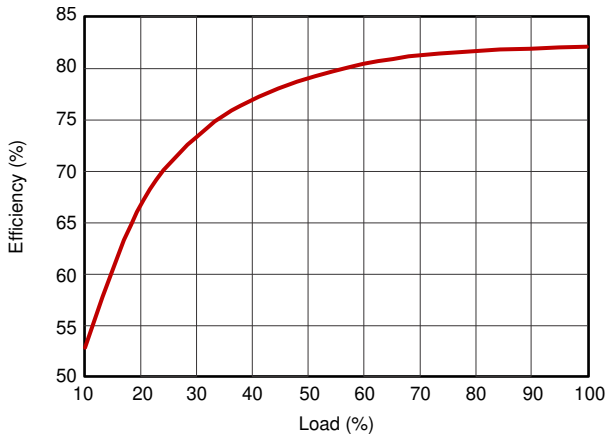


图 7-13. Efficiency versus Load

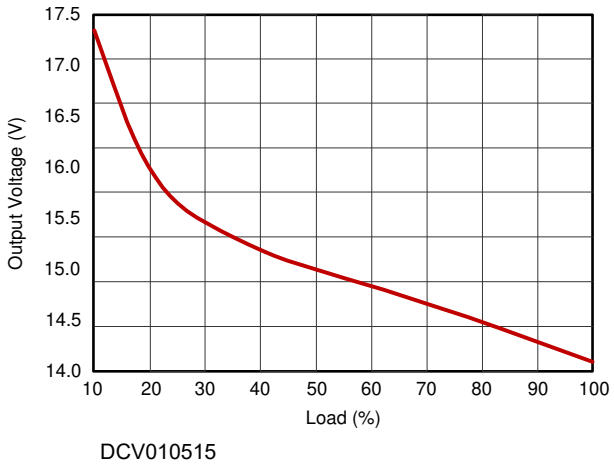


图 7-14. Load Regulation

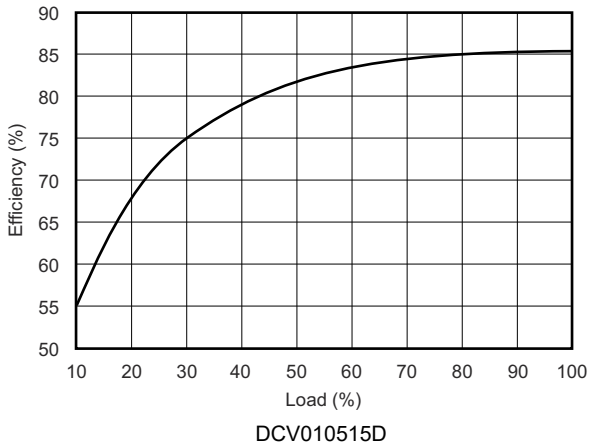


图 7-15. Efficiency versus Load

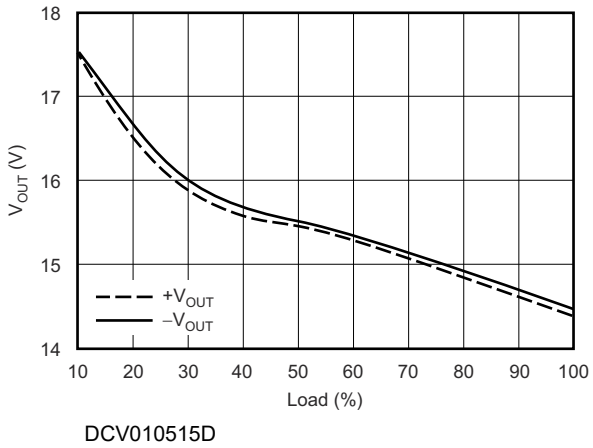


图 7-16. Load Regulation

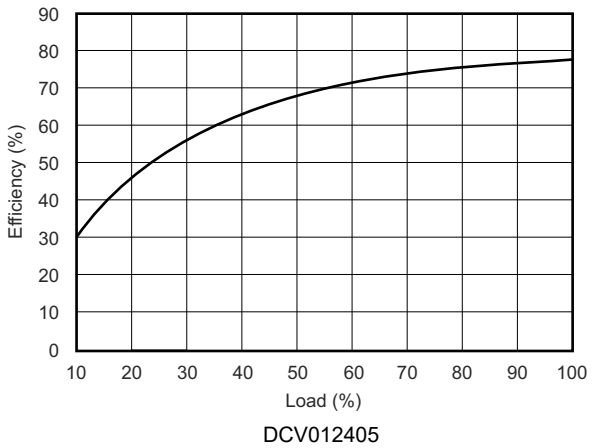


图 7-17. Efficiency versus Load

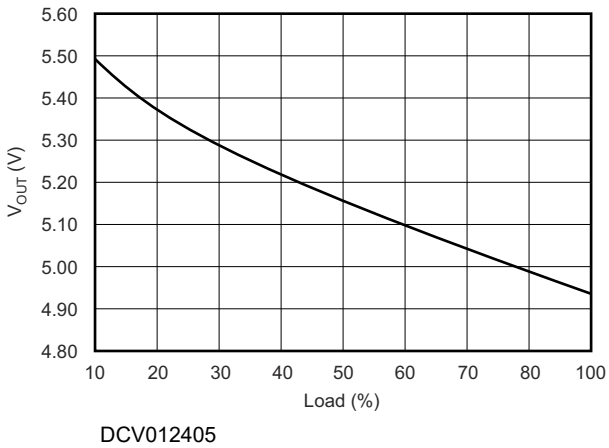


图 7-18. Load Regulation

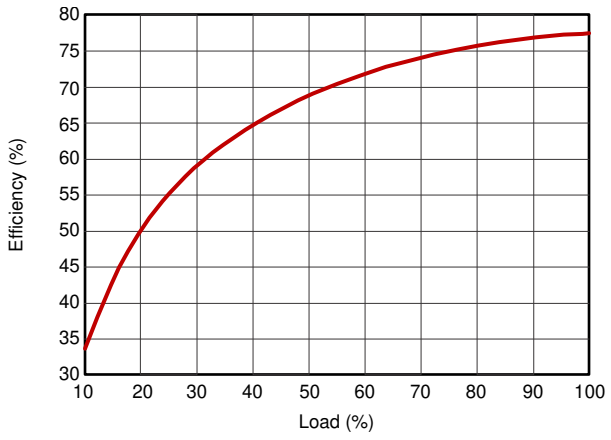


图 7-19. Efficiency versus Load

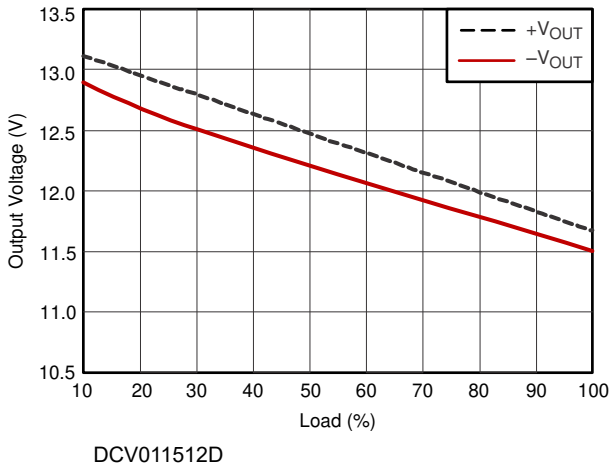


图 7-20. Load Regulation

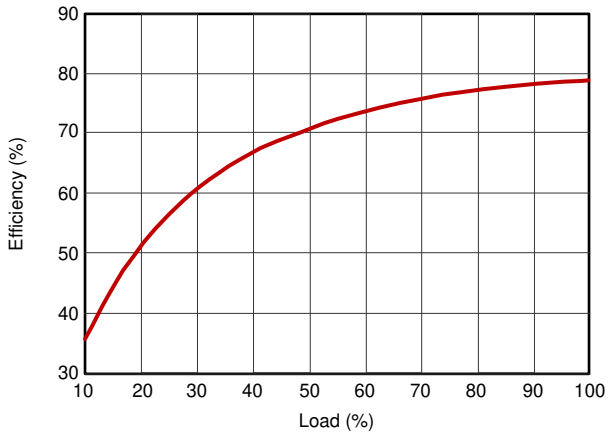


图 7-21. Efficiency versus Load

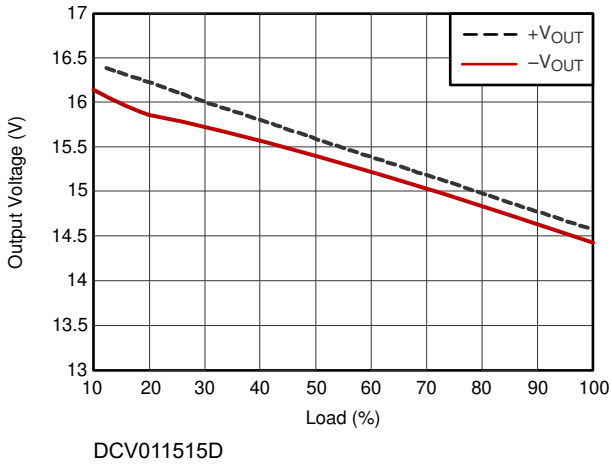


图 7-22. Load Regulation

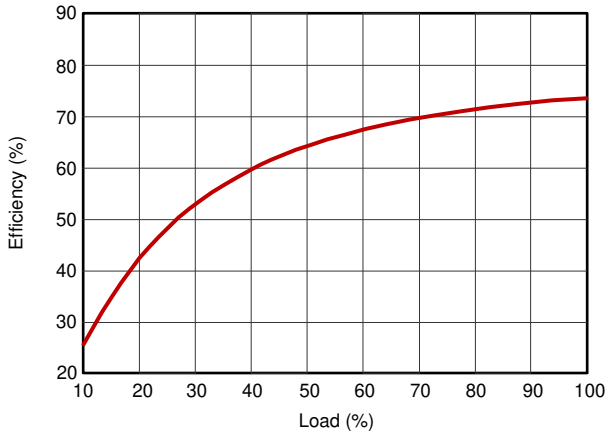


图 7-23. Efficiency versus Load

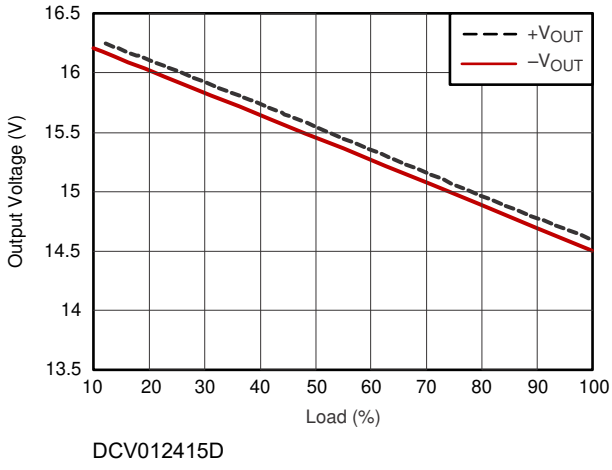


图 7-24. Load Regulation

8 Detailed Description

8.1 Overview

The DCV01 offers up to 1 W of isolated, unregulated output power from a 5-V, 15-V, or 24-V input source with a typical efficiency of up to 86%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCV01 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

8.2 Functional Block Diagrams

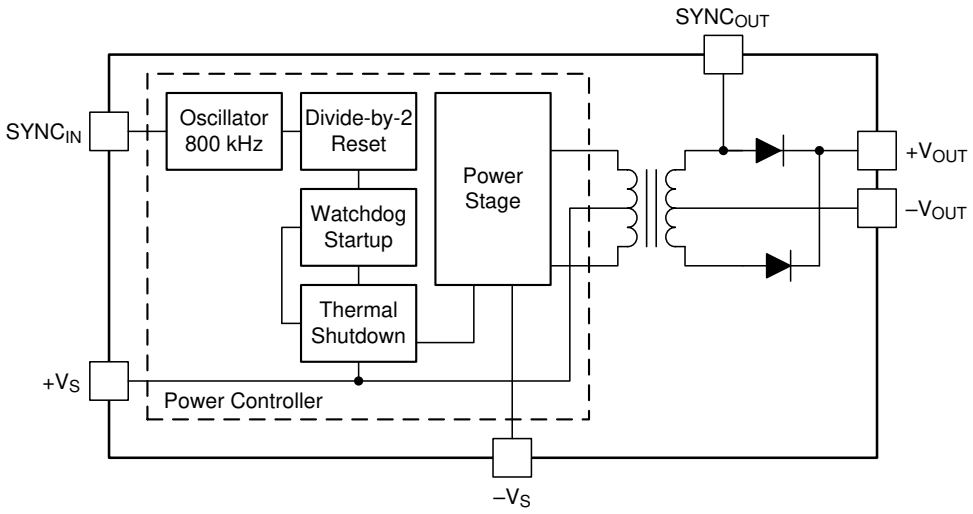


图 8-1. Single Output Device

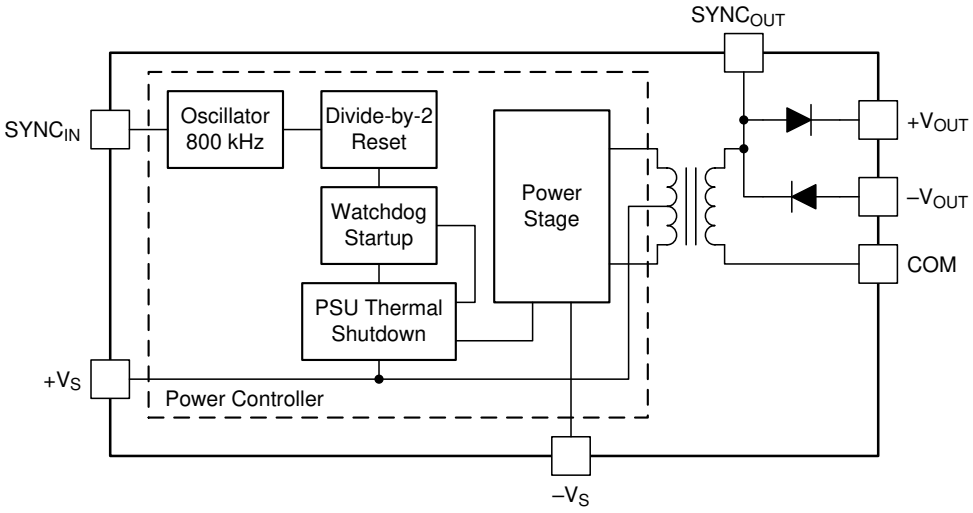


图 8-2. Dual Output Device

8.3 Feature Description

8.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.5 V_{RMS} or 60 V_{DC} peak.

8.3.1.1 Operation or Functional Isolation

The type of isolation used in the DCV01 products is referred to as operational or functional isolation. Insulated wire used in the construction of the transformer acts as the primary isolation barrier. A high-potential (hipot), one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

8.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

Note

The DCV01 products do not provide basic or enhanced isolation.

8.3.1.3 Working Voltage

For a device with operational isolation, the continuous working voltage that can be applied across the device in normal operation must be less than 42.5 V_{RMS} or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits.

WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.5 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

8.3.1.4 Isolation Voltage Rating

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* all relate to the same thing. These terms describe a test voltage that is applied across a component for a specified time, to verify the integrity of the isolation barrier of the component. TI’ s DCV01 series of DC/DC converters are all 100% production tested at 1.5 kV_{rms} for one second.

8.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCV01 series of DC/DC converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

8.3.2 Power Stage

The DCV01 series of devices use a push-pull, center-tapped topology. The DCV01 devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator).

8.3.3 Oscillator and Watchdog Circuit

The onboard, 800-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCV01 device circuits or an external source, and is used to minimize system noise.

A watchdog circuit monitors the operation of the oscillator circuit. The oscillator can be disabled by pulling the SYNC pin low. When the SYNC pin goes low, the output pins transition into tri-state mode, which occurs within 2 µs.

8.3.4 Thermal Shutdown

The DCV01 series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C, the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C. While the overtemperature condition continues, operation randomly cycles on and off. This cycling continues until the temperature is reduced.

8.3.5 Synchronization

When more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCV01 series of devices overcome this interference by allowing devices to be synchronized to one another. Synchronize up to eight devices by connecting the SYNC pins of each device, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) reduces the switching frequency, or can sometimes stop the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3 V.

For an application that uses more than eight synchronized devices use an external device to drive the SYNC pins. *External Synchronization of the DCP01/02 Series of DC/DC Converters* (SBAA035) describes this configuration.

Note

During the start-up period, all synchronized devices draw maximum current from the input simultaneously. If the input voltage falls below approximately 4 V, the devices may not start up. A ceramic capacitor must be connected close to the input pin of each device. Use a 2.2-µF capacitor for 5-V and 15-V input devices, and a 0.47-µF capacitor for the 24-V devices.

8.3.6 Light Load Operation (< 10%)

Operation below 10% load can cause the output voltage to increase up to double the typical output voltage. For applications that operate less than 10% of rated output current, it is recommended to add a minimum load to ensure the output voltage of the device is within the load regulation range. For example, connect a 250-Ω pre-load resistor to meet the 10% minimum load condition for the DCV010505P.

8.3.7 Load Regulation (10% to 100%)

The load regulation of the DCV01 series of devices are specified at 10% to 100% load. Placing a minimum of 10% load will ensure the output voltage is within the range specified in the 节 *7.5*. For more information regarding the operation below 10% load, see 节 *8.3.6*.

8.3.8 Construction

The basic construction of the DCV01 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCV01 series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any

special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

8.3.9 Thermal Management

Due to the high power density of this device, it is advisable to provide ground planes on the input and output rails.

8.3.10 Power-Up Characteristics

The DCV01 series of devices do not include a soft-start feature. Therefore, a high in-rush current during power-up is expected. To ensure a more stable start-up, allow the input voltage to be in regulation before enabling the device. Refer to the *节 8.4.1* section on how to disable/enable the device. 图 8-6 shows the typical start-up waveform for a DCV010505P when enabled after the input voltage is in regulation. 图 8-3 shows the typical start-up waveform for a DCV010505P, operating from a 5-V input with no load on the output. 图 8-4 shows the start-up waveform for a DCV010505P starting up into a 10% load. 图 8-5 shows the start-up waveform starting up into a full (100%) load.

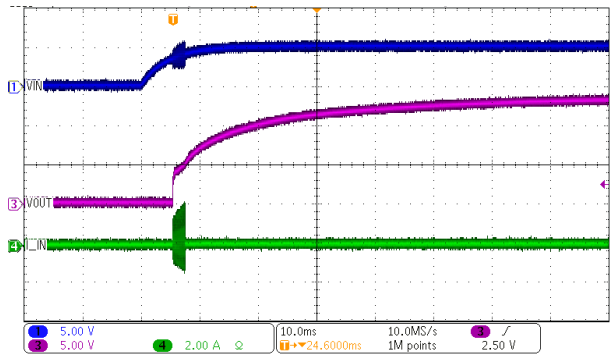


图 8-3. DCV010505P Start-Up at No Load

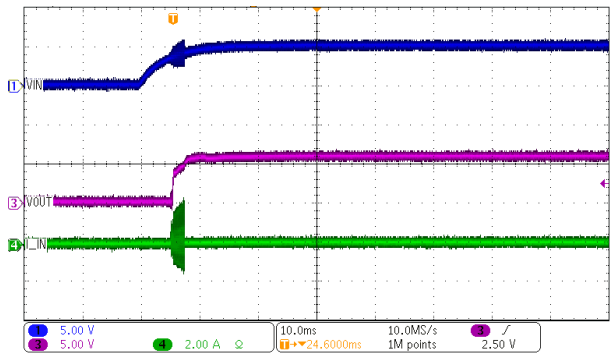


图 8-4. DCV010505P Start-Up at 10% Load

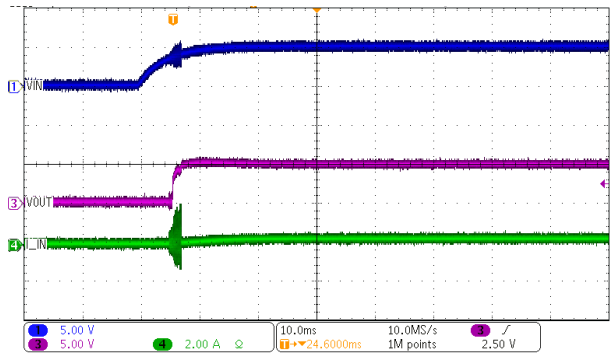


图 8-5. DCV010505P Start-Up at 100% Load

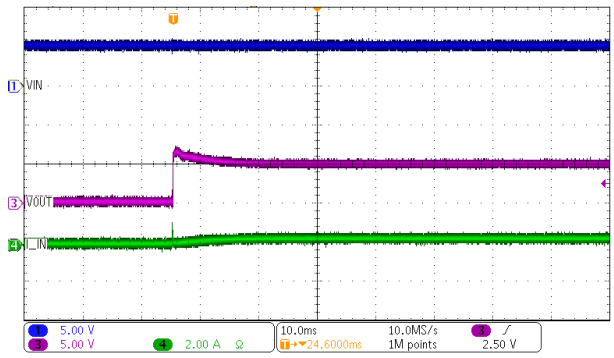


图 8-6. DCV010505P Enable Start-Up at 100% Load

8.4 Device Functional Modes

8.4.1 Disable and Enable ($SYNC_{IN}$ Pin)

Each of the DCV01 series devices can be disabled or enabled by driving the $SYNC_{IN}$ pin using an open-drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCV01 becomes disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2 µs. Removal of the pulldown causes the DCV01 to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin must be minimized ($\leqslant$ 3 pF) in order to prevent a reduction in the oscillator frequency. The *External Synchronization of the DCP01/02 Series of DC/DC Converters* application report (SBAA035) describes disable/enable control circuitry.

8.4.2 Decoupling

8.4.2.1 Ripple Reduction

The high switching frequency of 400 kHz allows simple filtering. To reduce ripple, TI recommends that a minimum of 1-µF capacitor be used on the $+V_{OUT}$ pin. For dual output devices, decouple both of the outputs to the COM pin. The required 2.2-µF, low ESR ceramic input capacitor also helps to reduce ripple and noise, (24-V input voltage versions require only 0.47 µF of input capacitance). See the *DC-to-DC Converter Noise Reduction* application report (SBVA012).

8.4.2.2 Connecting the DCV01 in Series

Multiple DCV01 devices can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCV01.

Connect the $+V_{OUT}$ from one DCV01 to the $-V_{OUT}$ of another (see 图 8-7). If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCV01 prevents beat frequencies on the voltage rails. The synchronization feature of the DCV01 allows easy series connection without external filtering, thus minimizing cost.

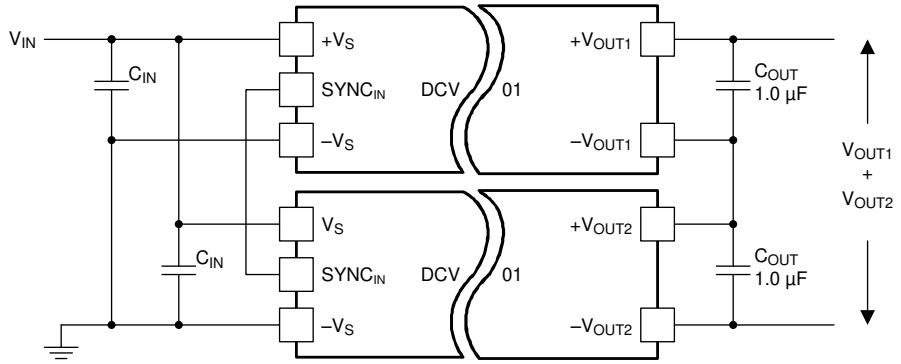


图 8-7. Multiple DCV01 Devices Connected in Series

The outputs of a dual-output DCV01 can also be connected in series to provide two times the magnitude of $+V_{OUT}$, as shown in 图 8-8. For example, connect a dual-output, 15-V, DCP012415D device to provide a 30-V rail.

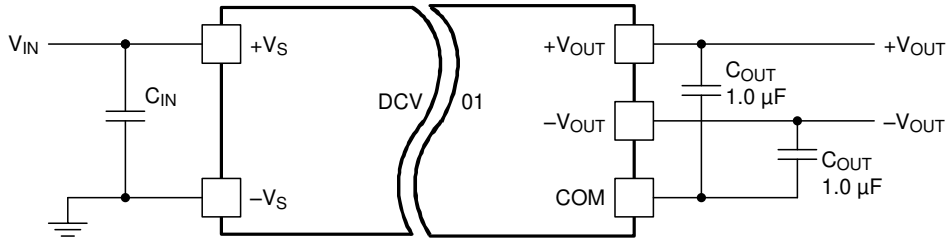


图 8-8. Dual Output Devices Connected in Series

8.4.2.3 Connecting the DCV01 in Parallel

If the output power from one DCV01 is not sufficient, it is possible to parallel the outputs of multiple DCV01s, as shown in 图 8-9 (applies to single output devices only). The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

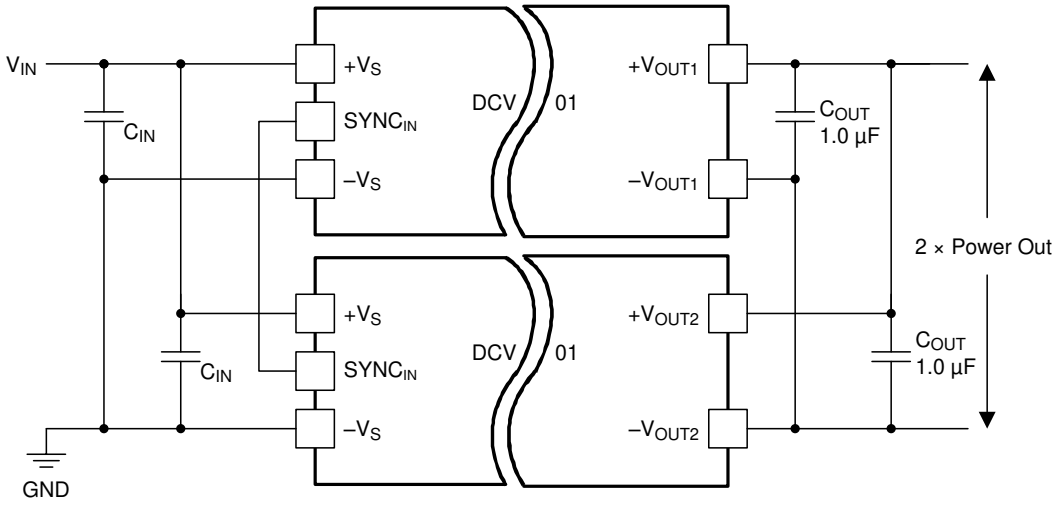


图 8-9. Multiple DCV01 Devices Connected in Parallel

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The DCV01 devices offer up to 1 W of isolated, unregulated output power from a 5-V, 15-V, or 24-V input supply. Applications requiring up to 1.5-kVrms of operational isolation benefit from the small size and ease-of-use of the DCV01 family of devices.

9.2 Typical Application

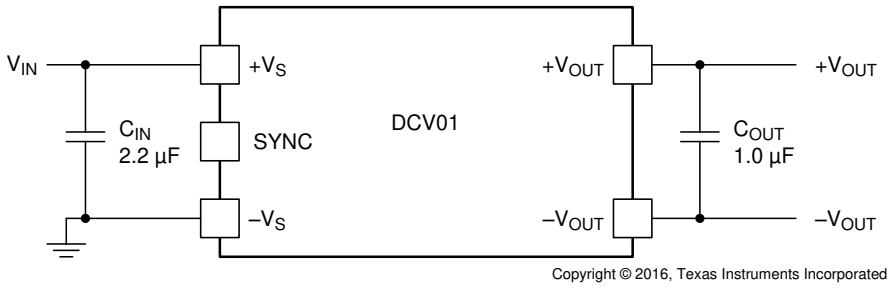


图 9-1. DCV010505 Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 and follow the procedures in the 节 9.2.2.

表 9-1. Design Example Parameters

PARAMETER		VALUE
$V_{(+VS)}$	Input voltage	5 V
$V_{(+VOUT)}$	Output voltage	5 V
I_{OUT}	Output current rating	200 mA
f_{SW}	Operating frequency	400 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor

For all 5-V and 15-V input voltage designs, select a 2.2-µF low-ESR ceramic input capacitor to ensure a good start-up performance. 24-V input applications require only 0.47 µF of input capacitance.

9.2.2.2 Output Capacitor

For any DCV01 design, select a 1-µF low-ESR ceramic output capacitor to reduce output ripple.

9.2.2.3 $SYNC_{IN}$ Pin

In a stand-alone application, leave the $SYNC_{IN}$ pin floating.

9.2.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by using wide ground and power traces or planes. If several devices are being powered from a common power source, a star-connected layout must be used. Device inputs must not be connected in series, as this will cascade the resistive losses. The position of the decoupling capacitors is important to reduce losses. Place the decoupling capacitors as close to the devices as possible. See the *PCB Layout* for more details.

9.2.2.5 Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in 图 9-2). In 图 9-2, X_C is the reactance due to the capacitance, X_L is the reactance due to the ESL, and f_0 is the resonant frequency. As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

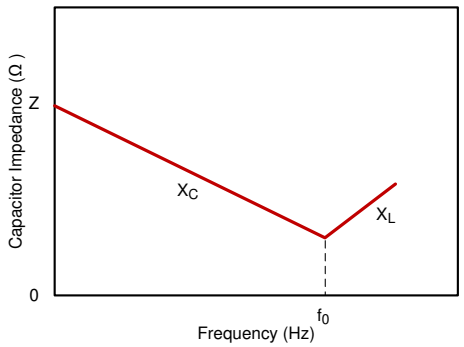


图 9-2. Capacitor Impedance versus Frequency

At f_0, $X_C = X_L$; however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance; namely, the value of the ESR. The resonant frequency must be well above the 800-kHz switching frequency of the device.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in 方程式 1.

$$V_{IN} = V_{PK} - (ESR \times I_{TR}) \quad (1)$$

where

- V_{IN} is the voltage at the device input
- V_{PK} is the maximum value of the voltage on the capacitor during charge
- I_{TR} is the transient load current

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), ESR is the dominant factor.

9.2.2.6 Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic (and has an ESR greater than 20 mΩ), then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. If the voltage falls below approximately 4 V, the DCV01 detects an undervoltage condition and switches the DCV01 drive circuits to a momentary off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage results in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value, at which time the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process repeats until the input capacitor charges sufficiently to start the device correctly.

Normal start-up must occur in approximately 1 ms after power is applied to the device. If a considerably longer start-up duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5-V to 15-V input devices, a 2.2-µF, low-ESR ceramic capacitor ensures a good start-up performance. For 24-V input voltage devices, TI recommends 0.47-µF ceramic capacitors. Tantalum capacitors are not recommended, because most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, designers must pay close attention to both the ESR and voltage as derated by the vendor.

Note

During the start-up period, these devices can draw maximum current from the input supply. If the input voltage falls below approximately 4 V, the devices may not start up. Connect a 2.2-µF ceramic capacitor close to the input pins.

9.2.2.7 Ripple and Noise

A good quality, low-ESR ceramic capacitor placed as close as possible across the input reduces reflected ripple and ensures a smooth start-up.

A good quality, low-ESR ceramic capacitor placed as close as possible across the rectifier output terminal and output ground gives the best ripple and noise performance. See the *DC-to-DC Converter Noise Reduction* application report (SBVA012) for more information on noise rejection.

9.2.2.7.1 Output Ripple Calculation Example

The following example shows that increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

To calculate the output ripple for a DCV010505 device:

- V_{OUT} = 5 V
- I_{OUT} = 0.2 A
- At full output power, the load resistor is 25 Ω
- Output capacitor of 1 µF, ESR of 0.1 Ω
- Capacitor discharge time 1% of 800 kHz (ripple frequency)
- t_{DIS} = 0.0125 µs
- $\tau = C \times R_{LOAD}$
- $\tau = 1 \times 10^{-6} \times 25 = 25$ µs
- $V_{DIS} = V_O(1 - EXP(-t_{DIS} / \tau))$
- V_{DIS} = 2.5 mV

By contrast, the voltage dropped because of ESR:

- $V_{ESR} = I_{LOAD} \times ESR$
- $V_{ESR} = 0.2 \times 0.1 = 20$ mV
- Ripple voltage = 22.5 mV

9.2.2.8 Dual DCV01 Output Voltage

The voltage output for dual DCV01 devices is half-wave rectified; therefore, the discharge time is 1.25 µs. Repeating the previous calculations using the 100% load resistance of 50 Ω (0.1 A per output), the results are:

- τ = 50 µs
- t_{DIS} = 1.25 µs
- V_{DIS} = 123 mV
- $V_{ESR} = 0.1 \times 0.1 = 10$ mV
- Ripple Voltage = 133 mV

In this example, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to 10 µF, and repeating the calculations, the result is that the ripple voltage is 22.3 mV.

This value is composed of almost equal components.

The previous calculations are offered as a guideline only. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

9.2.2.9 Optimizing Performance

Optimum performance can only be achieved if the device is correctly supported. The very nature of a switching converter requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not experience this transient (this is analogous to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected through a low-impedance path.

The optimum performance primarily depends on two factors:

- Connection of the input and output circuits for minimal loss.
- The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

9.2.3 Application Curves

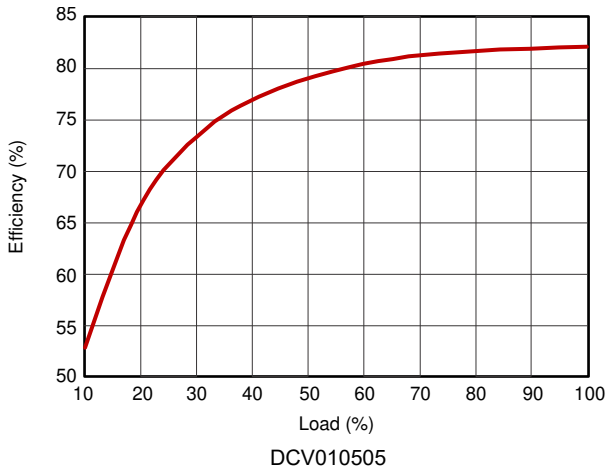
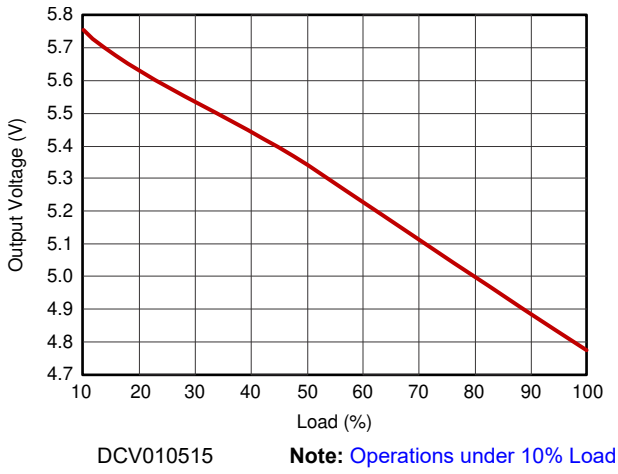


图 9-3. Efficiency versus Load



Note: Operations under 10% Load

图 9-4. Load Regulation

10 Power Supply Recommendations

The DCV01 is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCV01. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

11 Layout

11.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output.

图 11-1 shows a schematic for two DCV01 devices. 图 11-2 and 图 11-3 show a typical layout for two through-hole PDIP devices.

Input power and ground planes provide a low-impedance path for the input power. For the output, the COM signal connects through a ground plane, while the connections for the positive and negative voltage outputs conduct through wide traces to minimize losses.

The output must be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

Allow the unused SYNC pin, to remain configured as a floating pad. It is advisable to place a guard ring (connected to input ground) or annulus connected around this pin to avoid any noise pickup. When connecting a SYNC pin to one or more SYNC design the linking trace to be short and narrow to avoid stray capacitance. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

11.2 Layout Example

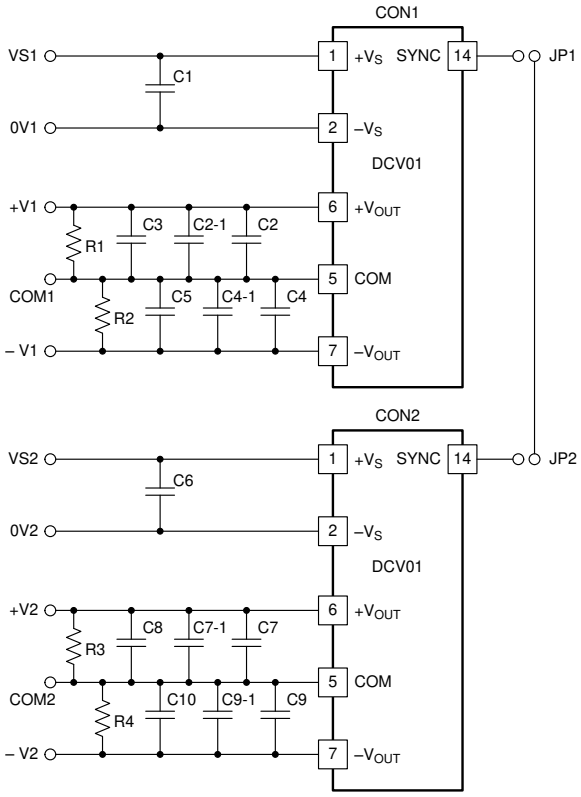


图 11-1. PCB Schematic, P and U Package

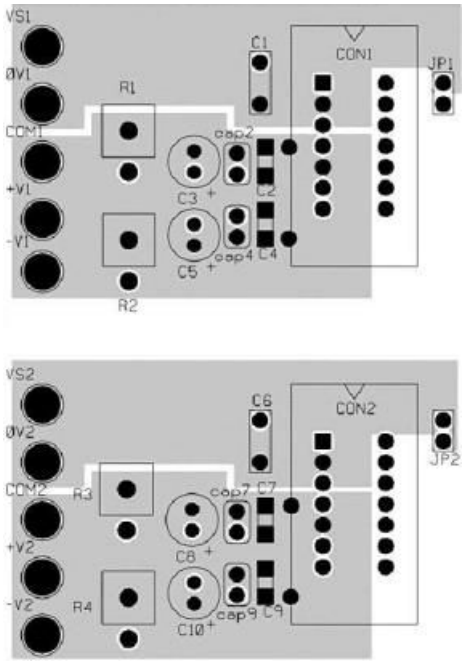


图 11-2. PCB Layout Example, Component-Side View

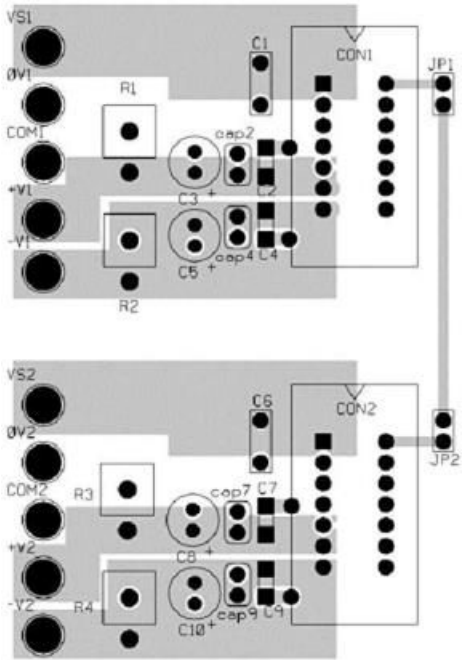


图 11-3. PCB Layout Example, Non-Component-Side View

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

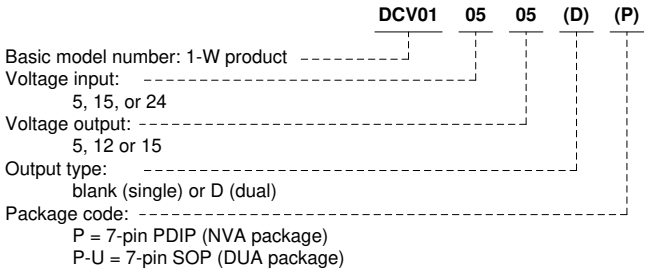


图 12-1. Supplemental Ordering Information

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *External Synchronization of the DCP01/02 Series of DC/DC Converters* (SBAA035)
- Texas Instruments, *DC-to-DC Converter Noise Reduction* (SBVA012)
- Texas Instruments, *Optimizing Performance of the DCP01/02 Series of DC/DC Converters* (SBVA013)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DCV010505DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010505DP
DCV010505DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010505DP-U
DCV010505P	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010505P
DCV010505P-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010505P-U
DCV010505P-U/700	Active	Production	SOP (DUA) | 7	700 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010505P-U
DCV010512DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010512DP
DCV010512DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV10512DPU
DCV010512P	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010512P
DCV010512P-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010512P-U
DCV010515DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010515DP
DCV010515DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010515DP-U
DCV010515P	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV010515P
DCV010515P-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV010515P-U
DCV011512DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV011512DP
DCV011512DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV011512DP-U
DCV011515DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV011515DP
DCV011515DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV011515DP-U
DCV011515DP-U/700	Active	Production	SOP (DUA) | 7	700 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV011515DP-U
DCV012405P	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV012405P
DCV012405P-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV012405P-U
DCV012415DP	Active	Production	PDIP (NVA) | 7	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	DCV012415DP
DCV012415DP-U	Active	Production	SOP (DUA) | 7	25 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV012415DP-U
DCV012415DP-U/700	Active	Production	SOP (DUA) | 7	700 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCV012415DP-U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

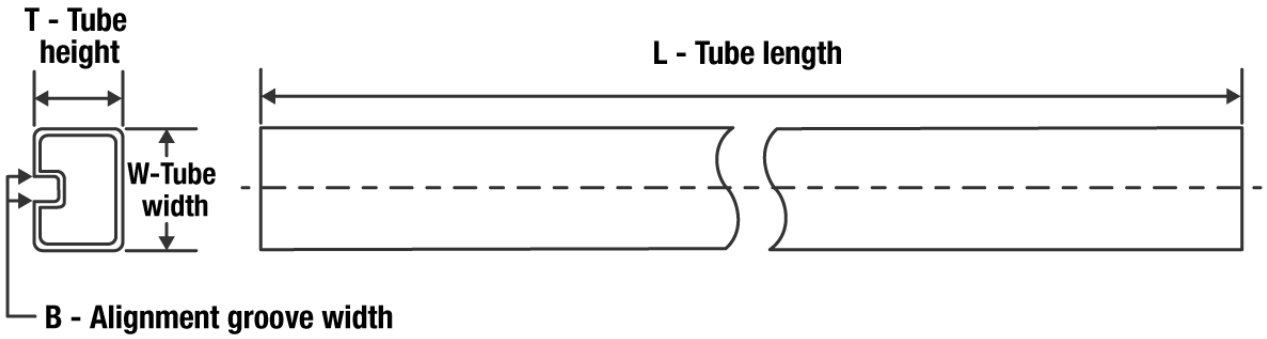
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

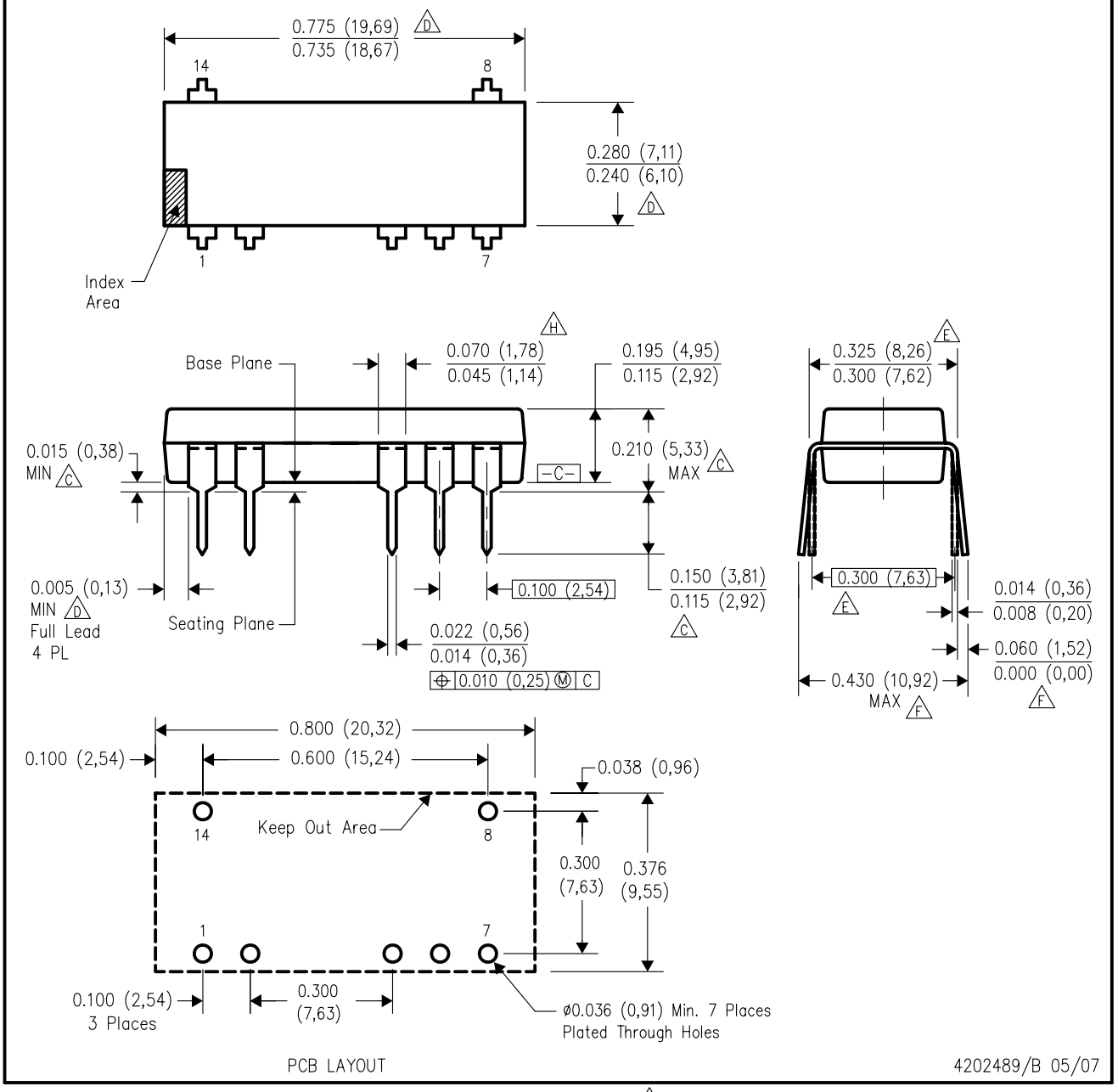
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DCV010505DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV010505P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV010512DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV010512P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV010512P-U	DUA	SOP	7	25	532.13	13.51	7.36	6.91
DCV010515DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV010515P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV011512DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV011515DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV012405P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCV012415DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07

NVA (R–PDIP–T7/14) PLASTIC DUAL–IN–LINE

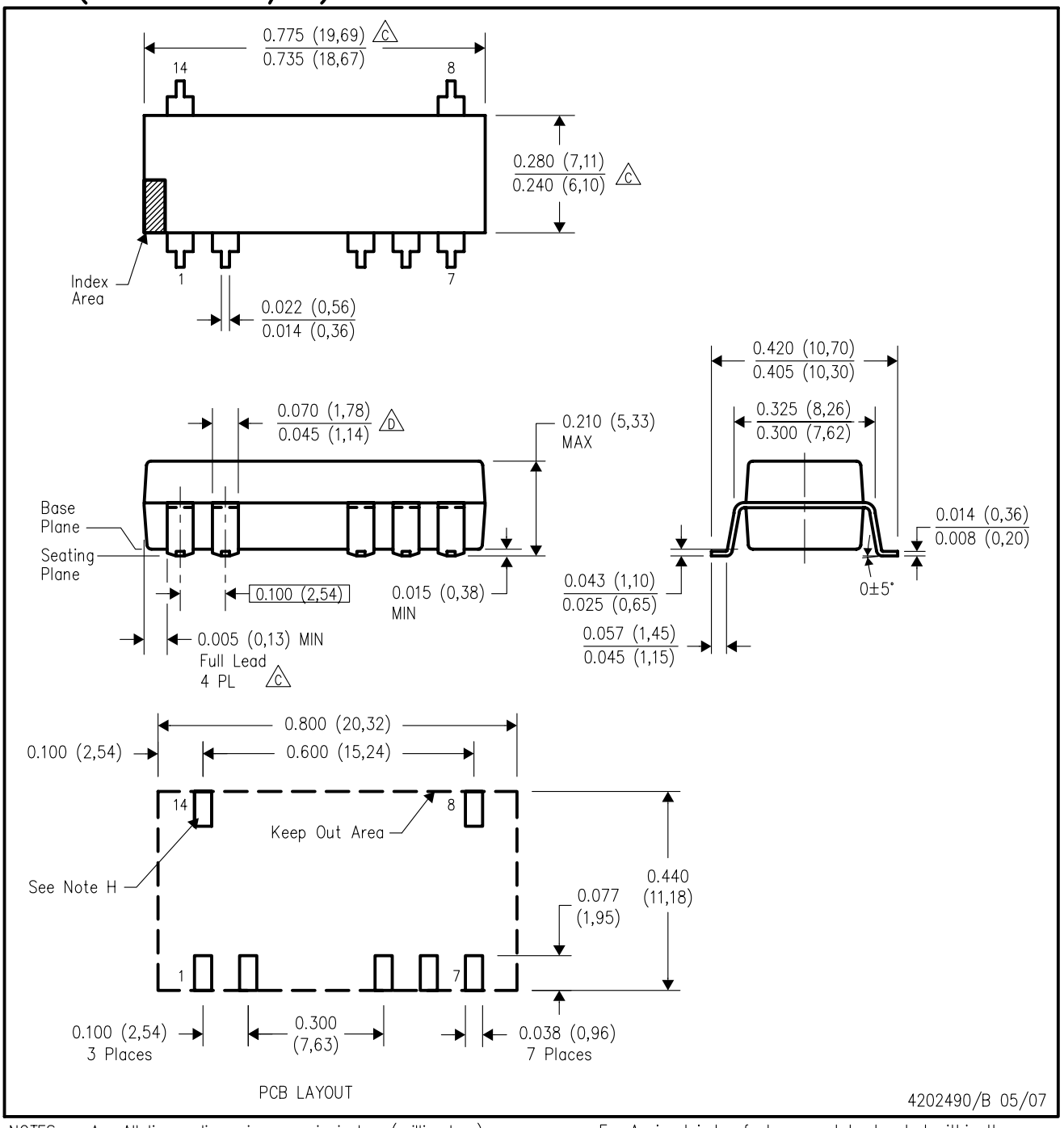


PCB LAYOUT

4202489/B 05/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS–3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross–hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS–001–AA.

DUA (R–PDSO–G7/14) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed exceed 0.010 (0,25).
- E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- F. A visual index feature must be located within the cross–hatched area.
- G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- H. Power pin connections should be two or more vias per input, ground and output pin.

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