

Features

- I_{off} supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16374T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162374T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

Functional Description

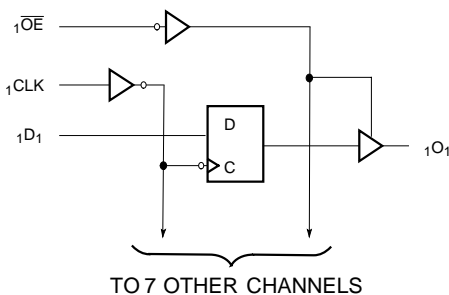
CY74FCT16374T and CY74FCT162374T are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent 8-bit registers or as a single 16-bit register by connecting the output Enable (OE) and Clock (CLK) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

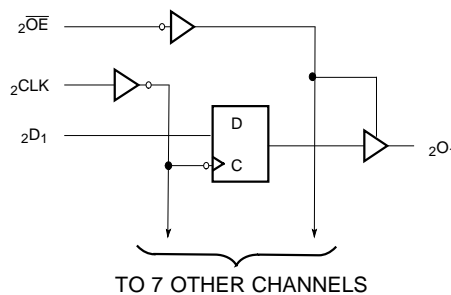
The CY74FCT16374T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162374T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162374T is ideal for driving transmission lines.

Logic Block Diagrams

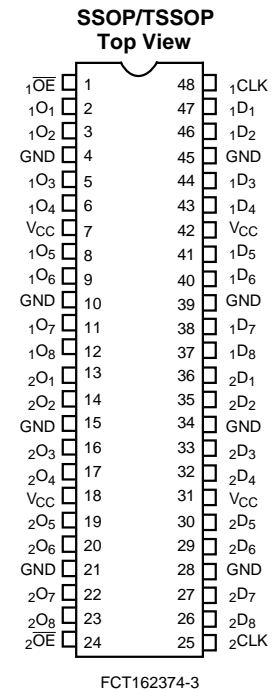


FCT162374-1



FCT162374-2

Pin Configuration



Function Table^[1]

Inputs			Outputs	Function
D	CLK	OE	O	
X	L	H	Z	High-Z
X	H	H	Z	
L	┐	L	L	Load Register
H	┐	L	H	
L	┐	H	Z	
H	┐	H	Z	

Pin Description

Name	Description
D	Data Inputs
CLK	Clock Inputs
OE	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-55°C to +125°C
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	-60 to +120 mA
Power Dissipation	1.0W
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[7]			±1	µA

Output Drive Characteristics for CY74FCT16374T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		V
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ┐ = LOW-to-HIGH Transition.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}= 5.0V, T_A= +25° C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Tested at +25° C.

Output Drive Characteristics for CY74FCT162374T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max. V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	5	500	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max. V _{IN} =3.4V ^[8]	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND V _{IN} =V _{CC} or V _{IN} =GND	60	100	μA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, f ₁ =5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND V _{IN} =V _{CC} or V _{IN} =GND	0.6	1.5	mA
		V _{IN} =3.4V or V _{IN} =GND	1.1	3.0	mA
		V _{CC} =Max., f ₀ =10 MHz, f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, OE=GND V _{IN} =V _{CC} or V _{IN} =GND	3.0	5.5 ^[11]	mA
		V _{IN} =3.4V or V _{IN} =GND	7.5	19.0 ^[11]	mA

Note:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f₀ = Clock frequency for registered devices, otherwise zero
 f₁ = Input signal frequency
 N₁ = Number of inputs changing at f₁
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[12]

Parameter	Description	CY74FCT16374T CY74FCT162374T		CY74FCT16374AT CY74FCT162374AT		Unit	Fig. No. ^[13]
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to O	2.0	10.0	2.0	6.5	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	12.5	1.5	6.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	8.0	1.5	5.5	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, D to CLK	1.5		1.5		ns	4
t _W	CLK Pulse Width HIGH or LOW	5.0		5.0		ns	5
t _{SK(O)}	Output Skew ^[14]		0.5		0.5	ns	

Parameter	Description	CY74FCT16374CT CY74FCT162374CT		Unit	Fig. No. ^[13]
		Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CLK to O	2.0	5.2	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time	1.5	5.5	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.0	ns	1, 7, 8
t _{SU}	Set-Up Time HIGH or LOW, D to CLK	2.0		ns	4
t _H	Hold Time HIGH or LOW, D to CLK	1.5		ns	4
t _W	CLK Pulse Width HIGH or LOW	3.3		ns	5
t _{SK(O)}	Output Skew ^[14]		0.5	ns	

Notes:

12. Minimum limits are specified but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16374T

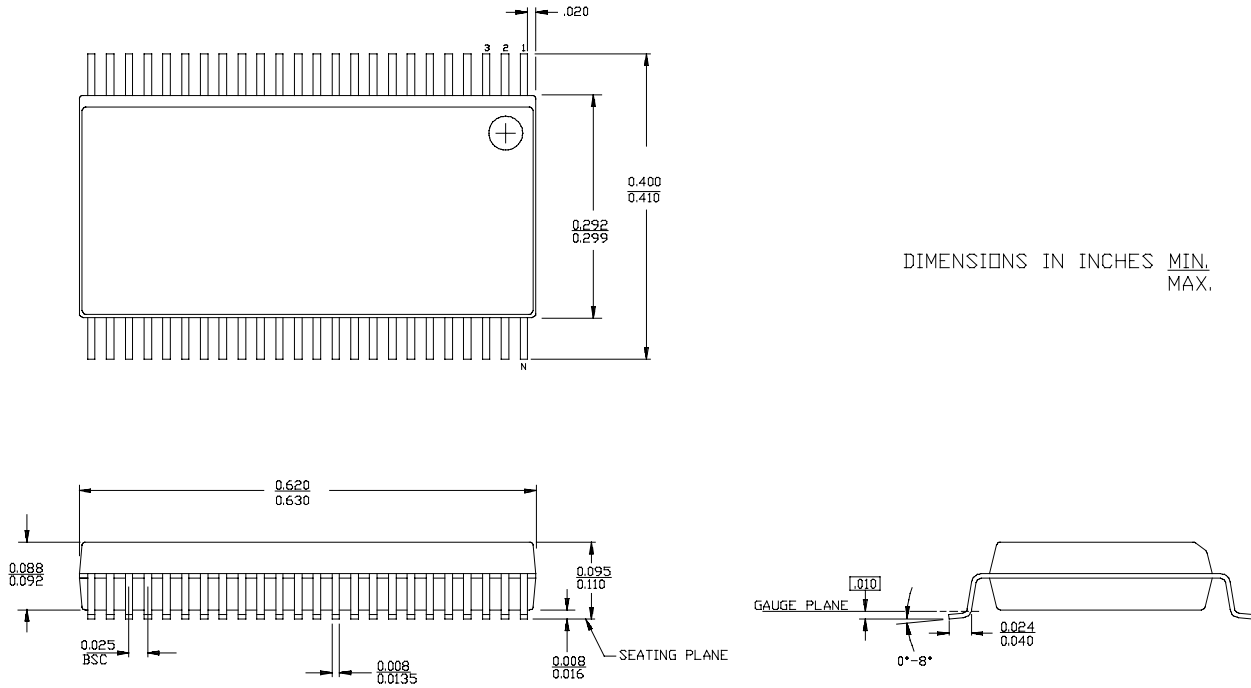
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT16374CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16374CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT16374ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16374ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT16374TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162374T

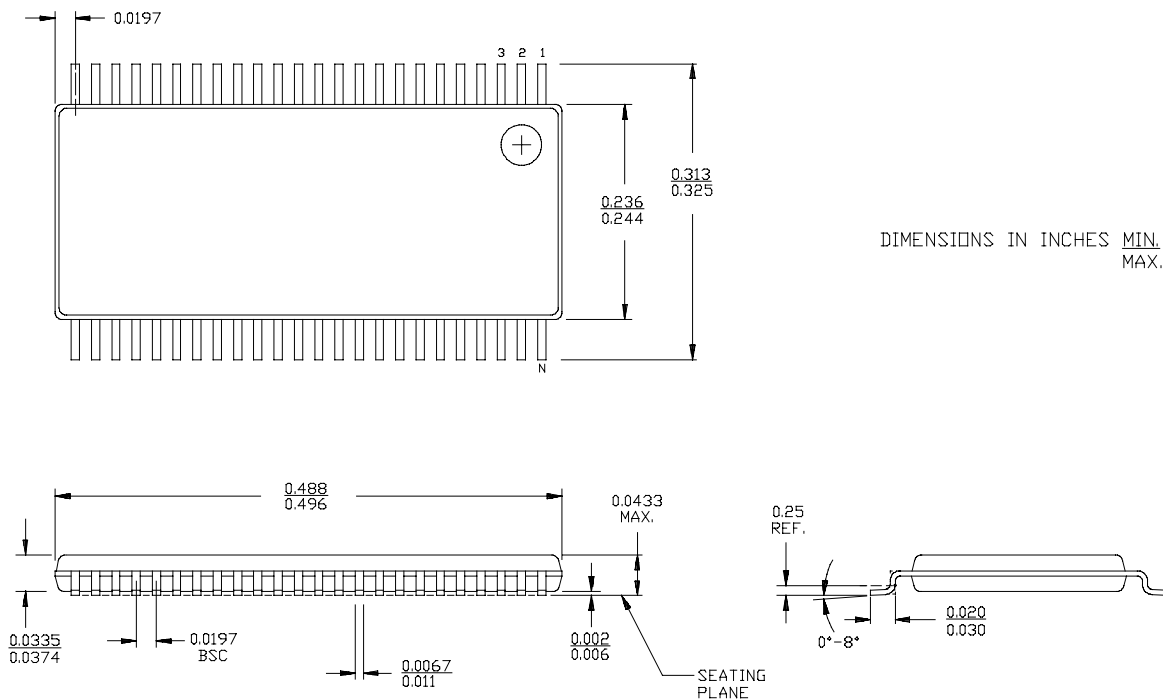
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	74FCT162374CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162374CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162374CTPVCT	O48	48-Lead (300-Mil) SSOP	
6.5	74FCT162374ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162374ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162374ATPVCT	O48	48-Lead (300-Mil) SSOP	
10.0	CY74FCT162374TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

Package Diagrams

48-Lead Shrunken Small Outline Package O48



48-Lead Thin Shrunken Small Outline Package Z48



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74FCT162374ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374ATPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374CTPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374CTPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162374ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
74FCT162374ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
74FCT162374TPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374ATPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374ATPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374CTPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374CTPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374CTPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374CTPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16374TPVCG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162374ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162374CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162374ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT162374ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT162374TPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374ATPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374ATPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374ATPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374CTPACT	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
CY74FCT16374CTPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374CTPVCT	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16374ETPAC	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT16374ETPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
CY74FCT16374ETPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT16374ETPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CY74FCT16374TPVC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374ATPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374ATPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374ATPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374CTPACTE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374CTPACTG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162374CTPVCTG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

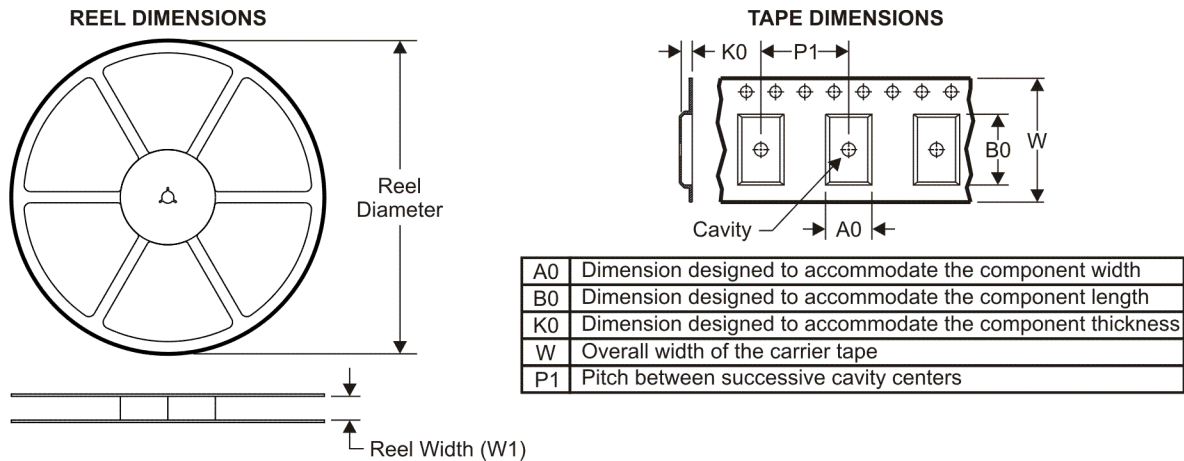
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI

to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162374ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
74FCT162374ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
74FCT162374CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
74FCT162374CTPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT162374TPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16374ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CY74FCT16374ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16374CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
CY74FCT16374CTPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

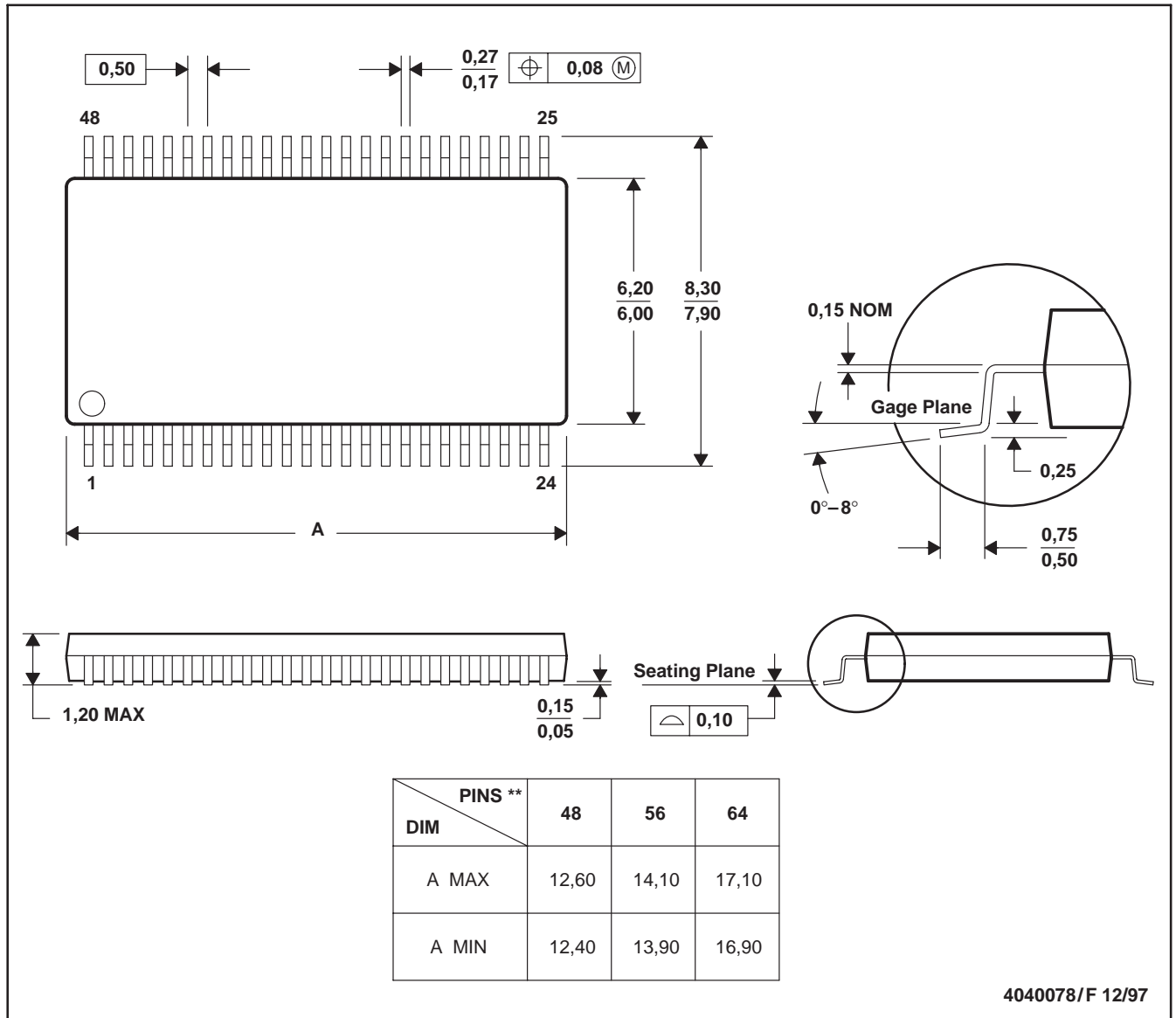

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162374ATPACT	TSSOP	DGG	48	2000	346.0	346.0	41.0
74FCT162374ATPVCT	SSOP	DL	48	1000	346.0	346.0	49.0
74FCT162374CTPACT	TSSOP	DGG	48	2000	346.0	346.0	41.0
74FCT162374CTPVCT	SSOP	DL	48	1000	346.0	346.0	49.0
CY74FCT162374TPVCT	SSOP	DL	48	1000	346.0	346.0	49.0
CY74FCT16374ATPACT	TSSOP	DGG	48	2000	346.0	346.0	41.0
CY74FCT16374ATPVCT	SSOP	DL	48	1000	346.0	346.0	49.0
CY74FCT16374CTPACT	TSSOP	DGG	48	2000	346.0	346.0	41.0
CY74FCT16374CTPVCT	SSOP	DL	48	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

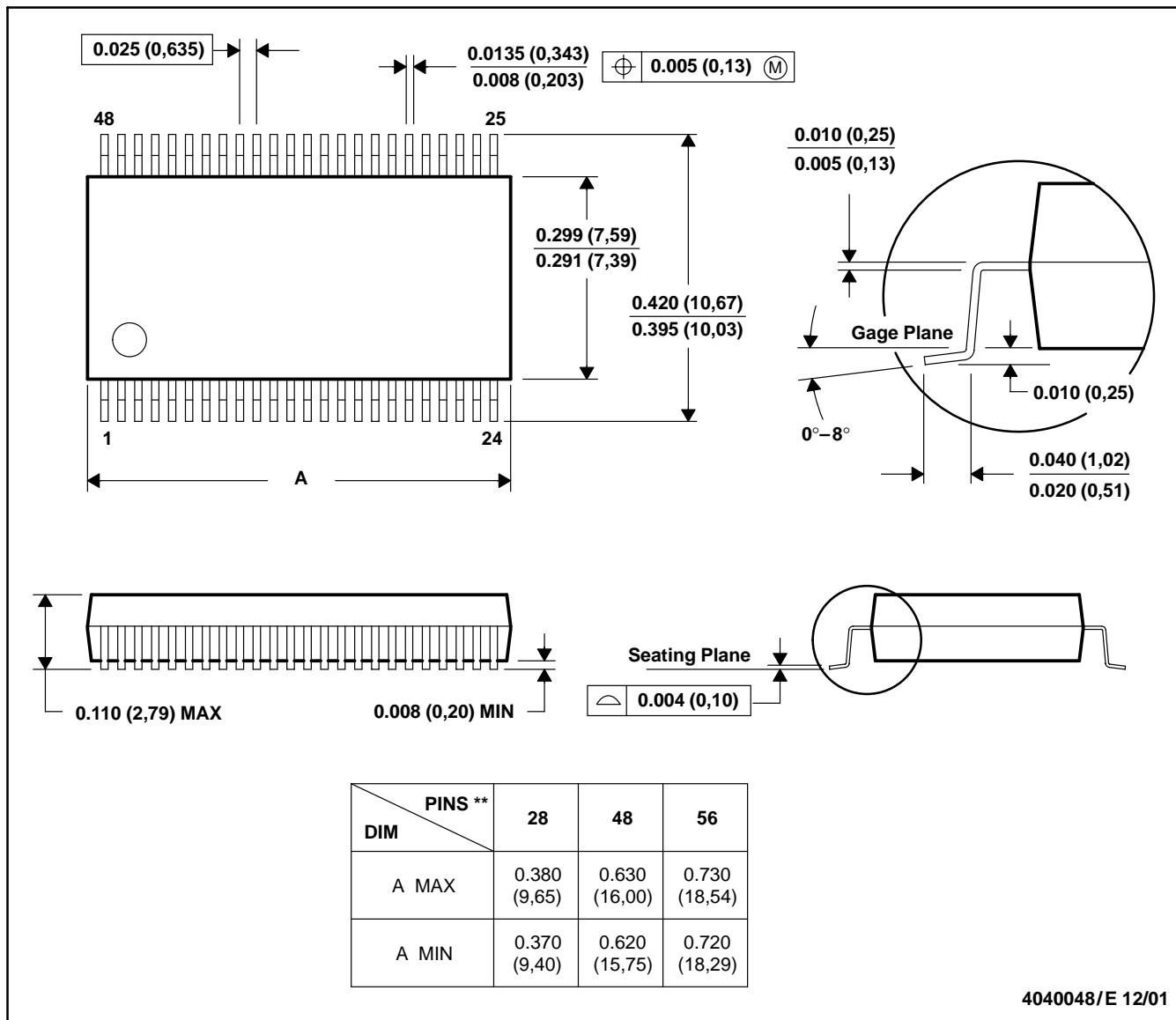


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162374ATPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT162374A	
74FCT162374CTPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT162374C	
74FCT162374CTPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	FCT162374C	
CY74FCT162374ATPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	FCT162374A	
CY74FCT162374TPVCT	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	FCT162374	
CY74FCT16374ATPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT16374A	
CY74FCT16374CTPACT	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI	-40 to 85	FCT16374C	
CY74FCT16374TPVC	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI	-40 to 85	FCT16374	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

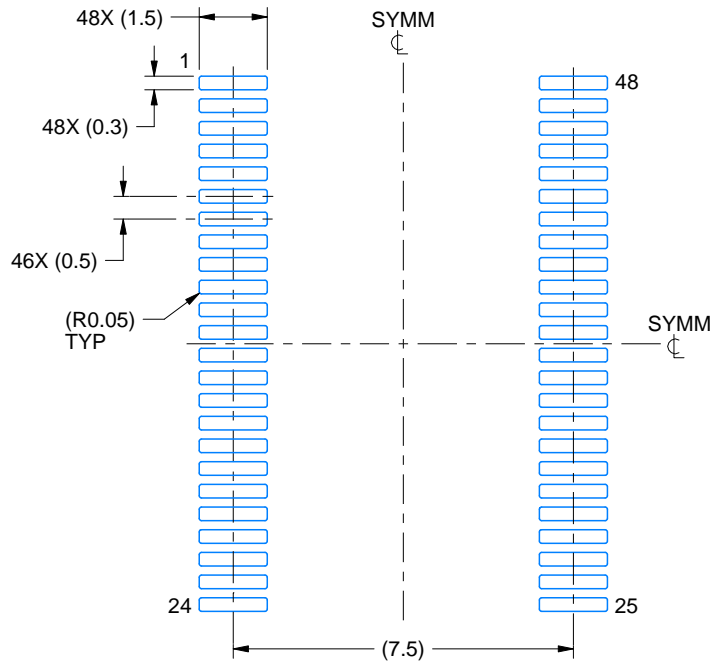
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

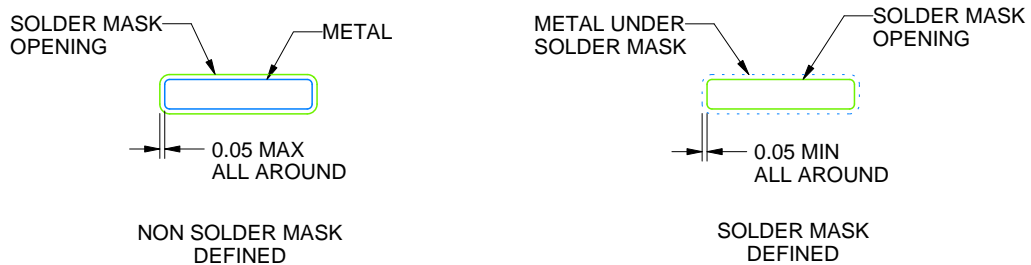
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

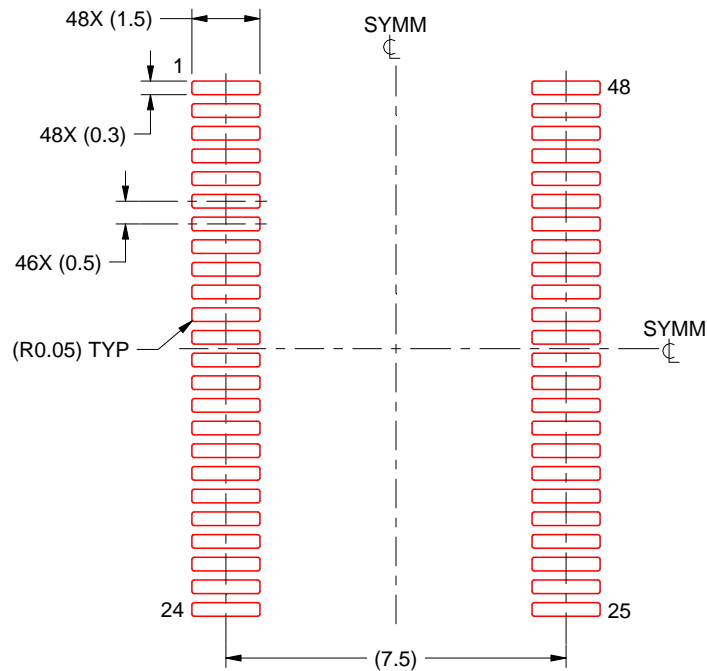
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

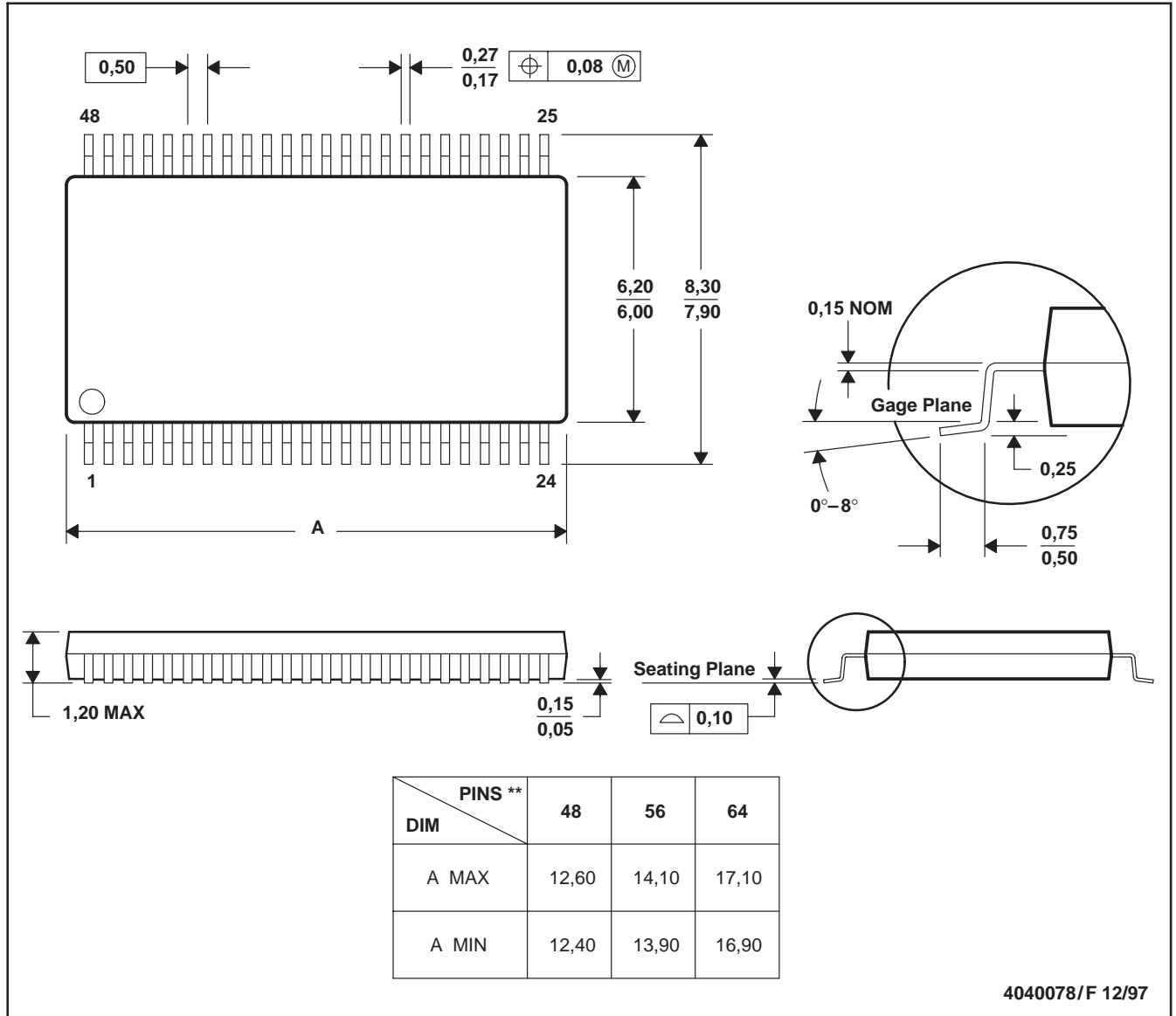
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated