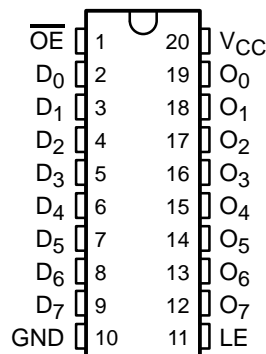


**CY54FCT573T, CY74FCT573T**  
**8-BIT LATCHES**  
**WITH 3-STATE OUTPUTS**  
 SCCS068 – OCTOBER 2001

- **Function and Pinout Compatible With FCT and F Logic**
- **Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **3-State Outputs**
- **CY54FCT573T**
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- **CY74FCT573T**
  - 64-mA Output Sink Current
  - 32-mA Output Source Current

CY54FCT573T . . . D PACKAGE  
 CY74FCT573T . . . P, Q, OR SO PACKAGE  
 (TOP VIEW)



**description**

The 'FCT573T devices consist of eight latches with 3-state outputs for bus-organized applications. When the latch-enable (LE) input is high, the flip-flops appear transparent to the data. Data that meets the required setup times are latched when LE transitions from high to low. Data appears on the bus when the output-enable ( $\overline{OE}$ ) input is low. When  $\overline{OE}$  is high, the bus output is in the high-impedance state. In this mode, data can be entered into the latches. The 'FCT573T devices are identical to the 'FCT373T devices, except for the flow-through pinout of the 'FCT573T, which simplifies board design.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**CY54FCT573T, CY74FCT573T**  
**8-BIT LATCHES**  
**WITH 3-STATE OUTPUTS**

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**ORDERING INFORMATION**

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.7	CY74FCT573CTQCT	FCT573C
	SOIC – SO	Tube	4.7	CY74FCT573CTSOC	FCT573C
		Tape and reel	4.7	CY74FCT573CTSUCT	
	DIP – P	Tube	5.2	CY74FCT573ATPC	CY74FCT573ATPC
	QSOP – Q	Tape and reel	5.2	CY74FCT573ATQCT	FCT573A
	SOIC – SO	Tube	5.2	CY74FCT573ATSOC	FCT573A
		Tape and reel	5.2	CY74FCT573ATSUCT	
	QSOP – Q	Tape and reel	8	CY74FCT573TQCT	FCT573
SOIC – SO	Tube	8	CY74FCT573TSOC	FCT573	
	Tape and reel	8	CY74FCT573TSUCT		
-55°C to 125°C	CDIP – D	Tube	8.5	CY54FCT573ATLMB	

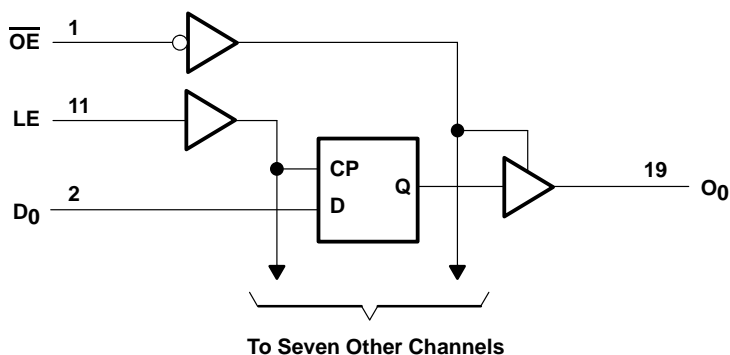
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS			OUTPUT
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

H = High logic level, L = Low logic level,  
 X = Don't care, Z = High-impedance state,  
 Q<sub>n</sub> = Previous state of flip flops (Q<sub>n-1</sub>)

**logic diagram (positive logic)**





# CY54FCT573T, CY74FCT573T

## 8-BIT LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT573T			CY74FCT573T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	-0.7	-1.2					V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2			
		I <sub>OH</sub> = -15 mA			2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>			5				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>					5		
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V					±1		
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V			±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V					±1		
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V			10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V					10		
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V			-10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V					-10		
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V			±1			±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1	0.2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open	0.5	2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open				0.5	2		
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.5 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.06	0.12					mA/MHz
	V <sub>CC</sub> = 5.25 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.06	0.12		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

¶ This parameter is derived for use in total power-supply calculations.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY54FCT573T		CY74FCT573T		UNIT
				MIN	TYP†	MAX	MIN	
I <sub>C</sub> #	V <sub>CC</sub> = 5.5 V, Outputs open, OE = GND, LE = V <sub>CC</sub>	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.7	1.4			mA
			V <sub>IN</sub> = 3.4 V or GND	1	2.4			
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	1.3	2.6			
			V <sub>IN</sub> = 3.4 V or GND	3.3	10.6			
	V <sub>CC</sub> = 5.25 V, Outputs open, OE = GND, LE = V <sub>CC</sub>	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.7	1.4	
			V <sub>IN</sub> = 3.4 V or GND			1	2.4	
		Eight bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			1.3	2.6	
			V <sub>IN</sub> = 3.4 V or GND			3.3	10.6	
C <sub>i</sub>				6	10	6	10	pF
C <sub>o</sub>				8	12	8	12	pF

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

# I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

I<sub>C</sub> = Total supply current

I<sub>CC</sub> = Power-supply current with CMOS input levels

ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

D<sub>H</sub> = Duty cycle for TTL inputs high

N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY54FCT573T		CY54FCT573AT		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	6		6		ns
t <sub>su</sub>	Setup time, data before LE↑	2		2		ns
t <sub>h</sub>	Hold time, data after LE↑	1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		CY74FCT573T		CY74FCT573AT		CY74FCT573CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	6		5		5		ns
t <sub>su</sub>	Setup time, data before LE↑	2		2		2		ns
t <sub>h</sub>	Hold time, data after LE↑	1.5		1.5		1.5		ns

**CY54FCT573T, CY74FCT573T**  
**8-BIT LATCHES**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over operating free-air temperature range (see Figure 1)**

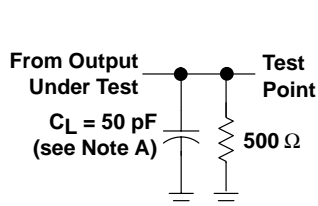
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT573AT		UNIT
			MIN	MAX	
t <sub>PLH</sub>	D	O	1.5	5.6	ns
t <sub>PHL</sub>			1.5	5.6	
t <sub>PLH</sub>	LE	O	2	9.8	ns
t <sub>PHL</sub>			2	9.8	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	7.5	ns
t <sub>PZL</sub>			1.5	7.5	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	6.5	ns
t <sub>PLZ</sub>			1.5	6.5	

**switching characteristics over operating free-air temperature range (see Figure 1)**

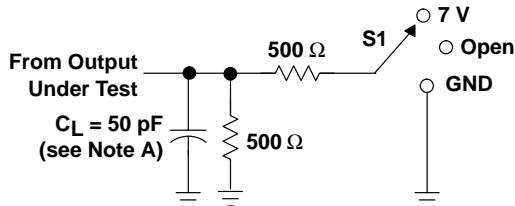
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT573T		CY74FCT573AT		CY74FCT573CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	O	1.5	8	1.5	5.2	1.5	4.7	ns
t <sub>PHL</sub>			1.5	8	1.5	5.2	1.5	4.7	
t <sub>PLH</sub>	LE	O	2	13	2	8.5	2	5.5	ns
t <sub>PHL</sub>			2	13	2	8.5	2	5.5	
t <sub>PZH</sub>	$\overline{OE}$	O	1.5	12	1.5	6.5	1.5	5.5	ns
t <sub>PZL</sub>			1.5	12	1.5	6.5	1.5	5.5	
t <sub>PHZ</sub>	$\overline{OE}$	O	1.5	7.5	1.5	5.5	1.5	5	ns
t <sub>PLZ</sub>			1.5	7.5	1.5	5.5	1.5	5	



PARAMETER MEASUREMENT INFORMATION

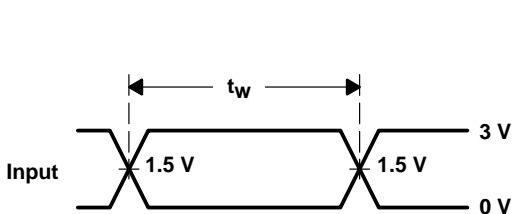


LOAD CIRCUIT FOR  
 TOTEM-POLE OUTPUTS

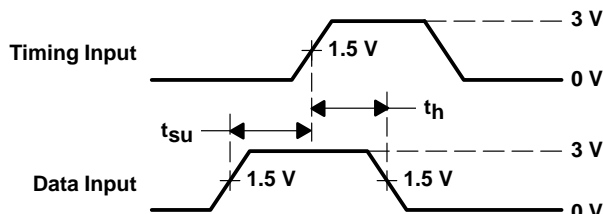


LOAD CIRCUIT FOR  
 3-STATE OUTPUTS

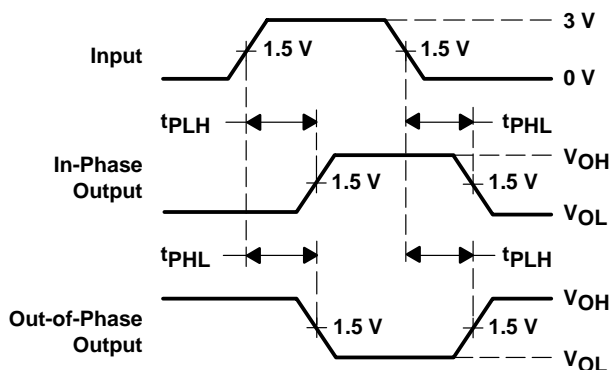
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



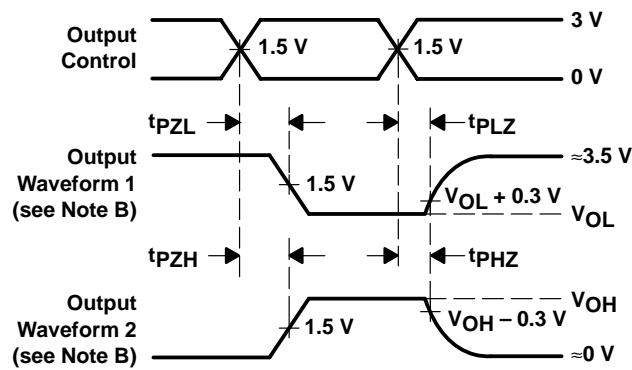
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9223801MRA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223801MRA A
5962-9223801MRA.Z	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223801MRA A
<a href="#">5962-9223802M2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223802M2A CY54FCT 573ATLMB
<a href="#">CY54FCT573ATLMB</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9223802M2A CY54FCT 573ATLMB
<a href="#">CY74FCT573ATPC</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT573ATPC
CY74FCT573ATPC.Z	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT573ATPC
<a href="#">CY74FCT573ATQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573A
CY74FCT573ATQCT.Z	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573A
<a href="#">CY74FCT573ATSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573A
CY74FCT573ATSOC.Z	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573A
<a href="#">CY74FCT573ATSOCT</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573A
CY74FCT573ATSOCT.Z	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573A
<a href="#">CY74FCT573CTQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573C
CY74FCT573CTQCT.Z	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573C
<a href="#">CY74FCT573CTSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573C
CY74FCT573CTSOC.Z	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573C
<a href="#">CY74FCT573TQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573
CY74FCT573TQCT.Z	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT573
<a href="#">CY74FCT573TSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573
CY74FCT573TSOC.Z	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT573

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).



- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT573ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT573ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT573CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT573TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT573ATQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT573ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT573CTQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT573TQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9223802M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT573ATLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT573ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT573ATPC.Z	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT573ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT573ATSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT573CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT573CTSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT573TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT573TSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6

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