

CY54FCT540T, CY74FCT540T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCCS029A – MAY 1994 – REVISED OCTOBER 2001

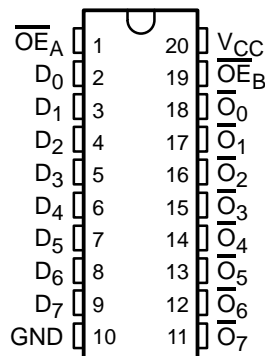
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT540T
 - 48-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT540T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current
- 3-State Outputs

description

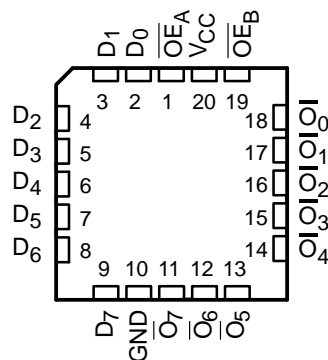
The 'FCT540T inverting buffers/line drivers can be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar-logic counterparts, while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

CY54FCT540T . . . D PACKAGE
CY74FCT540T . . . Q PACKAGE
(TOP VIEW)



CY54FCT540T . . . L PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT540CTQCT	FCT540C
	CDIP – D	Tube	4.7	CY54FCT540CTDMB	
–55°C to 125°C	LCC – L	Tube	4.7	CY54FCT540CTLMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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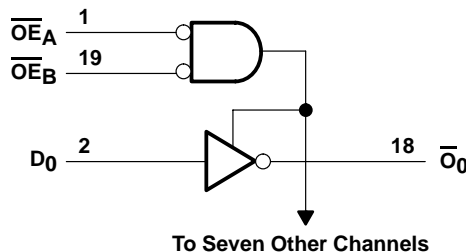
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FUNCTION TABLE

INPUTS			OUTPUT \bar{O}
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	H
L	L	H	L
H	H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	68°C/W
Ambient temperature range with power applied, T_A	-65°C to 135°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	CY54FCT540T			CY74FCT540T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			-12			-32	mA
I_{OL} Low-level output current			48			64	mA
T_A Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT540T			CY74FCT540T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _{IN} = -18 mA	-0.7	-1.2					V
	V _{CC} = 4.75 V, I _{IN} = -18 mA				-0.7	-1.2		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -12 mA	2.4	3.3					V
	V _{CC} = 4.75 V	I _{OH} = -32 mA			2			
		I _{OH} = -15 mA			2.4	3.3		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA	0.3	0.55					V
	V _{CC} = 4.75 V, I _{OL} = 64 mA				0.3	0.55		
V _{hys}	All inputs	0.2			0.2			V
I _I	V _{CC} = 5.5 V, V _{IN} = V _{CC}			5				μA
	V _{CC} = 5.25 V, V _{IN} = V _{CC}					5		
I _{IH}	V _{CC} = 5.5 V, V _{IN} = 2.7 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 2.7 V					±1		
I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V			±1				μA
	V _{CC} = 5.25 V, V _{IN} = 0.5 V					±1		
I _{OZH}	V _{CC} = 5.5 V, V _{OUT} = 2.7 V			10				μA
	V _{CC} = 5.25 V, V _{OUT} = 2.7 V					10		
I _{OZL}	V _{CC} = 5.5 V, V _{OUT} = 0.5 V			-10				μA
	V _{CC} = 5.25 V, V _{OUT} = 0.5 V					-10		
I _{OS} ‡	V _{CC} = 5.5 V, V _{OUT} = 0 V	-60	-120	-225				mA
	V _{CC} = 5.25 V, V _{OUT} = 0 V				-60	-120	-225	
I _{off}	V _{CC} = 0 V, V _{OUT} = 4.5 V			±1			±1	μA
I _{CC}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V	0.1	0.2					mA
	V _{CC} = 5.25 V, V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V				0.1	0.2		
ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open	0.5	2					mA
	V _{CC} = 5.25 V, V _{IN} = 3.4 V§, f ₁ = 0, Outputs open				0.5	2		
I _{CCD} ¶	V _{CC} = 5.5 V, 50% duty cycle, Outputs open, One bit switching at f ₁ = 10 MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ and $\overline{OE}_B = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V	0.06	0.12					mA/ MHz
	V _{CC} = 5.25 V, 50% duty cycle, Outputs open, One bit switching at f ₁ = 10 MHz, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ or $\overline{OE}_A = \text{GND}$ and $\overline{OE}_B = V_{CC}$, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V				0.06	0.12		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		CY54FCT540T		CY74FCT540T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I _C #	V _{CC} = 5.5 V, Outputs open, $\overline{OE}_A = \overline{OE}_B =$ GND or $\overline{OE}_A =$ GND and $\overline{OE}_B = V_{CC}$	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4		mA	
			V _{IN} = 3.4 V or GND	1	2.4			
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1.3	2.6			
			V _{IN} = 3.4 V or GND	3.3	10.6			
	V _{CC} = 5.25 V, Outputs open, $\overline{OE}_A = \overline{OE}_B =$ GND or $\overline{OE}_A =$ GND and $\overline{OE}_B = V_{CC}$	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7		1.4
			V _{IN} = 3.4 V or GND			1		2.4
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			1.3		2.6
			V _{IN} = 3.4 V or GND			3.3		10.6
C _i					5	10	pF	
C _o					9	12	pF	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

I_C = I_{CC} + ΔI_{CC} × D_H × N_T + I_{CCD} (f₀/2 + f₁ × N₁)

Where:

- I_C = Total supply current
- I_{CC} = Power-supply current with CMOS input levels
- ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
- D_H = Duty cycle for TTL inputs high
- N_T = Number of TTL inputs at D_H
- I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
- f₀ = Clock frequency for registered devices, otherwise zero
- f₁ = Input signal frequency
- N₁ = Number of inputs changing at f₁

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



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switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT540CT		UNIT
			MIN	MAX	
t _{PLH}	D	\bar{O}	1.5	4.7	ns
t _{PHL}			1.5	4.7	
t _{PZH}	\bar{OE}	\bar{O}	1.5	6.5	ns
t _{PZL}			1.5	6.5	
t _{PHZ}	\bar{OE}	\bar{O}	1.5	5.7	ns
t _{PLZ}			1.5	5.7	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT540CT		UNIT
			MIN	MAX	
t _{PLH}	D	\bar{O}	1.5	4.1	ns
t _{PHL}			1.5	4.1	
t _{PZH}	\bar{OE}	\bar{O}	1.5	5.8	ns
t _{PZL}			1.5	5.8	
t _{PHZ}	\bar{OE}	\bar{O}	1.5	5.2	ns
t _{PLZ}			1.5	5.2	



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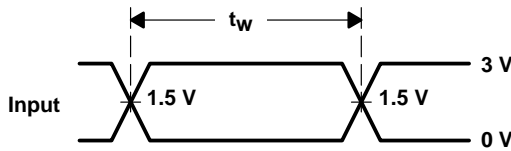
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9222006MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9222006MRA
5962-9223701M2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701M2A CY54FCT 541TLMB
5962-9223701MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701MRA CY54FCT541TDMB
5962-9223705MRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223705MRA
CY54FCT541TDMB	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701MRA CY54FCT541TDMB
CY54FCT541TLMB	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701M2A CY54FCT 541TLMB
CY74FCT540CTQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT540C
CY74FCT541ATPC	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT541ATPC
CY74FCT541ATQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541A
CY74FCT541ATSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541ATSOCT	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541CTQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541C
CY74FCT541CTSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C
CY74FCT541CTSOCT	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C
CY74FCT541TQCT	Active	Production	SSOP (DBQ) 20	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541
CY74FCT541TSOC	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT540CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT541CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT541TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT540CTQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT541ATQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT541ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT541CTQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT541CTSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT541TQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9223701M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT541TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT541TLMB.Z	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT541ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT541ATPC.Z	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT541ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541ATSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541CTSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541TSOC.Z	DW	SOIC	20	25	507	12.83	5080	6.6

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