CSD87313DMS 30V 双路 N 通道 NexFET™功率 MOSFET

1 特性

- 低源极至源极导通电阻
- 双共漏极 N 通道 MOSFET
- 针对 5V 栅极驱动进行了优化
- 低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

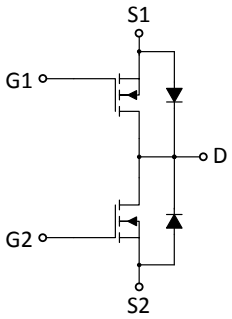
2 应用范围

- USB Type-C™和电力输送 (PD) VBus 保护
- 电池保护
- 负载开关

3 说明

CSD87313DMS 是一款 30V 共漏极、双路 N 通道器件，专为 USB Type-C/PD 和电池保护而设计。此 3.3mm × 3.3mm SON 器件具有低源极至源极导通电阻，可最大限度地较少损耗，且具有较少的组件数量，适用于空间受限的 应用。

原理图



产品概要

T_A = 25°C		数值		单位
V_{S1S2}	源极 1 到源极 2 电压	30		V
Q_g	栅极电荷总量 (4.5V)	28		nC
Q_{gd}	栅极电荷（栅极到漏极）	6.0		nC
$R_{S1S2(on)}$	源极 1 到源极 2 最大导通电阻	V_{GS} = 2.5V	9.6	mΩ
		V_{GS} = 4.5V	5.5	
$V_{GS(th)}$	阈值电压	0.9		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD87313DMS	2500	13 英寸卷带	SON 3.30mm × 3.30mm 塑料封装	卷带封装
CSD87313DMST	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C 时测得，除非另外注明		值	单位
V_{S1S2}	源极 1 到源极 2 电压	30	V
V_{GS}	栅源电压(1)	±10	V
I_{S1S2}	持续源极电流(2)	17	A
I_{SM}	脉冲源极电流，T_A = 25°C 时测得(2)(3)	120	A
P_D	功率耗散(2)	2.7	W
	功率耗散(4)	1	
T_J，T_{stg}	工作结温，储存温度	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲，I_D = 100A，L = 0.1mH，R_G = 25Ω	67	mJ

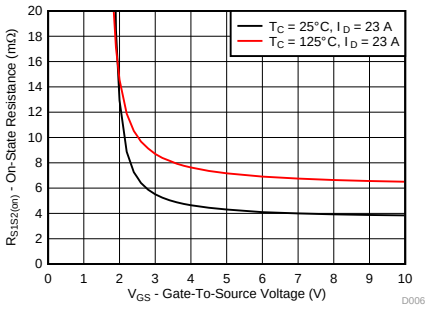
(1) V_{G1S1} 不应超过 ±10V，V_{G2S2} 不应超过 ±10V。

(2) 典型 $R_{\theta JA}$ = 45°C/W（当在 0.06 英寸 [1.52mm] 厚的 FR4 PCB 上将其安装在 1 平方英寸 [6.45cm^2] 2oz [0.071mm] 厚的铜焊盘上时）。

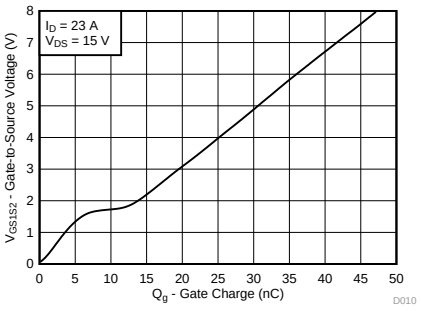
(3) 占空比 ≤ 2%，脉冲持续时间 ≤ 300µs。

(4) 典型 $R_{\theta JA}$ = 125°C/W（在 2oz 铜焊盘上）。

$R_{S1S2(ON)}$ 与 V_{GS} 对比



栅极电荷



目录

4 修订历史记录

日期	修订版本	注释
2017 年 4 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
I_{S1S2}	Source1-to-Source2 leakage current	V_{G1S1} = 0 V, V_{G2S2} = 0 V, V_{S1S2} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_{S1S2} = 250 µA	0.6	0.9	1.2	V
$R_{S1S2(on)}$	Source1-to-Source2 on resistance	V_{GS} = 2.5 V, I_{S1S2} = 20 A		6.7	9.6	mΩ
		V_{GS} = 4.5 V, I_{S1S2} = 23 A		4.6	5.5	
g_{fs}	Transconductance	V_{S1S2} = 3 V, I_{S1S2} = 23 A		149		S
DYNAMIC CHARACTERISTICS(1)						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 15 V, f = 1 MHz		3300	4290	pF
C_{OSS}	Output capacitance			281	365	pF
C_{RSS}	Reverse transfer capacitance			154	200	pF
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 15 V, I_{S1S2} = 23 A V_{G1S1} = 4.5 V, V_{G2S2} = 0 V		28		nC
Q_{gd}	Gate charge gate-to-drain			6.0		nC
Q_{gs}	Gate charge gate-to-source			6.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			3.2		nC
$t_{d(on)}$	Turnon delay time	V_{S1S2} = 15 V, I_{S1S2} = 23 A V_{GS} = 4.5 V, R_{GEN} = 0 Ω		9		ns
t_r	Rise time			27		ns
$t_{d(off)}$	Turnoff delay time			41		ns
t_f	Fall time			13		ns
DIODE CHARACTERISTICS						
I_{fss}	Maximum continuous Source1-to-Source2 diode forward current(2)	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V			2	A
V_{fss}	Source1-to-Source2 diode forward voltage	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V, I_{fss} = 23 A		0.8	1.0	V

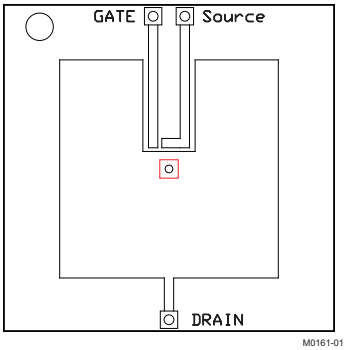
(1) Dynamic characteristic measurements are for a single FET.
(2) Typical $R_{\theta JA}$ = 125°C/W on a minimum 2-oz Cu pad.

5.2 Thermal Information

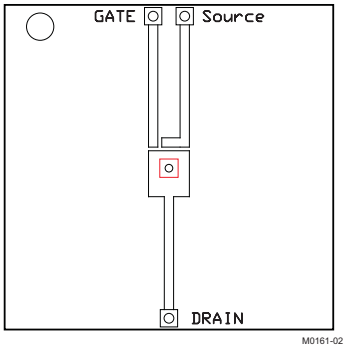
T_A = 25°C (unless otherwise stated)

THERMAL METRIC			UNIT
$R_{\theta JA}$	Junction-to-case thermal resistance(1)	125	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)	45	°C/W

(1) Device mounted on minimum 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



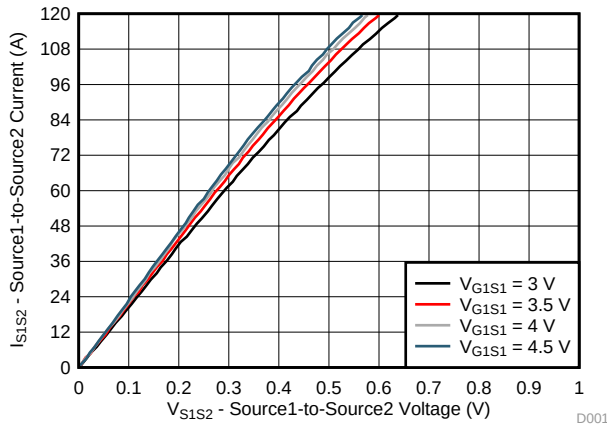
$R_{\theta JA}$ = 45°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



$R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

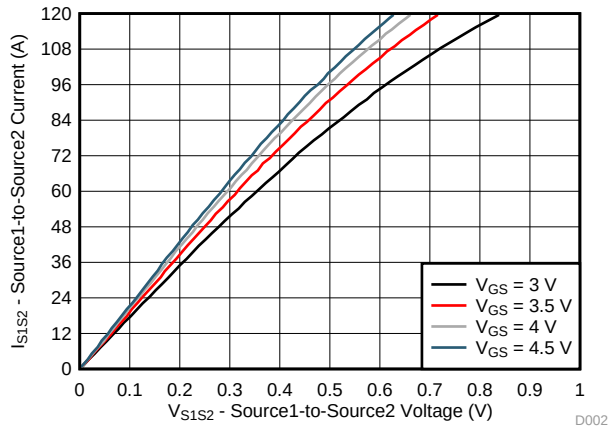
5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)



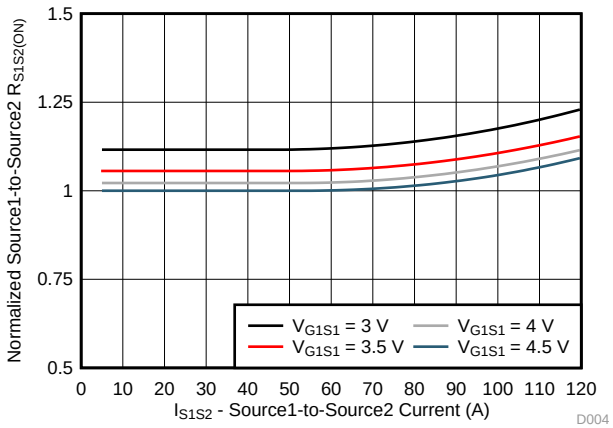
Pulse width = 250 µs, duty cycle = 0.5% V_{G2S2} = 4.5 V

Figure 1. Saturation Characteristics



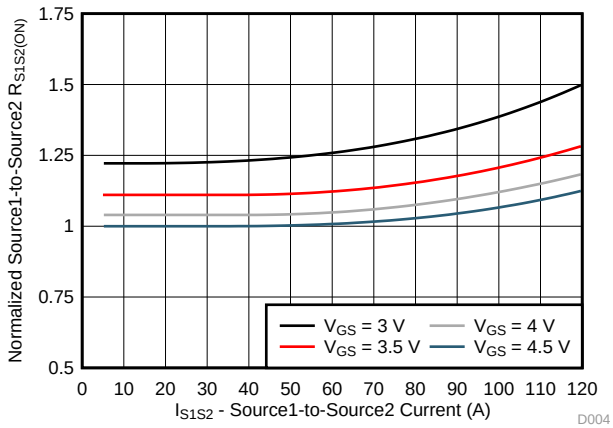
Pulse width = 250 µs, duty cycle = 0.5%

Figure 2. Saturation Characteristics



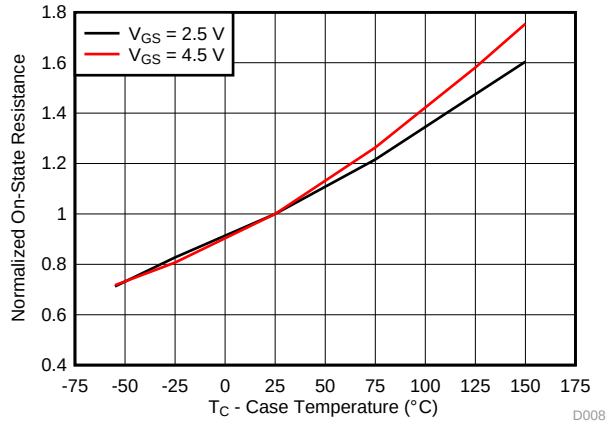
Pulse width = 250 µs, duty cycle = 0.5% V_{G2S2} = 4.5 V

Figure 3. Saturation Characteristics



Pulse width = 250 µs, duty cycle = 0.5%

Figure 4. Saturation Characteristics



I_{S1S2} = 23 A V_{GS} = 15 V

Figure 5. Normalized On-State Resistance vs Temperature

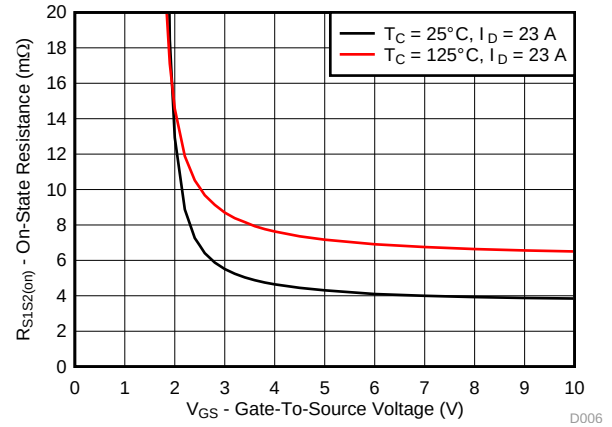
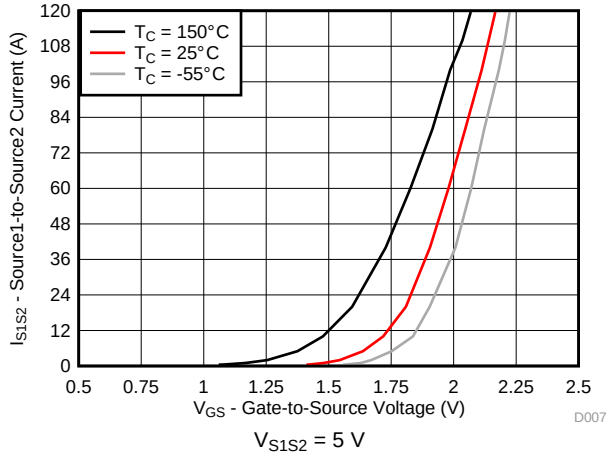


Figure 6. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



V_{S1S2} = 5 V

Figure 7. Transfer Characteristics

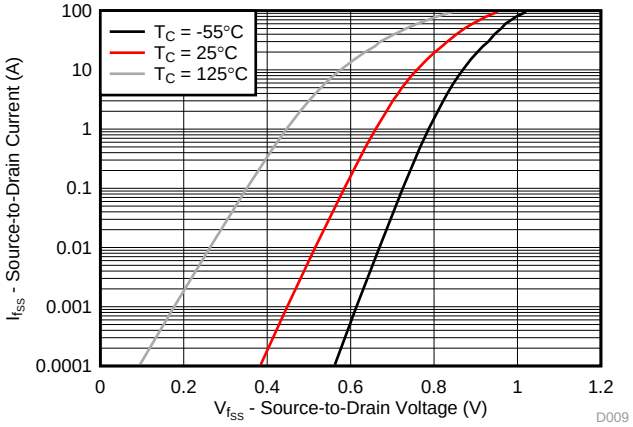
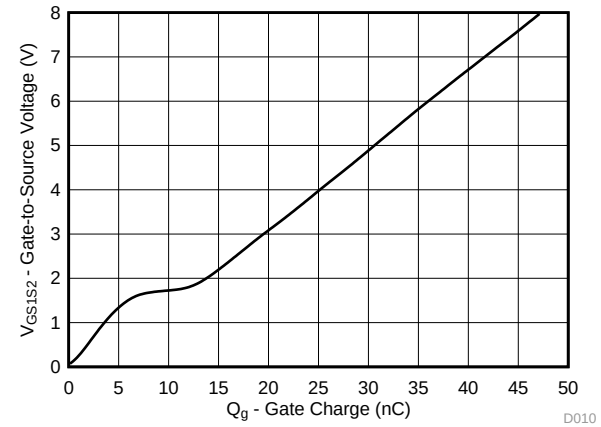


Figure 8. Typical Diode Forward Voltage



I_D = 23 A V_{S1S2} = 15 V

Figure 9. Gate Charge

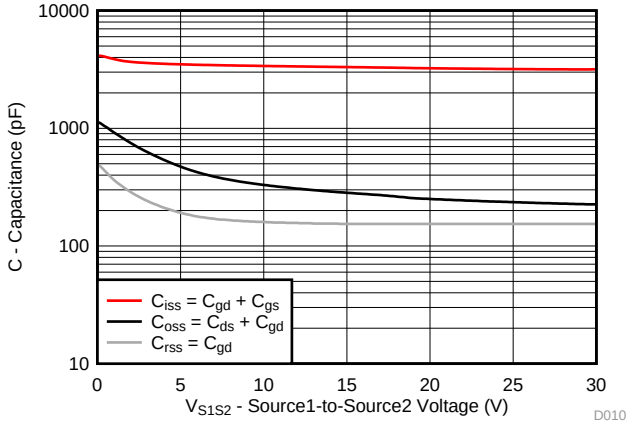
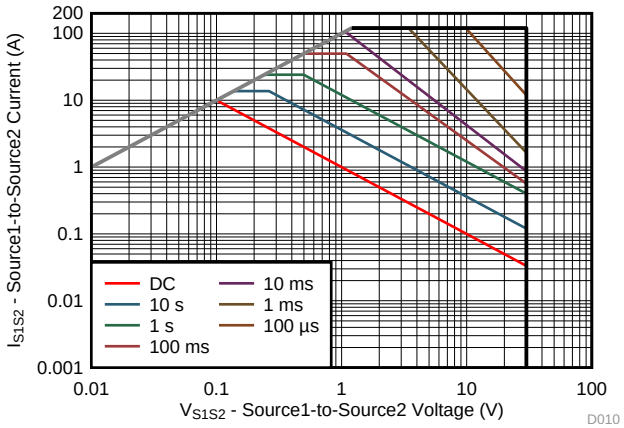
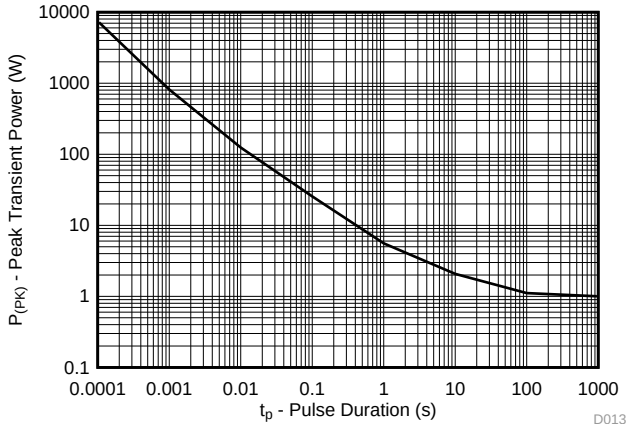


Figure 10. Capacitance



Single pulse, $R_{\theta JA}$ = 125°C/W

Figure 11. Maximum Safe Operating Area



$R_{\theta JA}$ = 125 °C/W, T_A = 25°C

Figure 12. Single Pulse Maximum Power Dissipation

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

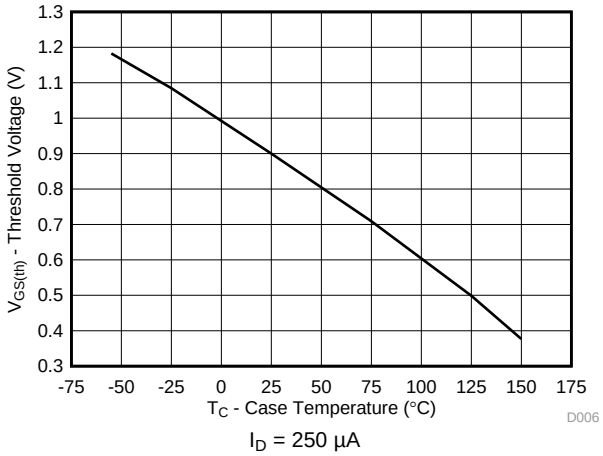


Figure 13. Threshold Voltage vs Temperature

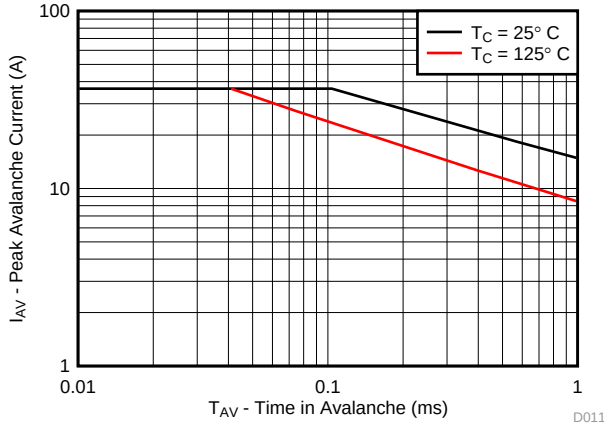


Figure 14. Single Pulse Unclamped Inductive Switching

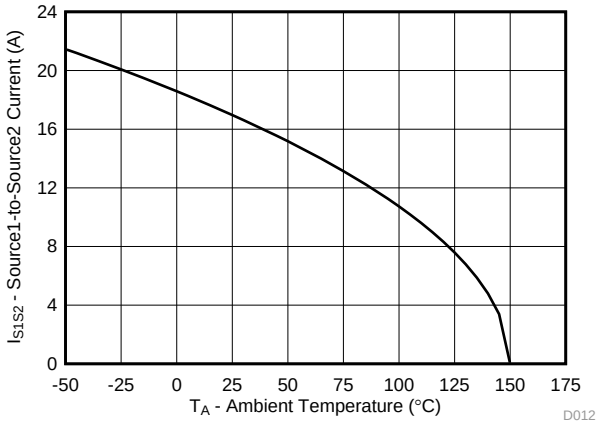


Figure 15. Maximum Source1-to-Source2 Current vs Temperature

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

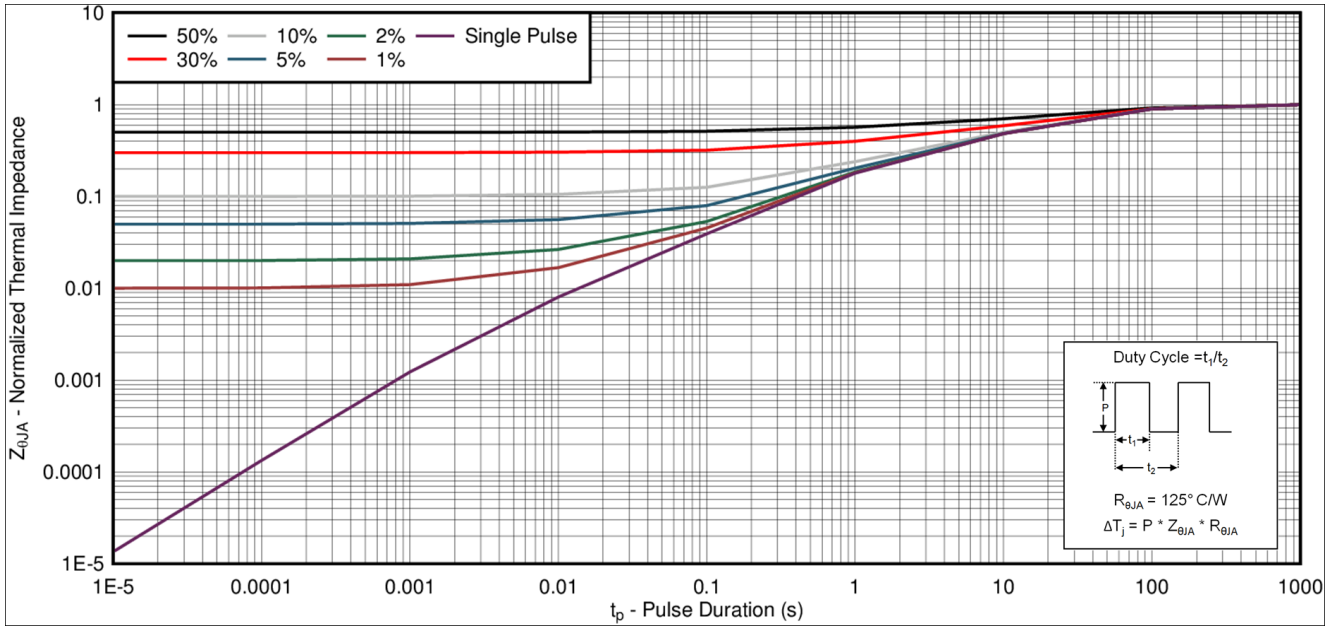


Figure 16. Transient Thermal Impedance

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

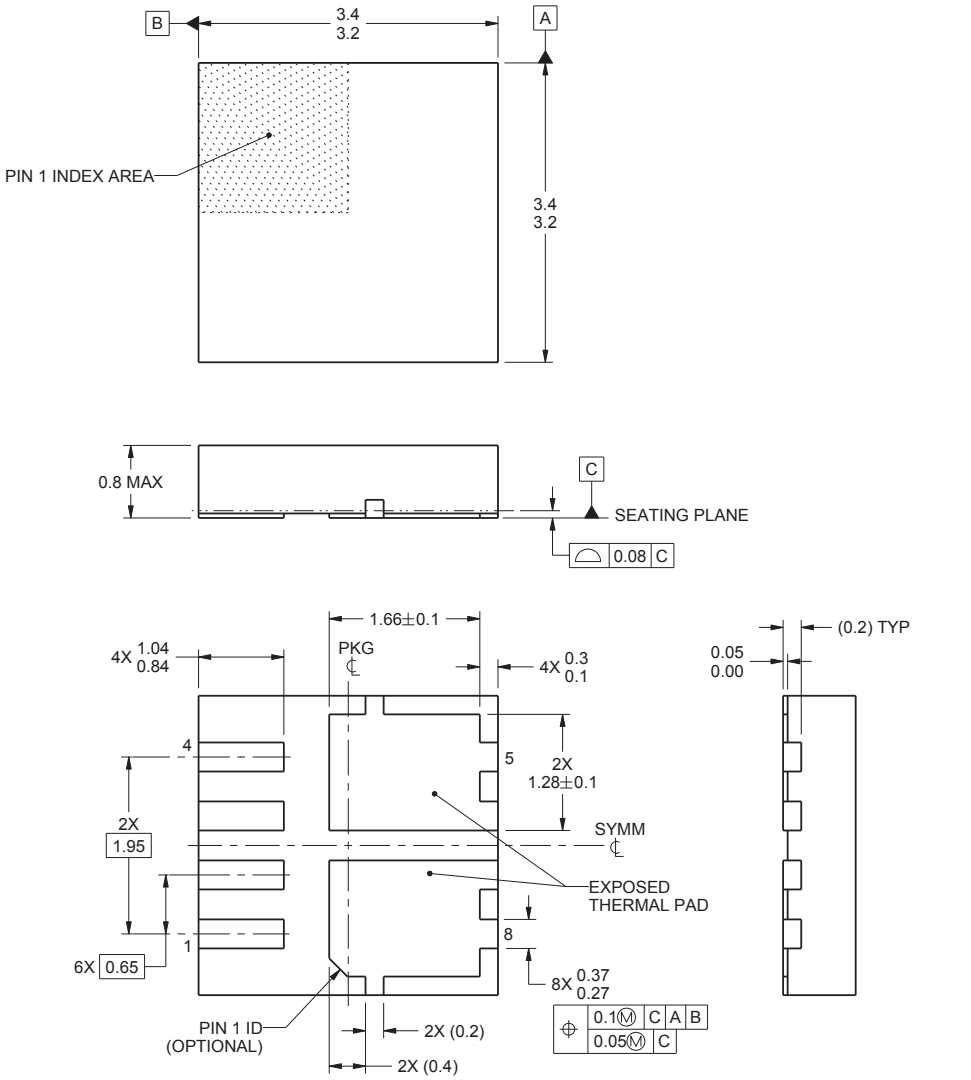
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

7.1 DMS 封装尺寸



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(1) 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。

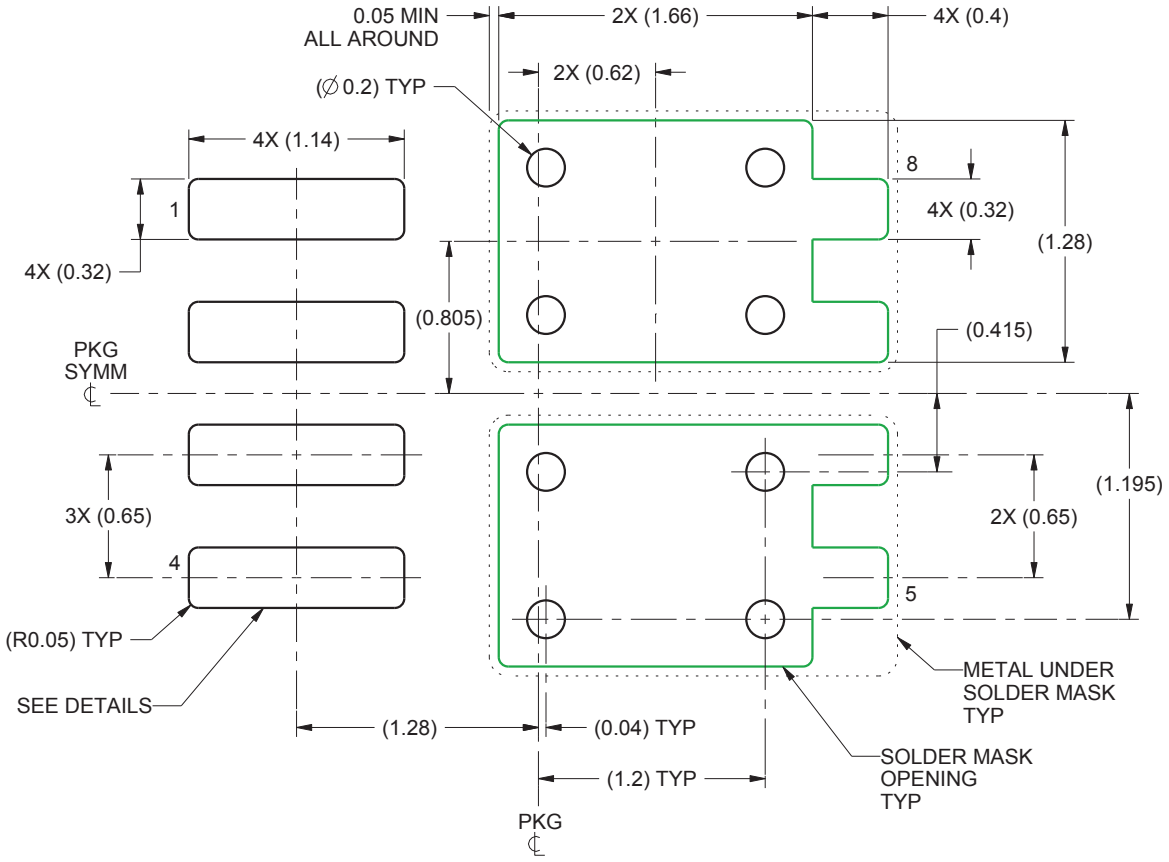
(2) 本图纸如有变更，恕不通知。

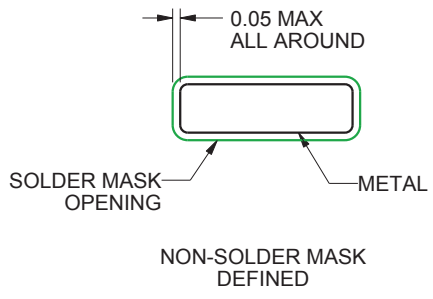
(3) 必须在印刷电路板上焊接封装散热焊盘，以获得良好的散热和机械性能。

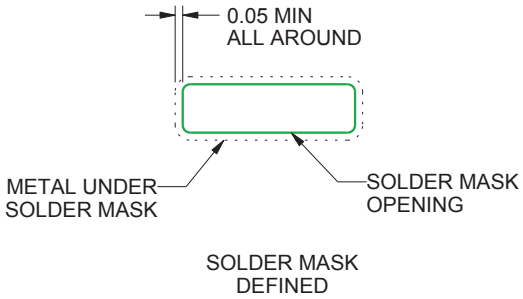
表 **1.** 引脚配置表

位置	名称	位置	名称
1	栅极 1	5	源极 2
2	漏极	6	源极 2
3	漏极	7	源极 1
4	栅极 2	8	源极 1

7.2 建议 PCB 布局





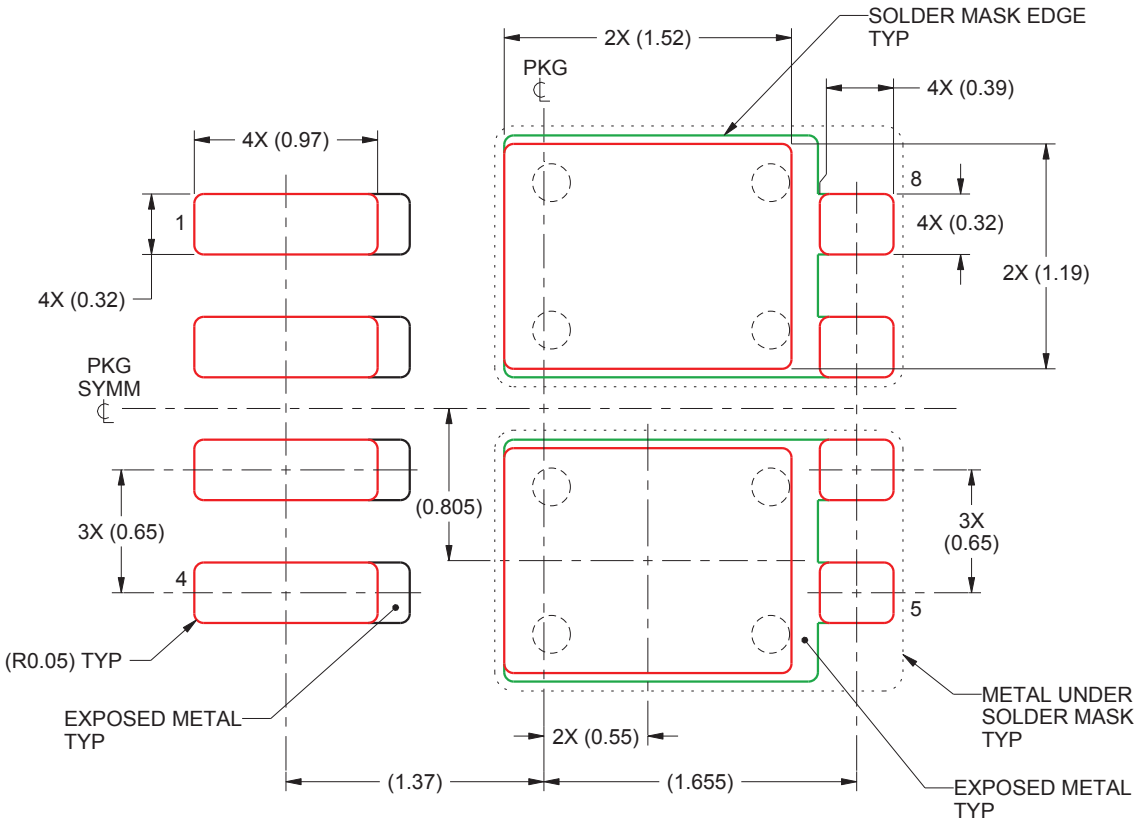


4222980/A 05/2016

(1) 此封装设计用于焊接到电路板的散热焊盘上。如需更多信息，请参见《QFN/SON PCB 连接》(SLUA271)。

(2) 根据具体应用决定是否选用通孔，请参见器件数据表。如需实施任意通孔，请参见此视图上的通孔位置。建议对焊锡膏下方的通孔进行填充、堵塞或包覆。

7.3 建议模板开口



(1) 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。IPC-7525 可能提供其他替代性设计建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87313DMS	ACTIVE	WSON	DMS	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD87313	Samples
CSD87313DMST	ACTIVE	WSON	DMS	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD87313	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要声明和免责声明

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