CSD85301Q2 20V 双路 N 沟道 NexFET™ 功率 MOSFET

1 特性

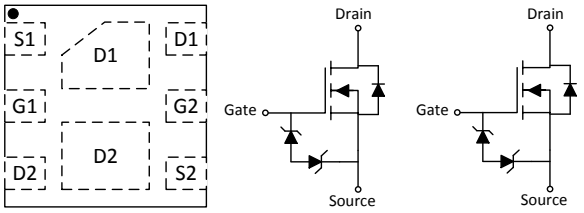
- 低导通电阻
- 两个独立的 MOSFET
- 节省空间的 SON 2mm × 2mm 塑料封装
- 针对 5V 栅极驱动器进行了优化
- 具有雪崩能力
- 无铅且无卤素
- 符合 RoHS

2 应用

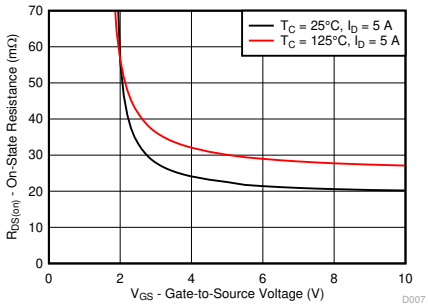
- 用于组网、电信和计算系统应用的负载点同步降压转换器
- 针对笔记本电脑 PC 和平板电脑的适配器或 USB 输入保护
- 电池保护

3 说明

CSD85301Q2 是一款 20V、23mΩ N 沟道器件，具有两个独立的 MOSFET，并且采用 SON 2mm x 2mm 塑料封装。这两个 FET 采用半桥配置，适用于同步降压等电源应用。此外，该器件还可用于适配器、USB 输入保护和电池充电应用。两个 FET 的漏源导通电阻均不高，可最大程度降低损耗并减少元件数，非常适合空间受限型应用。



顶视图和电路图



$R_{DS(on)}$ 与 V_{GS} 之间的关系

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	20		V
Q_g	栅极电荷总量 (4.5V)	4.2		nC
Q_{gd}	栅漏栅极电荷	1.0		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 1.8V	65	mΩ
		V_{GS} = 2.5V	33	mΩ
		V_{GS} = 3.8V	25	mΩ
		V_{GS} = 4.5V	23	mΩ
$V_{GS(th)}$	阈值电压	0.9		V

订购信息

器件(1)	介质	数量	封装	运输
CSD85301Q2	7 英寸卷带	3000	SON 2mm x 2mm 塑料封装	卷带包装
CSD85301Q2T	7 英寸卷带	250		

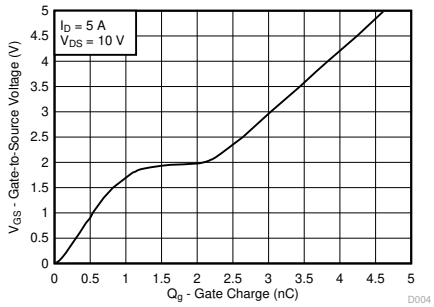
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	20	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流（受封装限制）	5.0	A
I_{DM}	脉冲漏极电流(1)	26	A
P_D	功率耗散(2)	2.3	W
T_J、T_{stg}	工作结温和贮存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 8.7A，L = 0.1mH，R_G = 25Ω	3.8	mJ

(1) 最大 $R_{\theta JA}$ = 185°C/W，脉冲持续时间 ≤ 100 μs，占空比 ≤ 1%。

(2) $R_{\theta JA}$ = 55°C/W，这是将 1 平方英寸、2oz 的铜焊盘安装在 0.06 英寸厚的 FR4 PCB 上时测得的典型值。



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

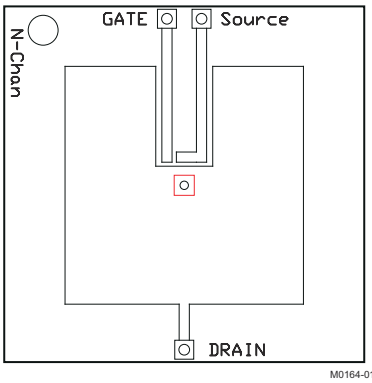
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0V, I_D = 250 μA	20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0V, V_{DS} = 16V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = 10V			10	μA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	0.9	1.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 1.8V, I_D = 0.5A		65	99	mΩ
		V_{GS} = 2.5V, I_D = 5A		33	39	mΩ
		V_{GS} = 3.8V, I_D = 5A		25	29	mΩ
		V_{GS} = 4.5V, I_D = 5A		23	27	mΩ
g_{fs}	Transconductance	V_{DS} = 2V, I_D = 5A		20		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		361	469	pF
C_{oss}	Output Capacitance			68	89	pF
C_{rss}	Reverse Transfer Capacitance			48	62	pF
R_G	Series Gate Resistance			7.3		Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 10V, I_D = 5A		4.2	5.4	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.0		nC
Q_{gs}	Gate Charge Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.5		nC
Q_{oss}	Output Charge	V_{DS} = 10V, V_{GS} = 0V		1.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 10V, V_{GS} = 5V, I_{DS} = 5A, R_G = 0Ω		6		ns
t_r	Rise Time			26		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			15		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 5A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 10V, I_F = 5A, di/dt = 300A/μs		7.2		nC
t_{rr}	Reverse Recovery Time			14		ns

4.2 Thermal Information

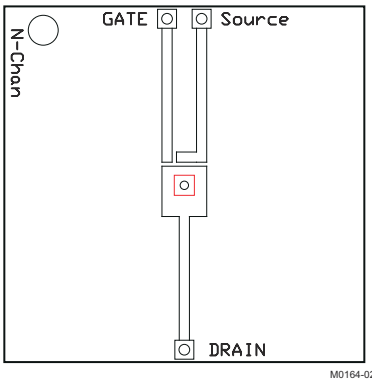
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)			70	°C/W
	Junction-to-Ambient Thermal Resistance(2)			185	

(1) Device mounted on FR4 material with 1 inch^2 (6.45cm^2), 2oz. (0.071mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.



Max $R_{\theta JA}$ = 70 when mounted on 1 inch^2 (6.45cm^2) of 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 185 when mounted on minimum pad area of 2oz. (0.071mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

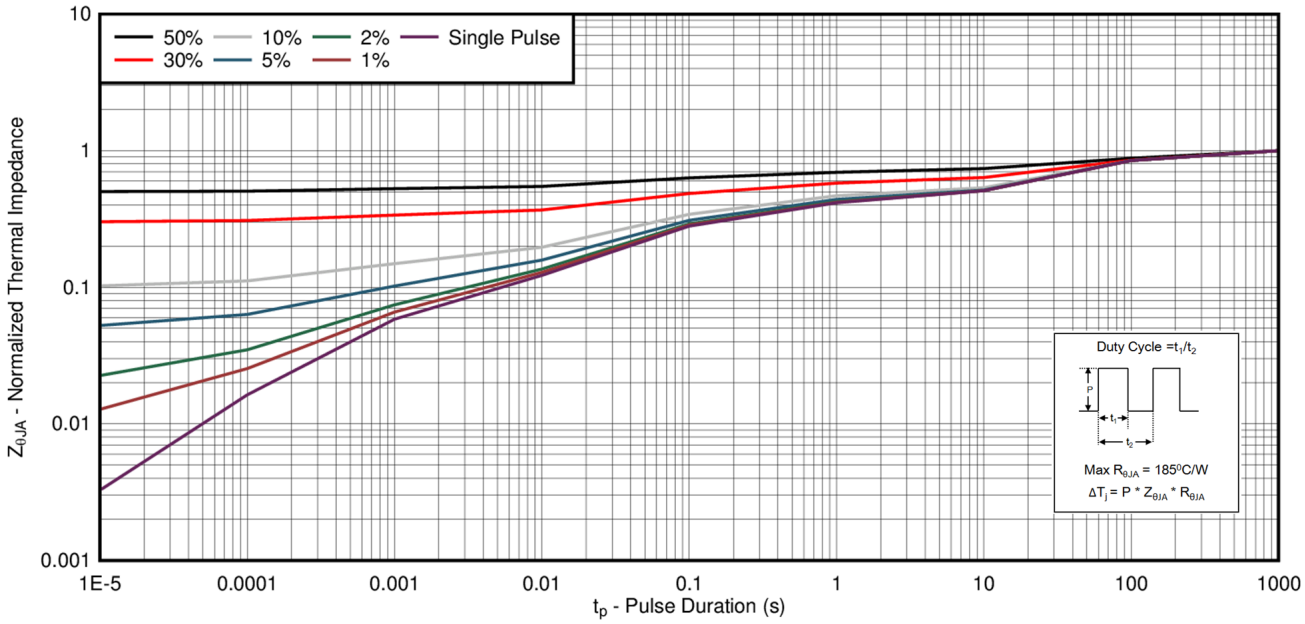


图 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

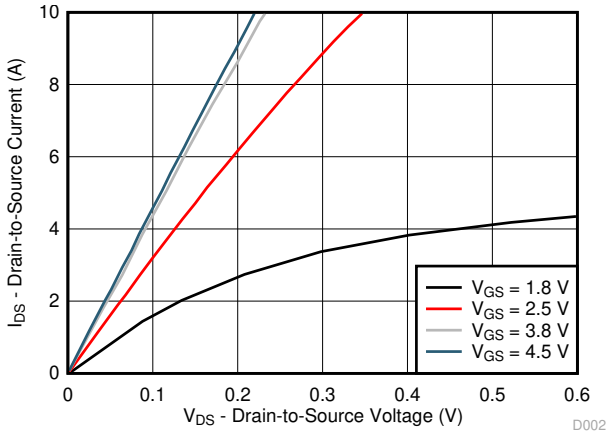
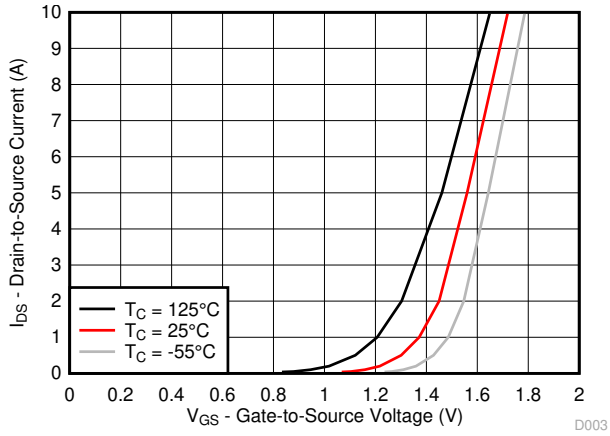
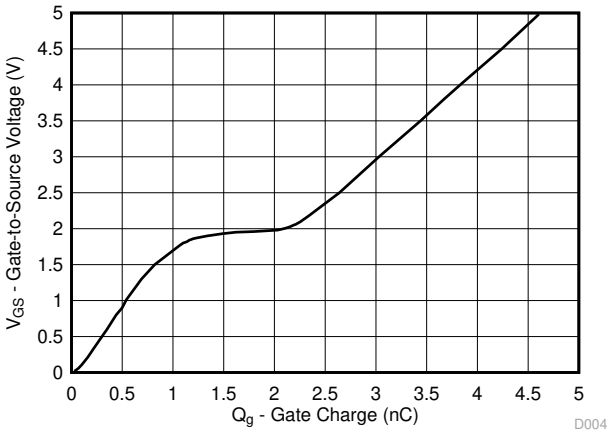


图 4-2. Saturation Characteristics



V_{DS} = 5V

图 4-3. Transfer Characteristics



I_D = 5A V_{DS} = 10V

图 4-4. Gate Charge

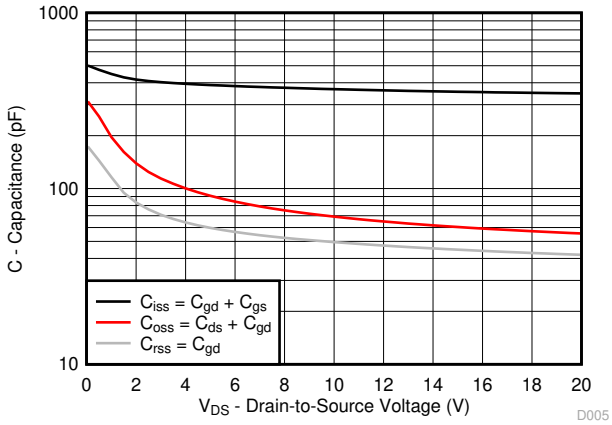
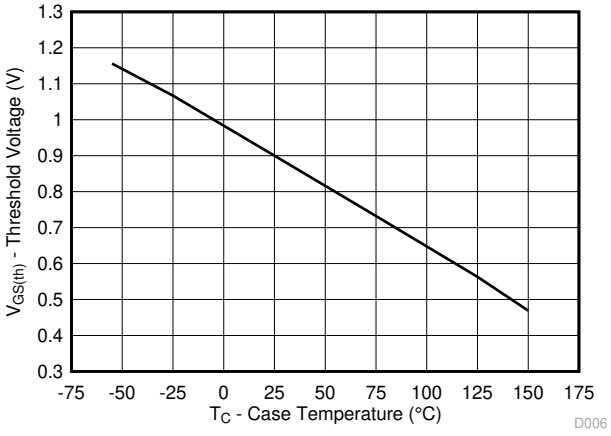


图 4-5. Capacitance



I_D = 5A

图 4-6. Threshold Voltage vs Temperature

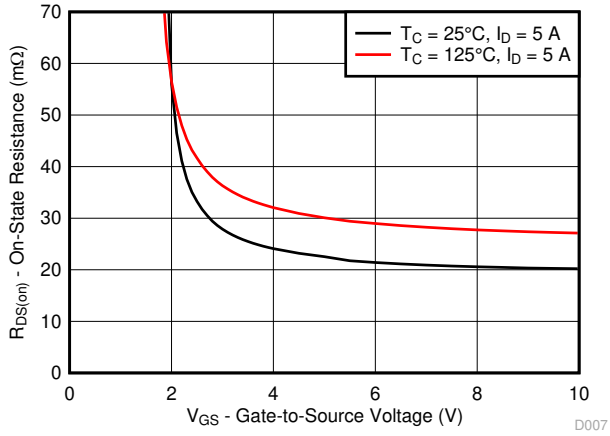
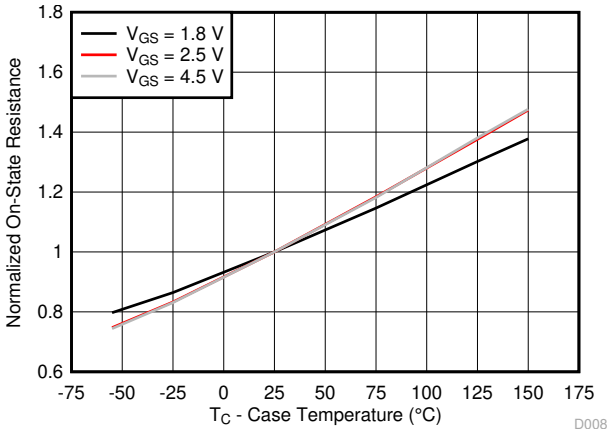


图 4-7. On-State Resistance vs Gate-to-Source Voltage

4.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = 5A

图 4-8. Normalized On-State Resistance vs Temperature

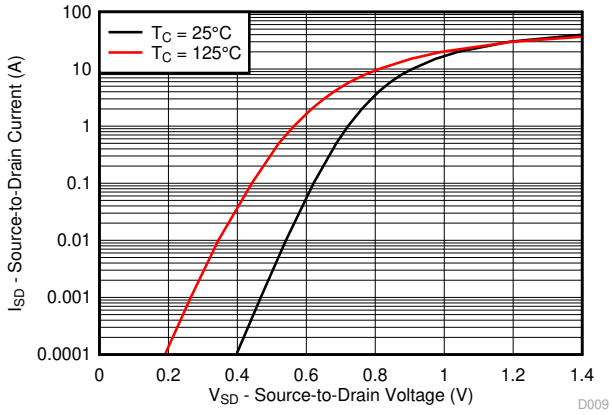
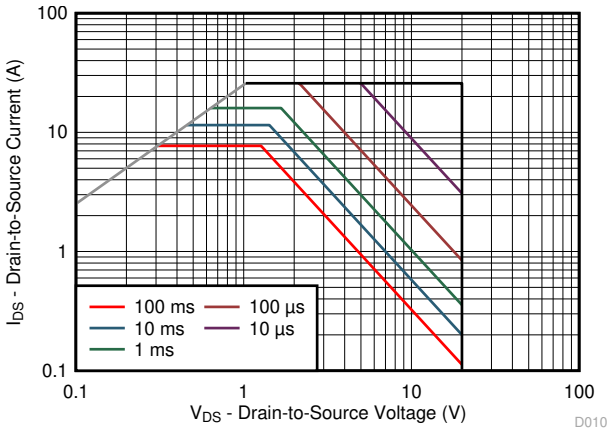


图 4-9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JA}$ = 185°C/W

图 4-10. Maximum Safe Operating Area

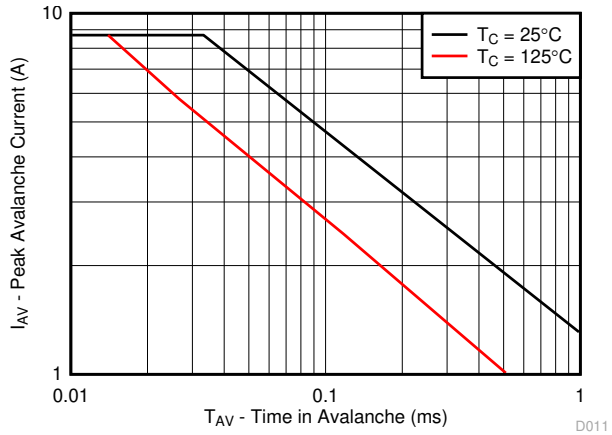


图 4-11. Single Pulse Unclamped Inductive Switching

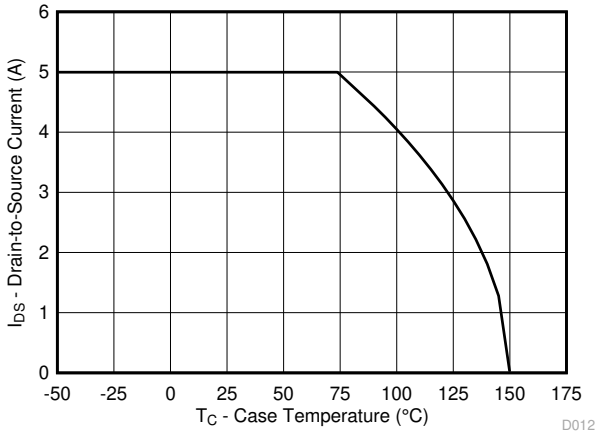


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.3 Trademarks

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所有商标均为其各自所有者的财产。

5.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

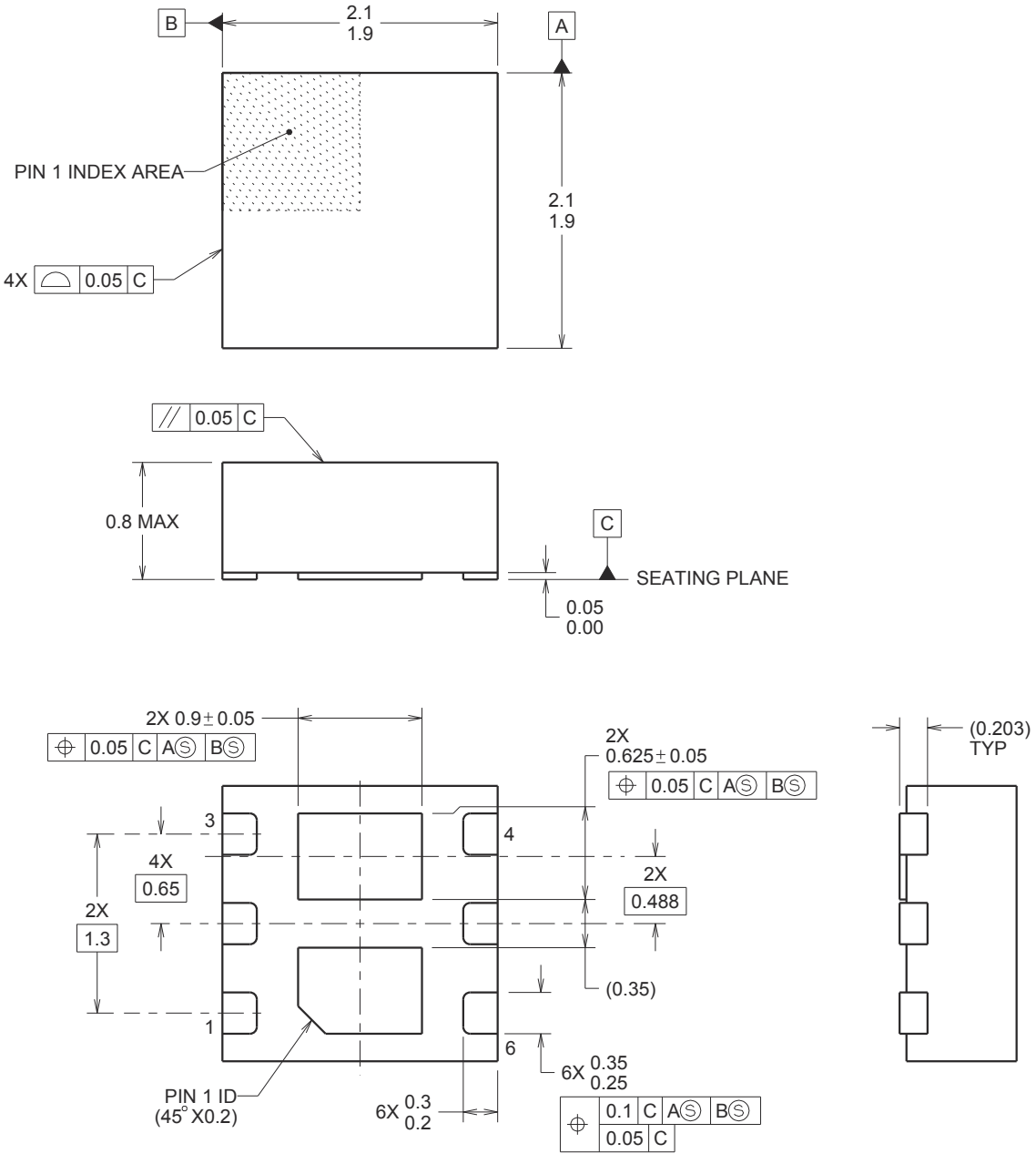
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2014) to Revision A (May 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

7 Mechanical, Packaging, and Orderable Information

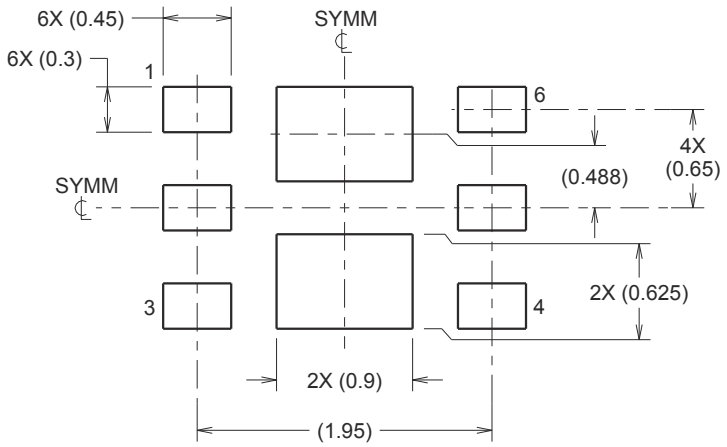
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions



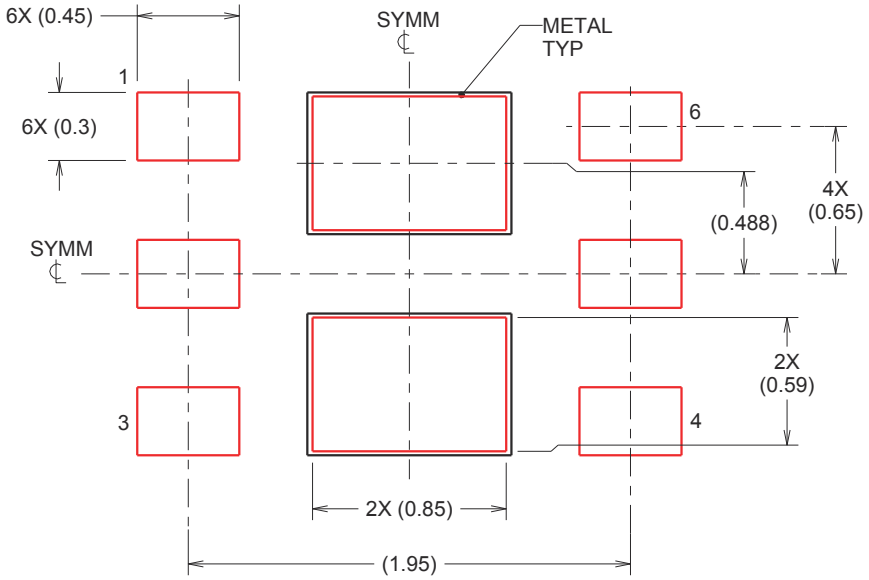
All dimensions are in mm, unless otherwise stated.

7.2 PCB Land Pattern



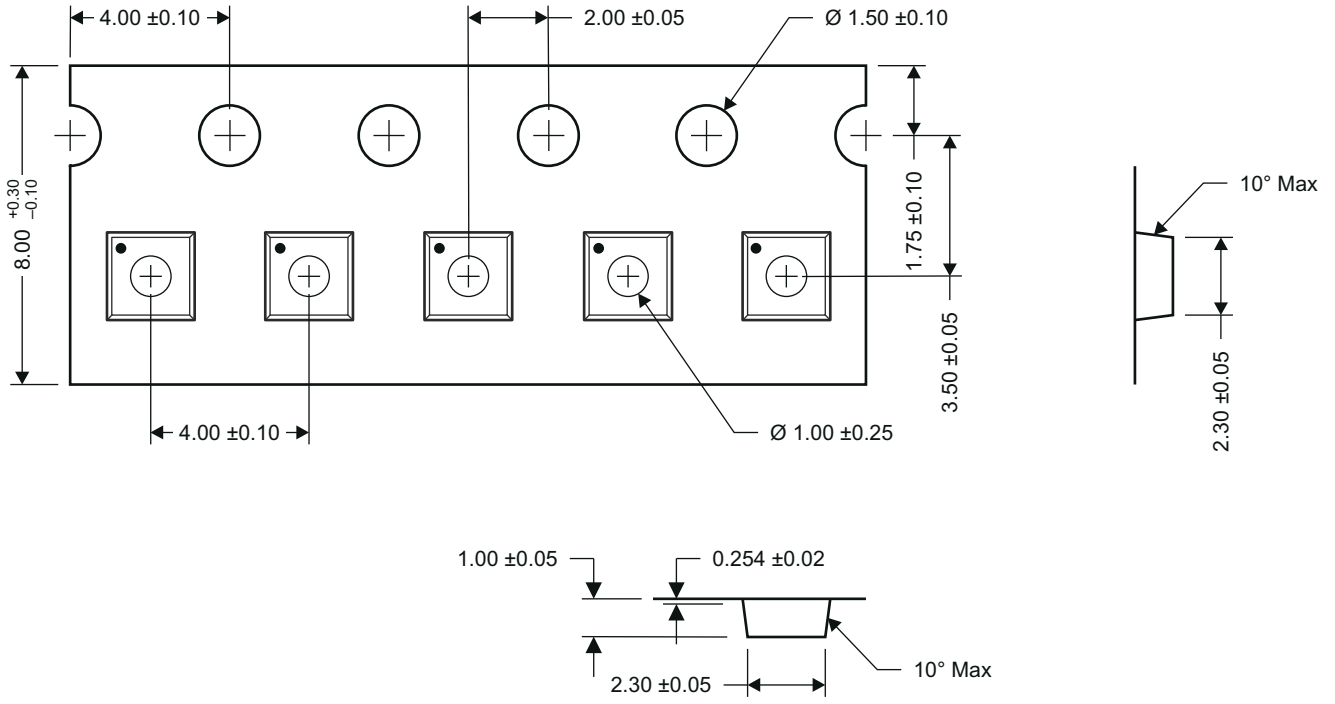
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise stated.

7.4 Q2 Tape and Reel Information



1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD85301Q2	Active	Production	WSON (DLV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531
CSD85301Q2.Z	Active	Production	WSON (DLV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531
CSD85301Q2G4.Z	Active	Production	WSON (DLV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531
CSD85301Q2T	Active	Production	WSON (DLV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531
CSD85301Q2T.Z	Active	Production	WSON (DLV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

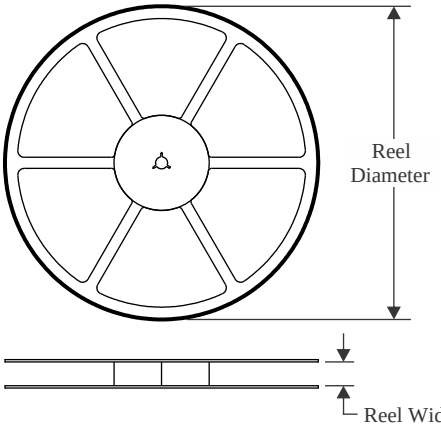
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

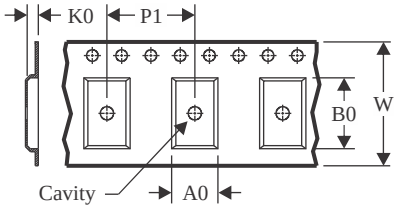
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

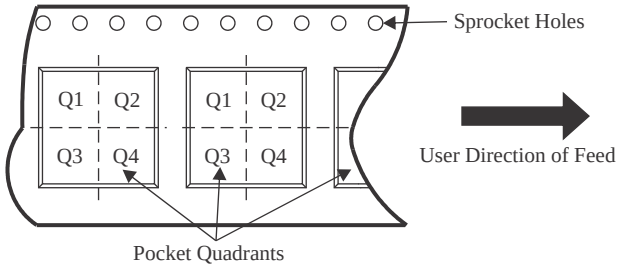


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

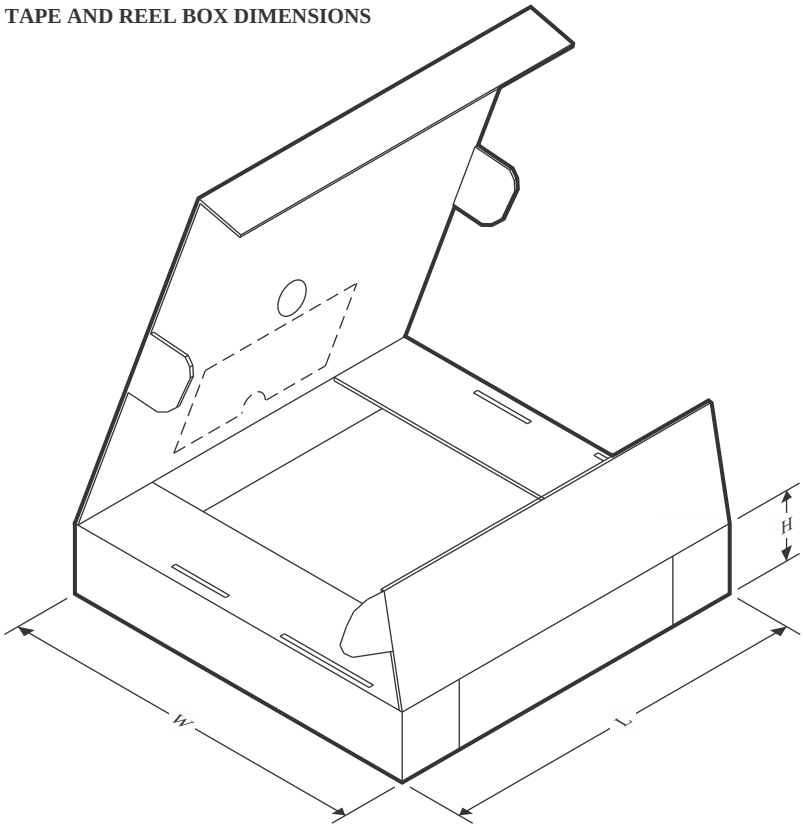
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD85301Q2	WSON	DLV	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD85301Q2T	WSON	DLV	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD85301Q2	WSON	DLV	6	3000	189.0	185.0	36.0
CSD85301Q2T	WSON	DLV	6	250	189.0	185.0	36.0

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