

20V P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

 查询样片: **CSD25402Q3A**

特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 低 $R_{DS(on)}$
- 无铅且无卤素
- 符合 RoHS 环保标准
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

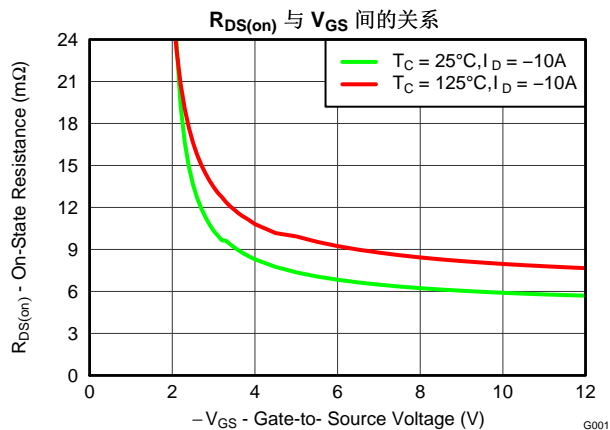
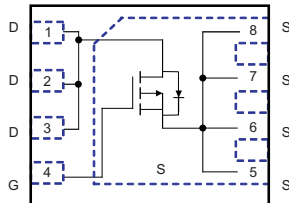
应用范围

- 直流-直流转换器
- 电池管理
- 负载开关
- 电池保护

说明

这款 -20V, 7.7mΩ NexFET™ 功率 MOSFET 被设计成最大限度地减少 SON 3 × 3 封装内的功率转换负载管理应用中的损耗, 此封装类型针对器件的尺寸提供出色的热性能。

顶视图



产品概述

V_{DS}	漏源极电压	-20	V
Q_g	栅极电荷总量 (-4.5V)	7.5	nC
Q_{gd}	栅极电荷漏极	1.1	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = -1.8V$	74 mΩ
		$V_{GS} = -2.5V$	13.3 mΩ
		$V_{GS} = -4.5V$	7.7 mΩ
V_{th}	阈值电压	-0.9	V

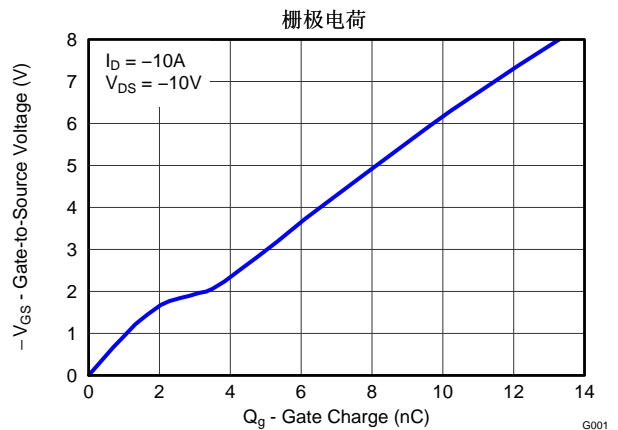
订购信息

器件	封装	介质	数量	出货
CSD25402Q3A	SON 3 × 3 塑料封装	13 英寸卷带	2500	卷带封装

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	+12 或 -12	V
I_D	持续漏极电流, $T_C = 25^\circ\text{C}$ 时测得	-72	A
	持续漏极电流 (受封装限制)	-35	A
	持续漏极电流 ⁽¹⁾	-15	A
I_{DM}	脉冲漏极电流 ⁽²⁾	-82	A
P_D	功率耗散 ⁽¹⁾	2.8	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$

- (1) $R_{\theta JA} = 55^\circ\text{C/W}$, 这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸² 铜过渡垫片 (2 盎司) 上测得的典型值。
- (2) 脉宽 $\leq 300\mu\text{s}$, 占空比 $\leq 2\%$



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

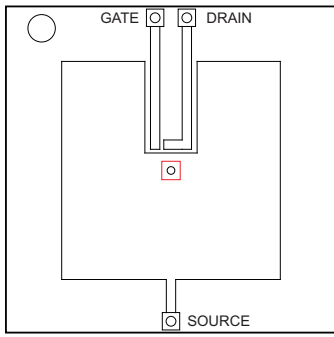
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
B _V DSS	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = -250 μA	-20			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = -16 V			-1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±12 V			-100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-0.65	-0.90	-1.15	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = -1.8 V, I _D = -1 A		74	300	mΩ
		V _{GS} = -2.5 V, I _D = -10 A		13.3	15.9	mΩ
		V _{GS} = -4.5 V, I _D = -10 A		7.7	8.9	mΩ
g _{fs}	Transconductance	V _{DS} = -10 V, I _D = -10 A		59		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = -10 V, f = 1 MHz		1380	1790	pF
C _{OSS}	Output Capacitance			763	992	pF
C _{RSS}	Reverse Transfer Capacitance			39	51	pF
R _G	Series Gate Resistance			3.7	7.4	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = -10 V, I _D = -10 A		7.5	9.7	nC
Q _{gd}	Gate Charge Gate to Drain			1.1		nC
Q _{gs}	Gate Charge Gate to Source			2.4		nC
Q _{g(th)}	Gate Charge at V _{th}			1.0		nC
Q _{OSS}	Output Charge	V _{DS} = -10 V, V _{GS} = 0 V		7.6		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -10 A, R _G = 5 Ω		10		ns
t _r	Rise Time			7		ns
t _{d(off)}	Turn Off Delay Time			25		ns
t _f	Fall Time			12		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _S = -10 A, V _{GS} = 0 V		-0.8	-1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = -8.5 V, I _F = -10 A, di/dt = 200 A/μs		10.3		nC
t _{rr}	Reverse Recovery Time			21		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

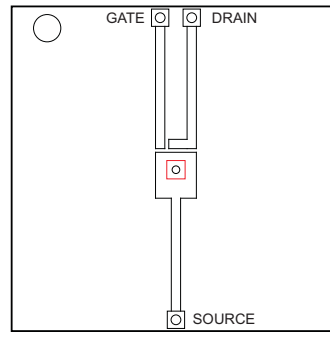
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			2.3	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			55	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on
1 inch² of 2 oz. Cu.

M0137-01



Max $R_{\theta JA} = 175^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2 oz. Cu.

M0137-02

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

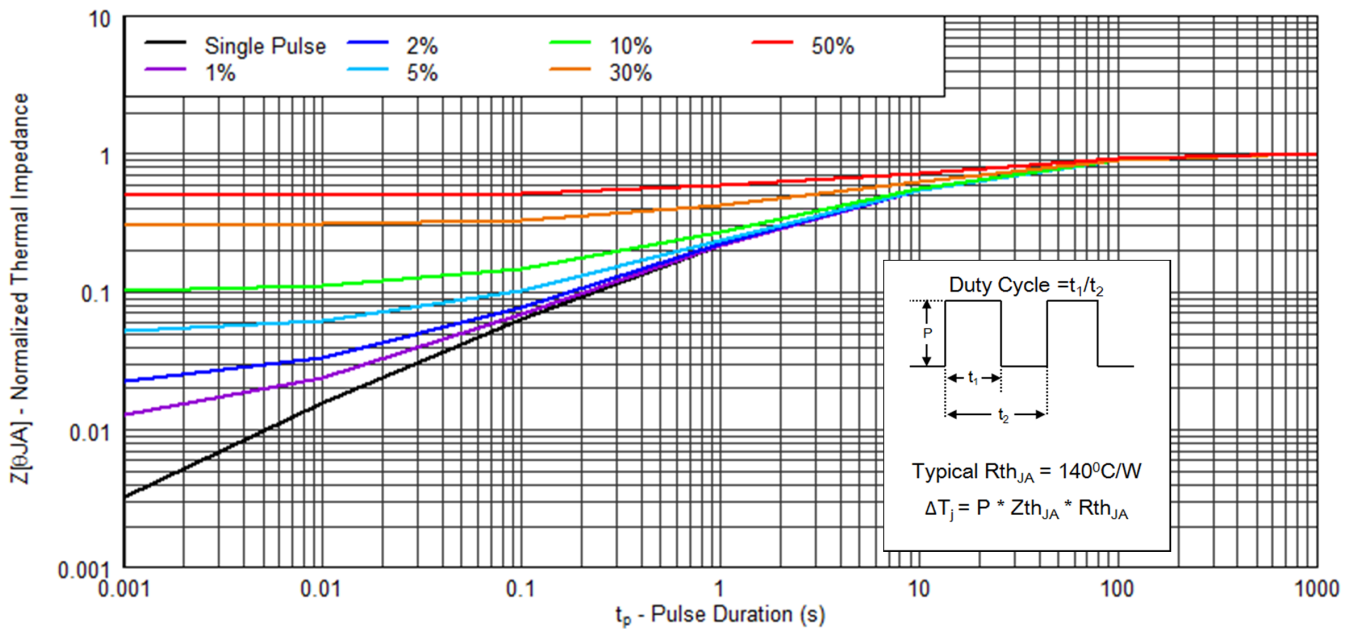


Figure 1. Transient Thermal Impedance

0001

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

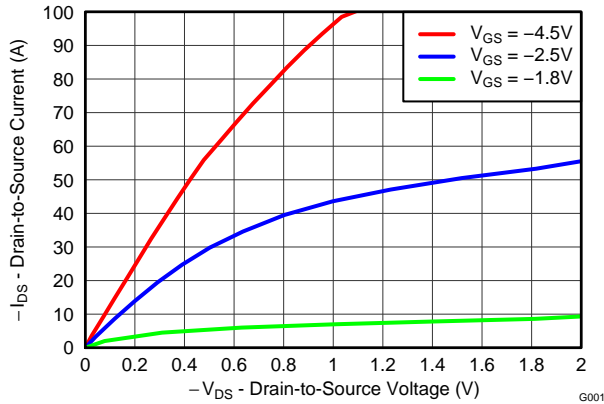


Figure 2. Saturation Characteristics

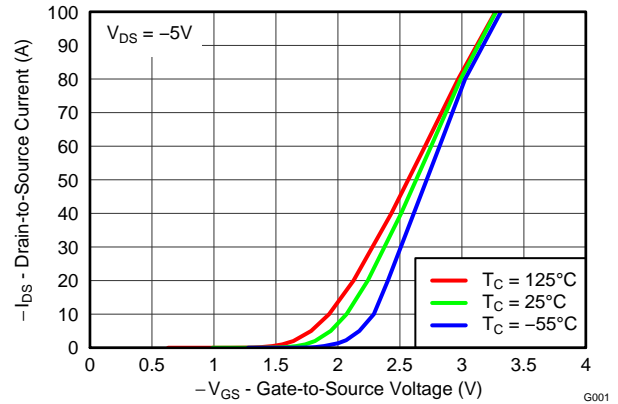


Figure 3. Transfer Characteristics

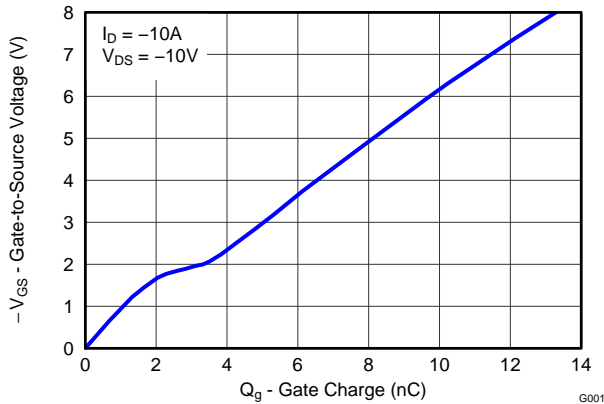


Figure 4. Gate Charge

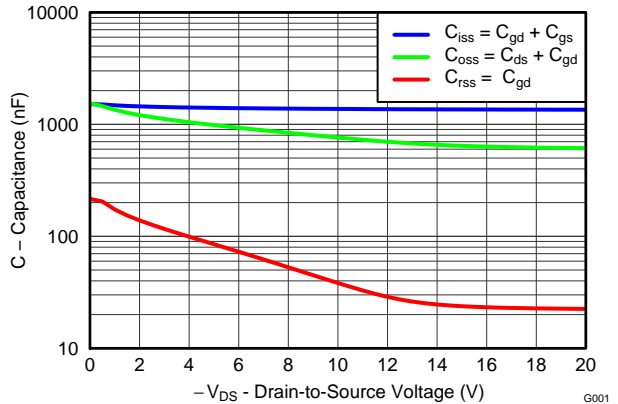


Figure 5. Capacitance

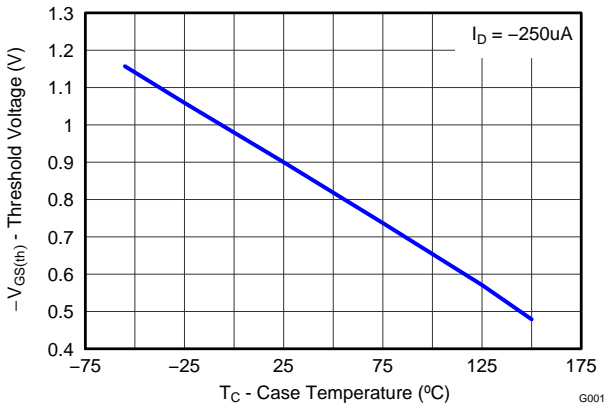


Figure 6. Threshold Voltage vs. Temperature

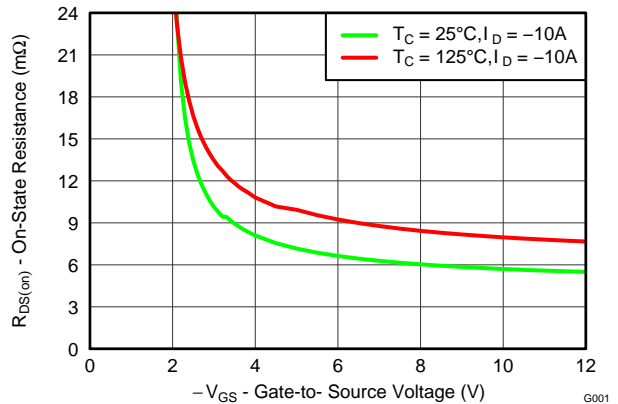


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

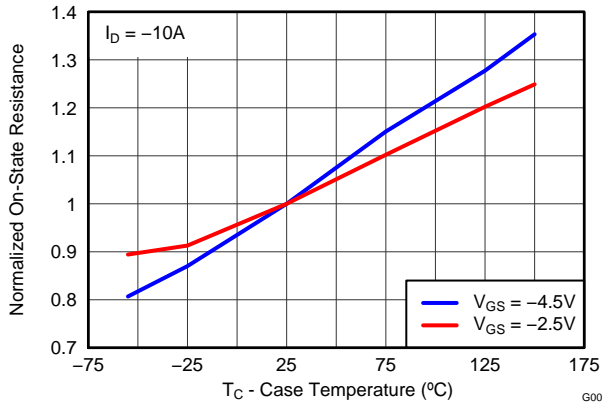


Figure 8. Normalized On-State Resistance vs. Temperature

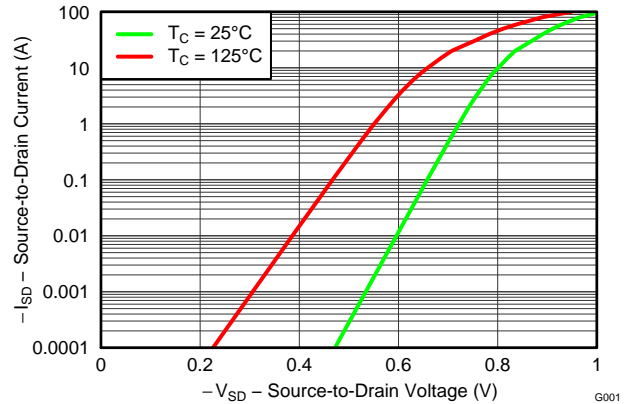


Figure 9. Typical Diode Forward Voltage

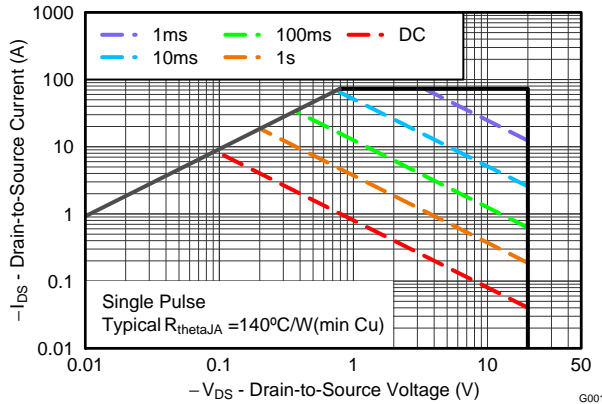


Figure 10. Maximum Safe Operating Area

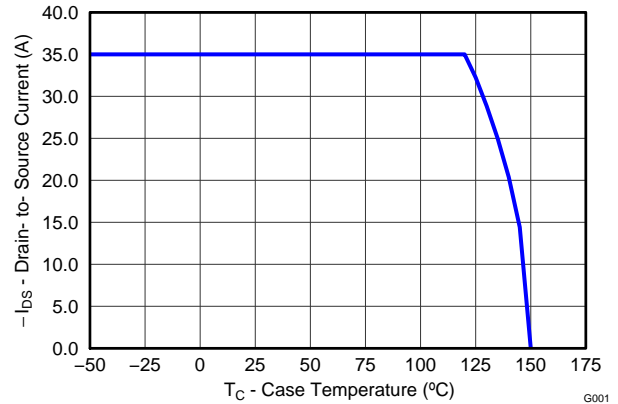
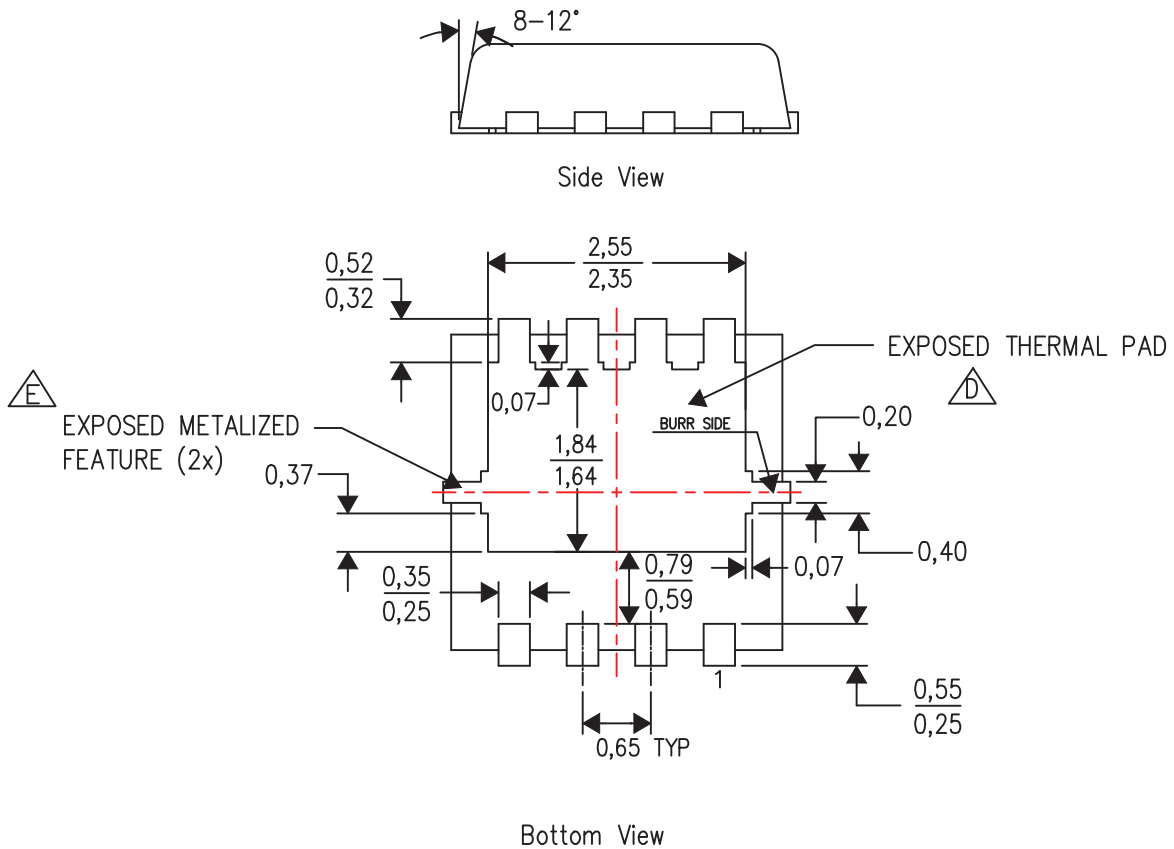
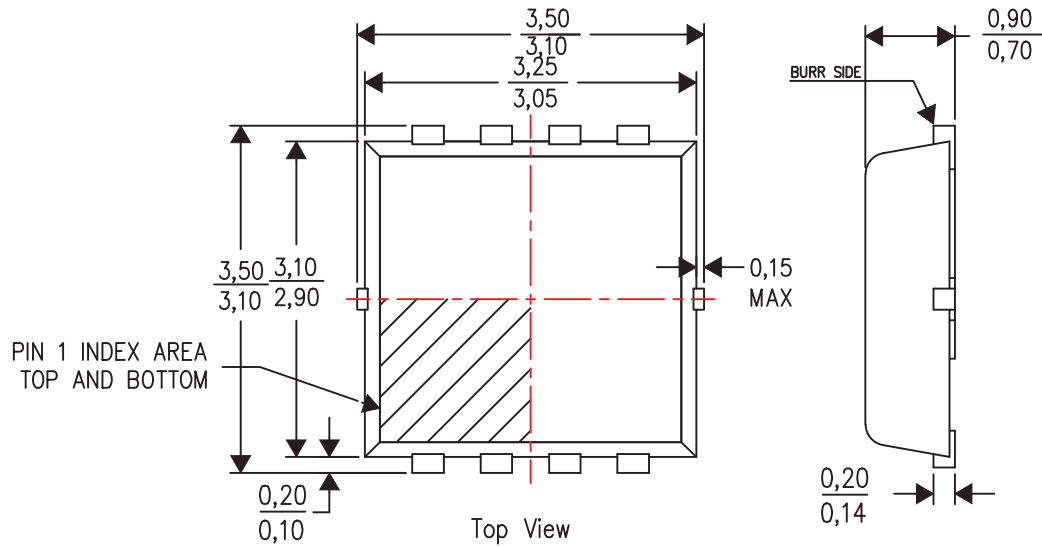


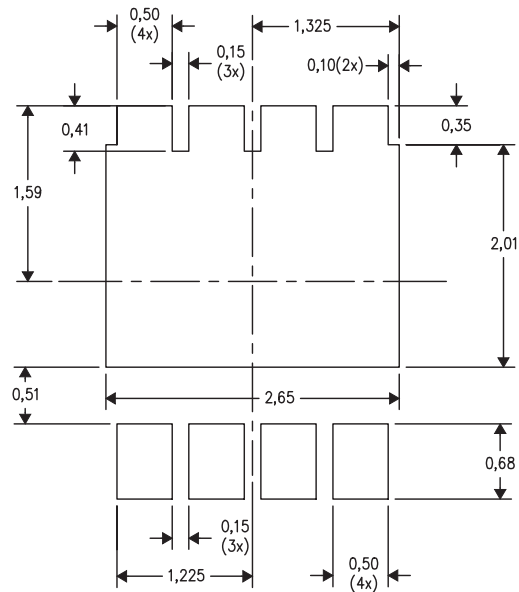
Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3A Package Dimensions

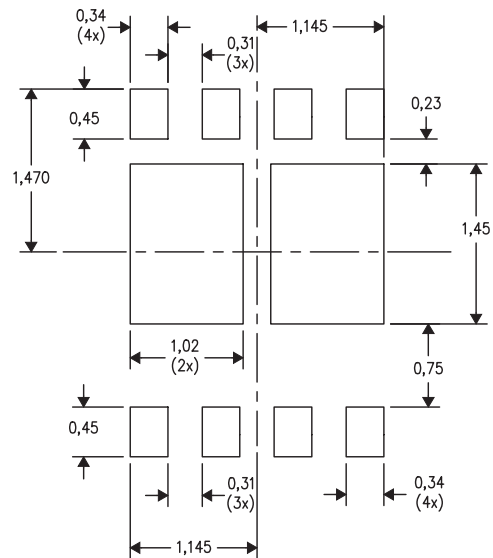


Q3A Recommended PCB Pattern

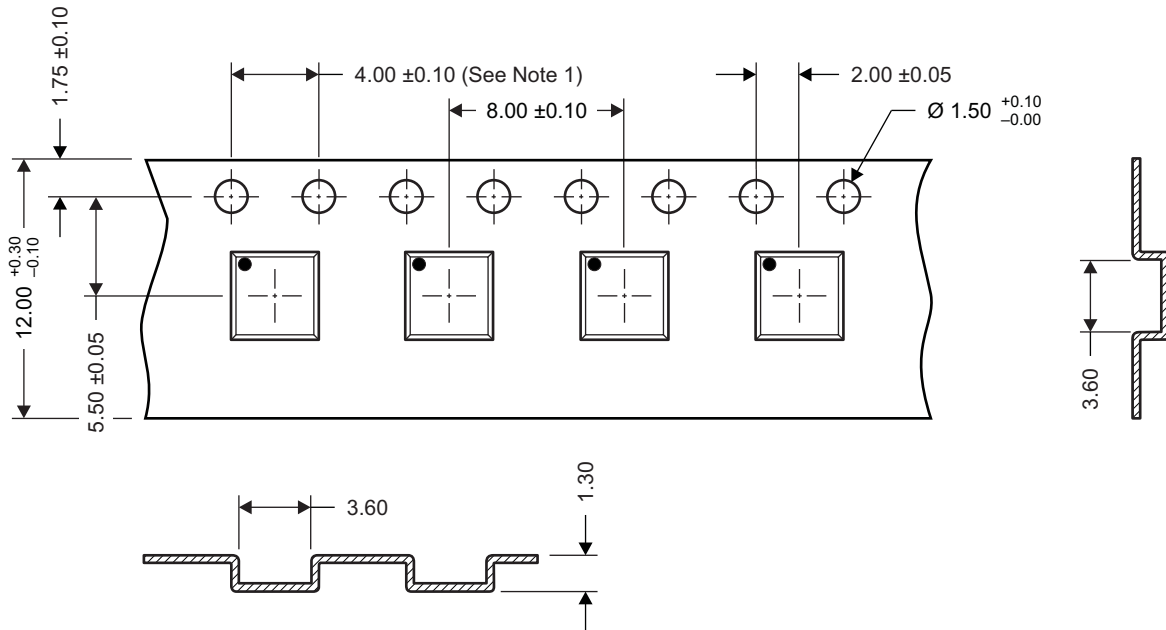


For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q3A Recommended Stencil Pattern



Q3A Tape and Reel Information



- Notes:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm, unless otherwise specified
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF reflow compatible

M0144-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25402Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	25402	Samples
CSD25402Q3AT	ACTIVE	VSONP	DNH	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	25402	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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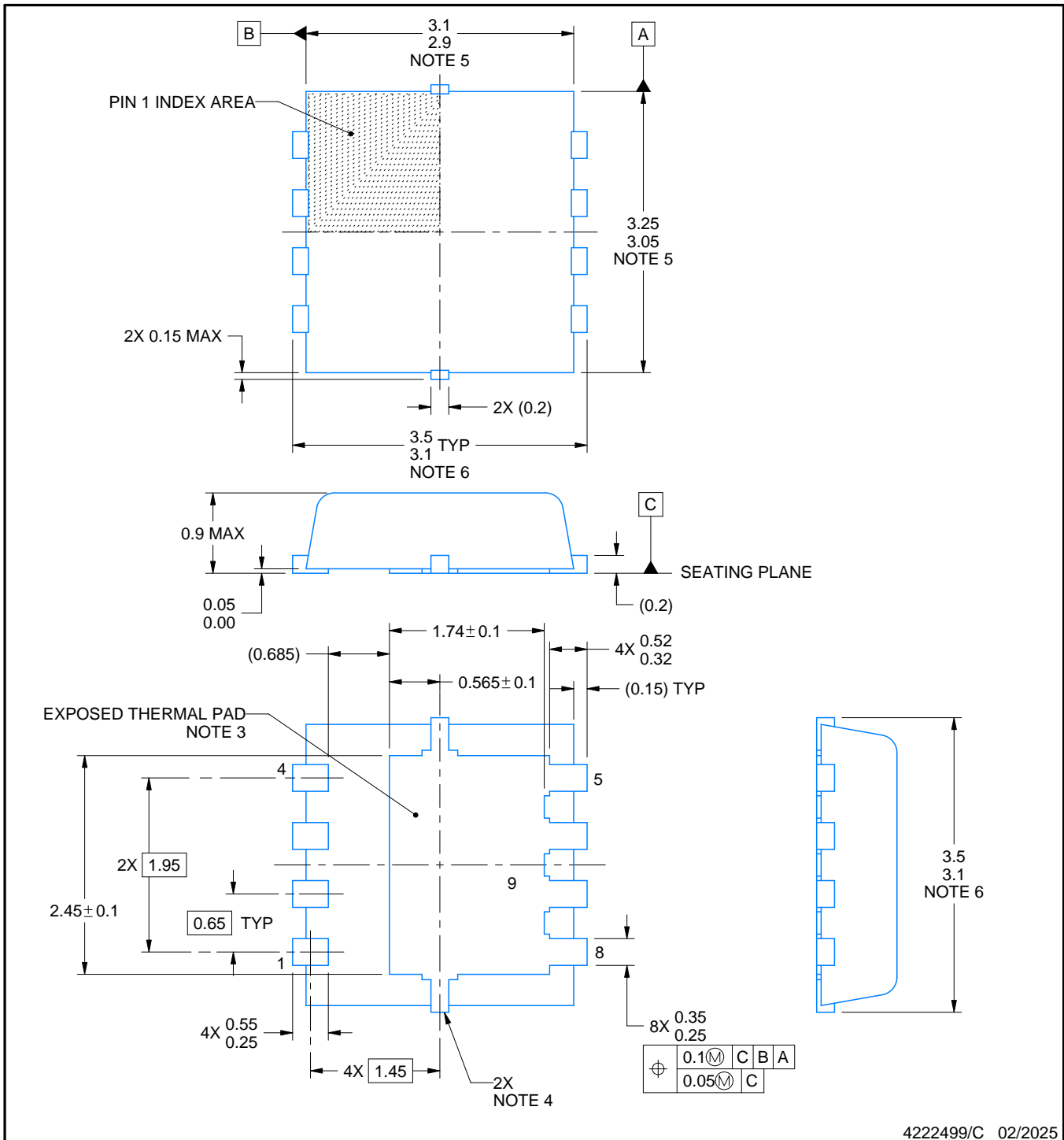
DNH0008A



PACKAGE OUTLINE

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

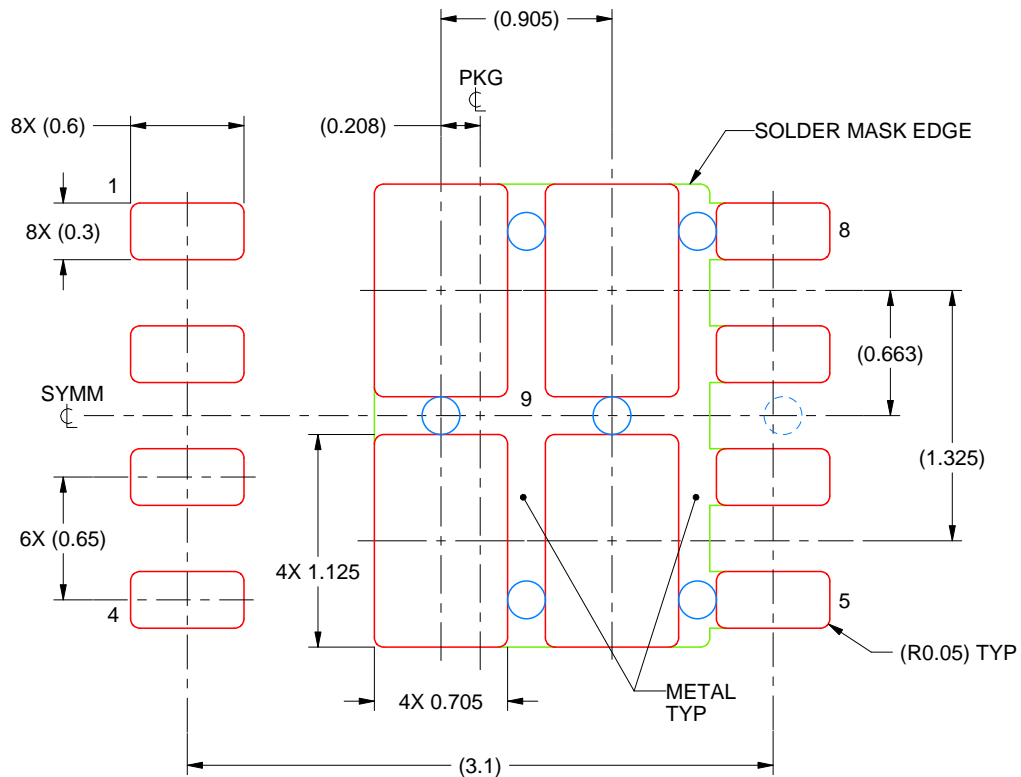
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
- Metalized features are supplier options and may not be on the package.
- These dimensions do not include mold flash protrusions or gate burrs.
- These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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