CSD17318Q2 30V N 通道 NexFET™ 功率 MOSFET

1 特性

- 针对 5V 栅极驱动器进行优化
- 低电容和电荷
- 低 $R_{DS(ON)}$
- 低热阻
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

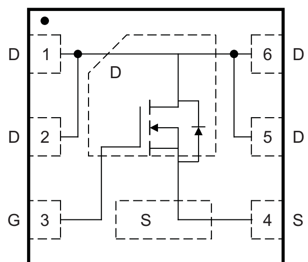
2 应用

- 存储、平板电脑和手持设备
- 优化负载开关 应用
- 直流/直流转换器
- 电池和负载管理 应用

3 说明

这款采用 2mm x 2mm SON 封装的 30V、12.6mΩ NexFET™功率 MOSFET 的设计被用来降低功率转换中的损耗， 并优化 5V 栅极驱动器。 2mm x 2mm SON 针对封装尺寸提供了出色的散热性能。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	6.0		nC
Q_{gd}	栅极电荷（栅极到漏极）	1.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V	20	mΩ
		V_{GS} = 4.5V	13.9	
		V_{GS} = 8V	12.6	
$V_{GS(th)}$	阈值电压	0.9		V

器件信息[(1)]

器件型号	数量	包装介质	封装	运输
CSD17318Q2	3000	7 英寸卷带	SON 2.00mm × 2.00mm 塑料封装	卷带封装
CSD17318Q2T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

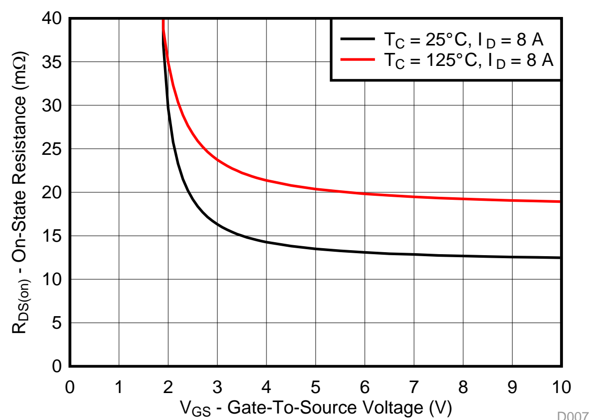
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流（受封装限制）	21.5	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	25	
	持续漏极电流[(1)]	10	
I_{DM}	脉冲漏极电流，T_A = 25°C 时测得[(2)]	68	A
P_D	功率耗散[(1)]	2.5	W
	功率耗散，T_C = 25°C	16	
T_J，T_{STG}	工作结温，储存温度	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲，I_D = 12.4A，L = 0.1mH，R_G = 25Ω	7.7	mJ

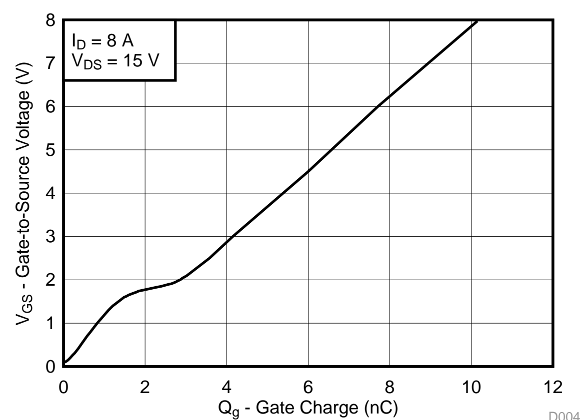
(1) $R_{\theta JA}$ = 55°C/W，这是在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸、2oz 铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 7°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

导通电阻与栅极至源极电压



栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Original (February 2017) to Revision A **Page**

- 更新后的 *机械数据* 图纸 ... 8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0 V, V_{GS} = 10 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	0.9	1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_D = 8 A		20	30	mΩ
		V_{GS} = 4.5 V, I_D = 8 A		13.9	16.9	
		V_{GS} = 8 V, I_D = 8 A		12.6	15.1	
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 8 A		42		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, *ƒ* = 1 MHz		676	879	pF
C_{oss}	Output capacitance			71	92	pF
C_{rss}	Reverse transfer capacitance			39	51	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 8 A		6.0		nC
Q_{gd}	Gate charge gate-to-drain			1.3		nC
Q_{gs}	Gate charge gate-to-source			1.5		nC
$Q_{g(th)}$	Gate charge at Vth			0.7		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		2.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 8 A, R_G = 2 Ω		5		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 8 A, V_{GS} = 0 V		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DD}= 15 V, I_F = 8 A, di/dt = 300 A/μs		2.9		nC
t_{rr}	Reverse recovery time			12		ns

5.2 Thermal Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{θJC}$	Thermal resistance junction-to-case[1]			7.9	°C/W
$R_{θJA}$	Thermal resistance junction-to-ambient[1][2]			65	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-inch (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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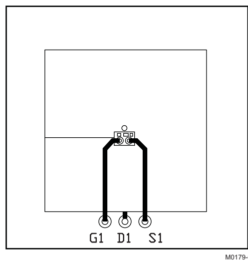
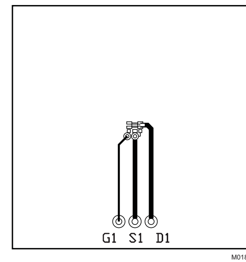


Max $R_{\theta JA}$ = 65°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

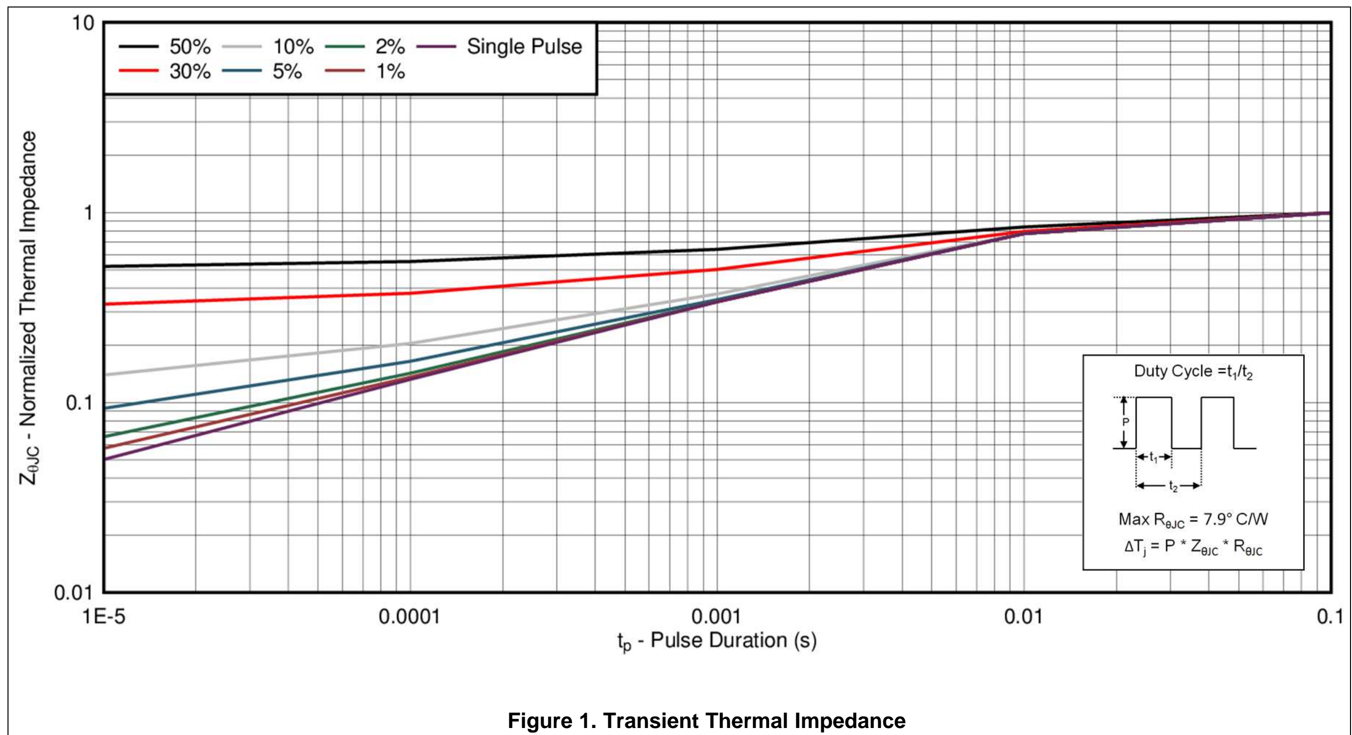


Figure 1. Transient Thermal Impedance

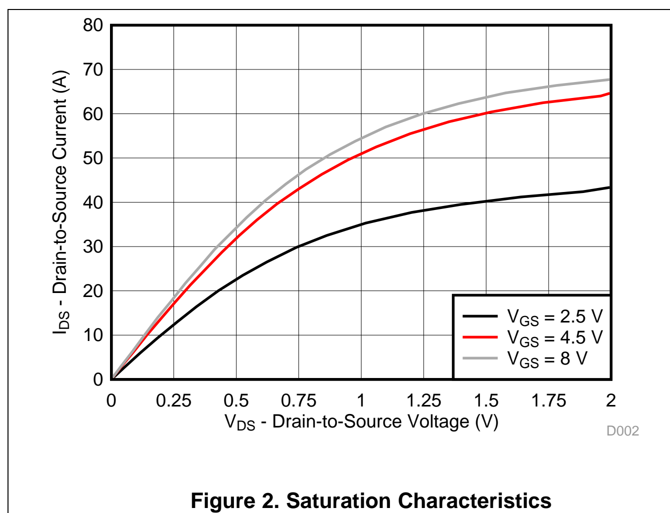


Figure 2. Saturation Characteristics

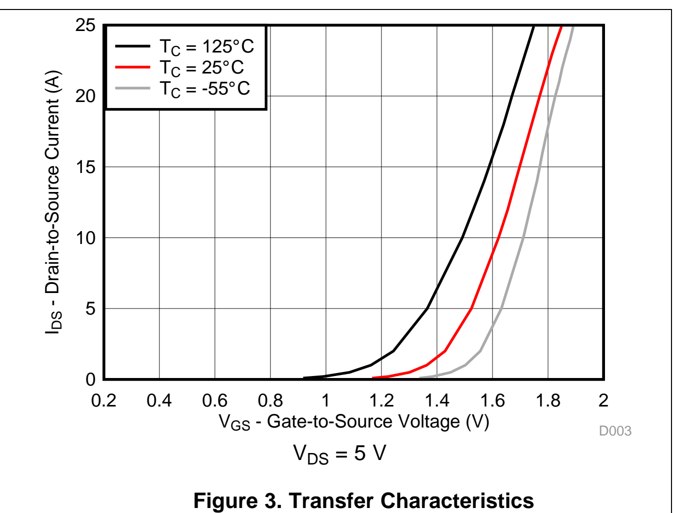


Figure 3. Transfer Characteristics

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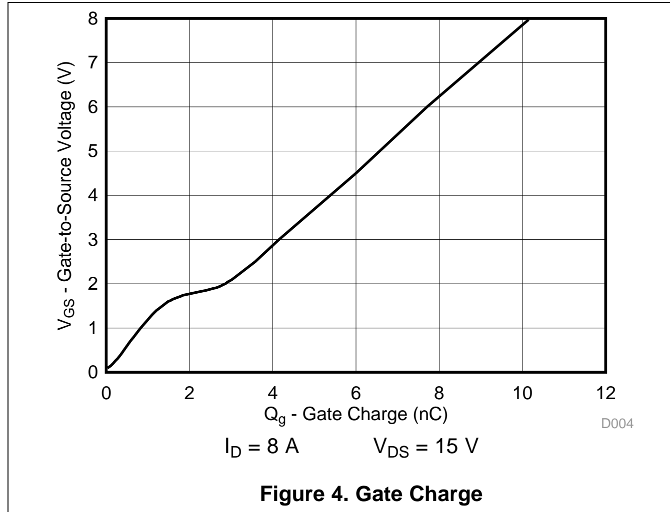
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



I_D = 8 A V_{DS} = 15 V

Figure 4. Gate Charge

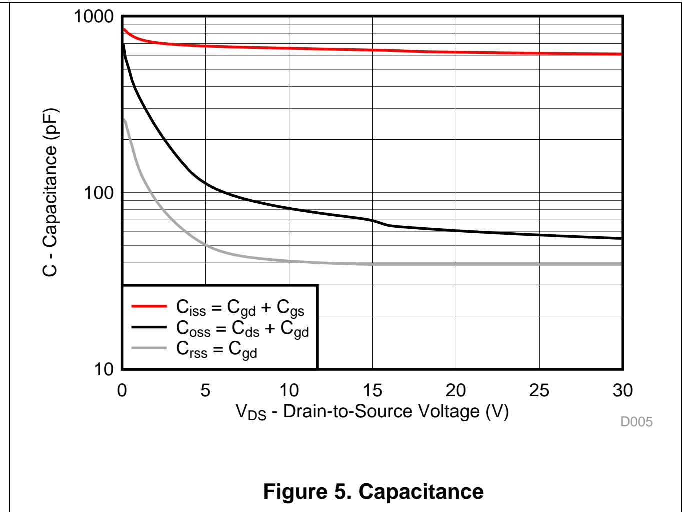
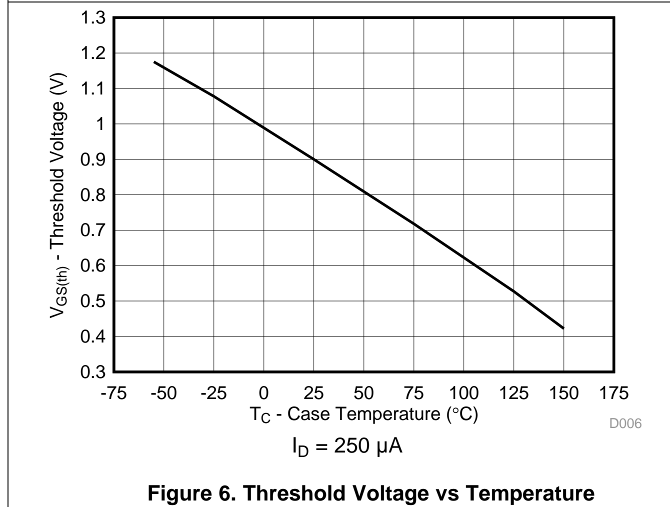
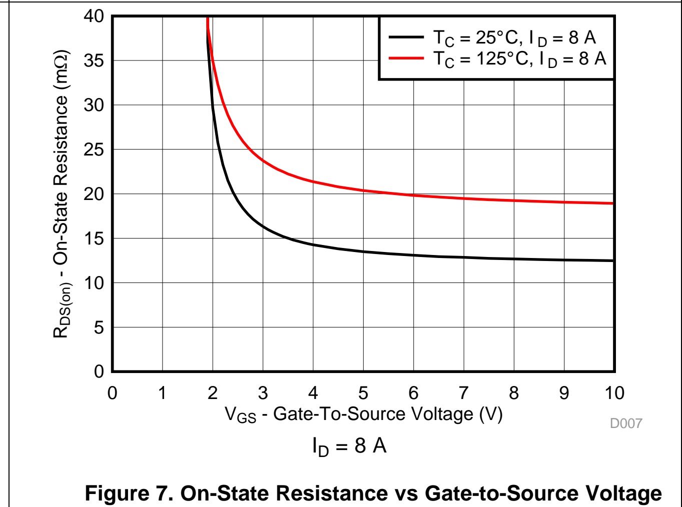


Figure 5. Capacitance



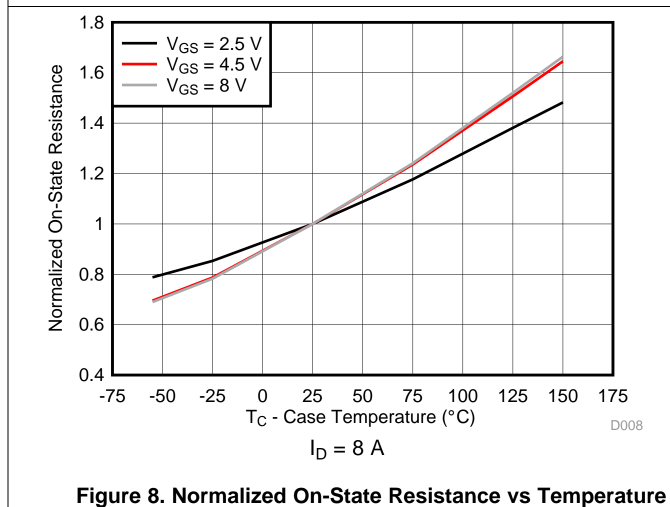
I_D = 250 μA

Figure 6. Threshold Voltage vs Temperature



I_D = 8 A

Figure 7. On-State Resistance vs Gate-to-Source Voltage



I_D = 8 A

Figure 8. Normalized On-State Resistance vs Temperature

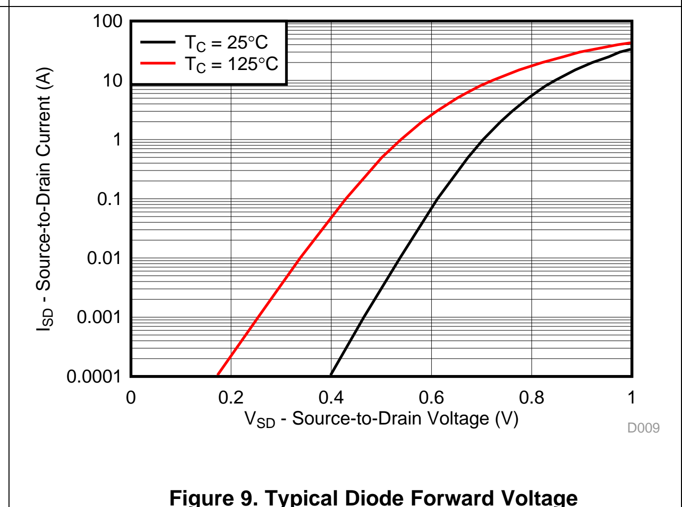


Figure 9. Typical Diode Forward Voltage

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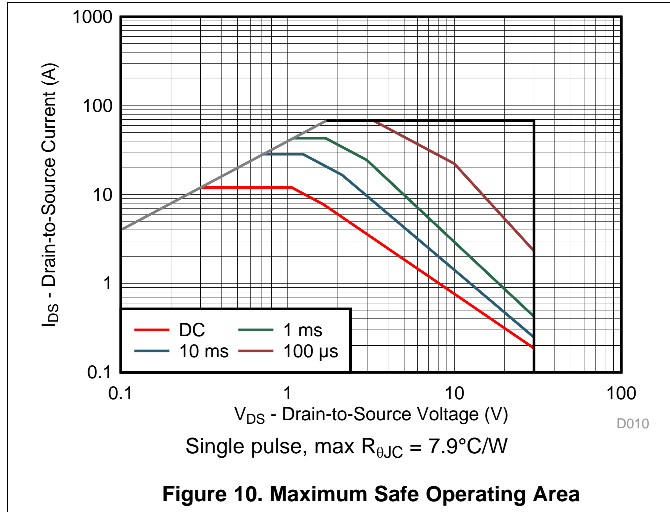
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



Single pulse, max $R_{\theta JC}$ = 7.9°C/W

Figure 10. Maximum Safe Operating Area

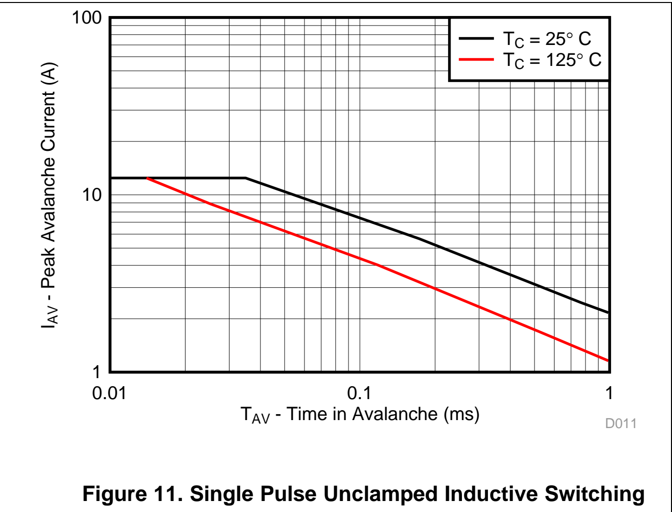


Figure 11. Single Pulse Unclamped Inductive Switching

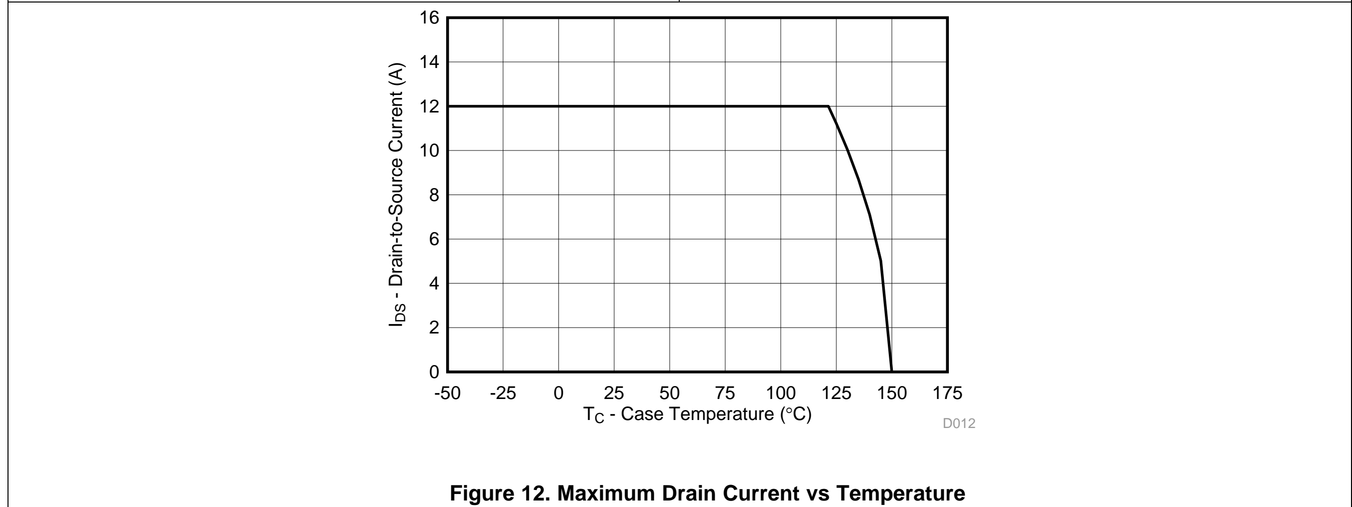


Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

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All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

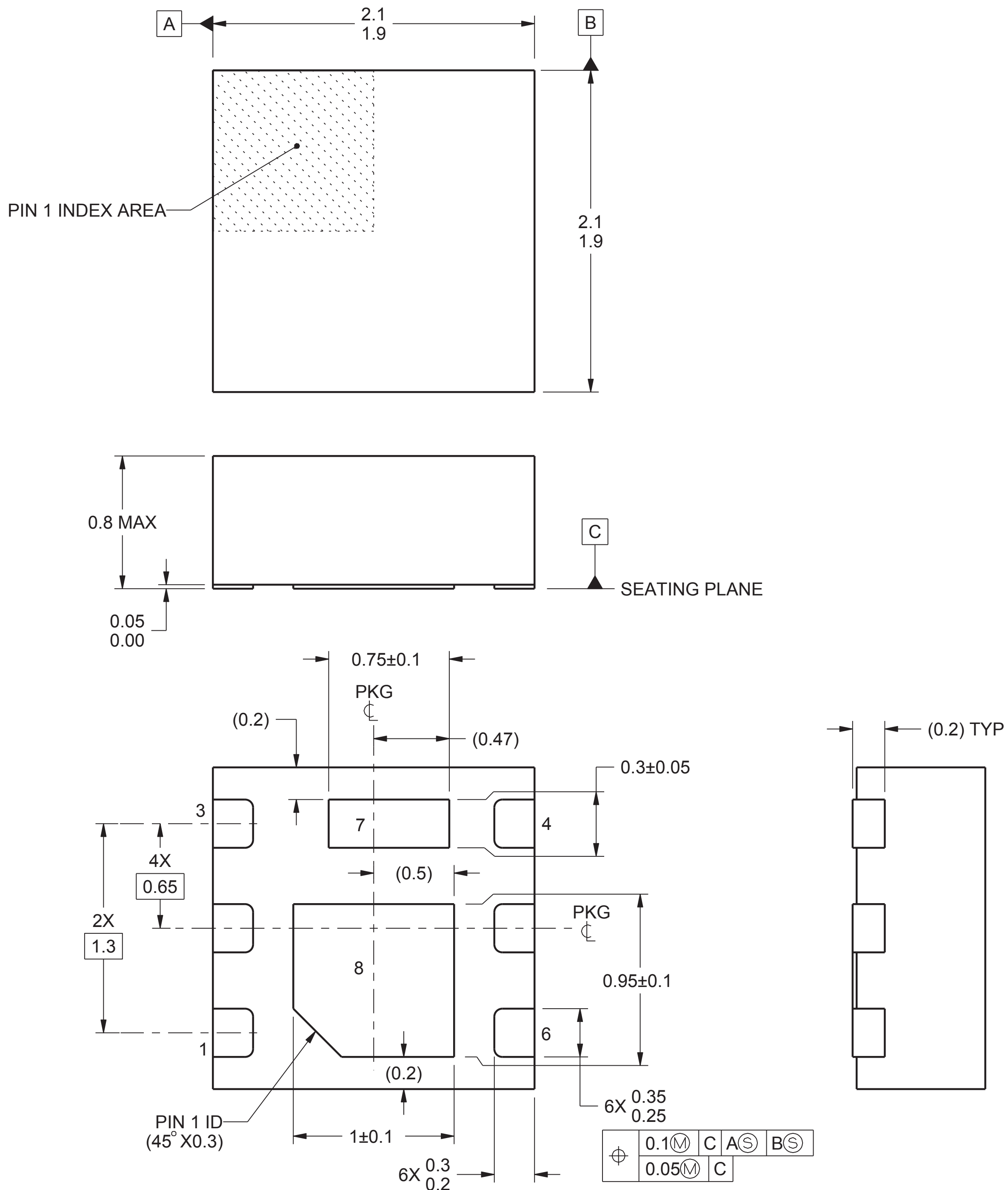
6.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械数据

7.1 Q2 封装尺寸



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。

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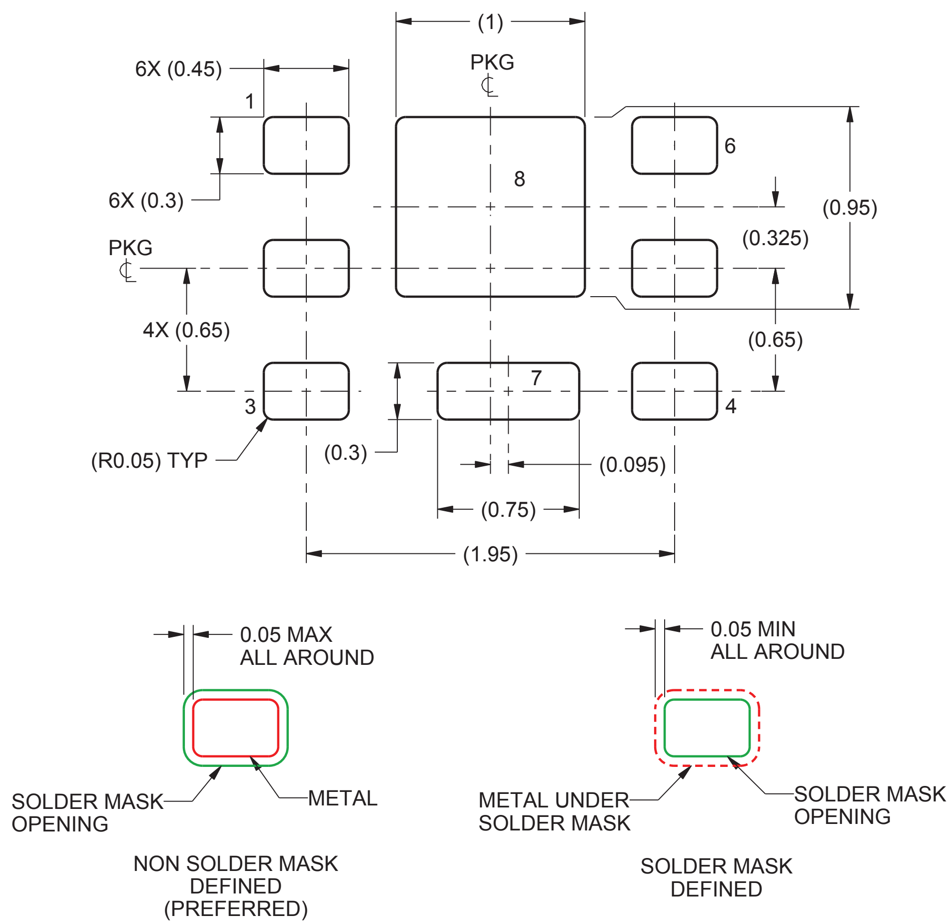
Q2 封装尺寸 (接下页)

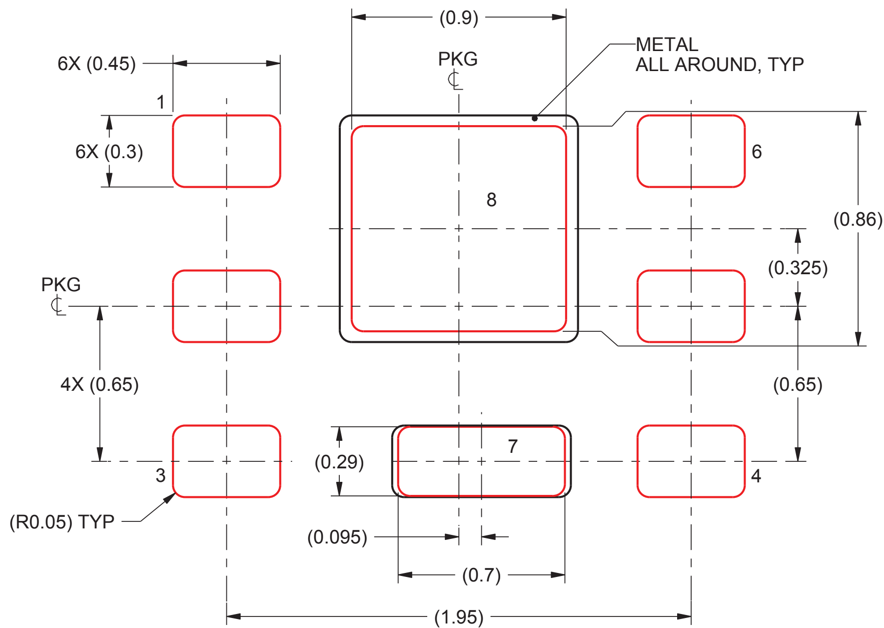
7.1.1 建议 PCB 布局



1. 此封装设计用于焊接到电路板的散热焊盘上。更多信息，请参见*《QFN/SON PCB 连接》*（文献编号：SLUA271）。

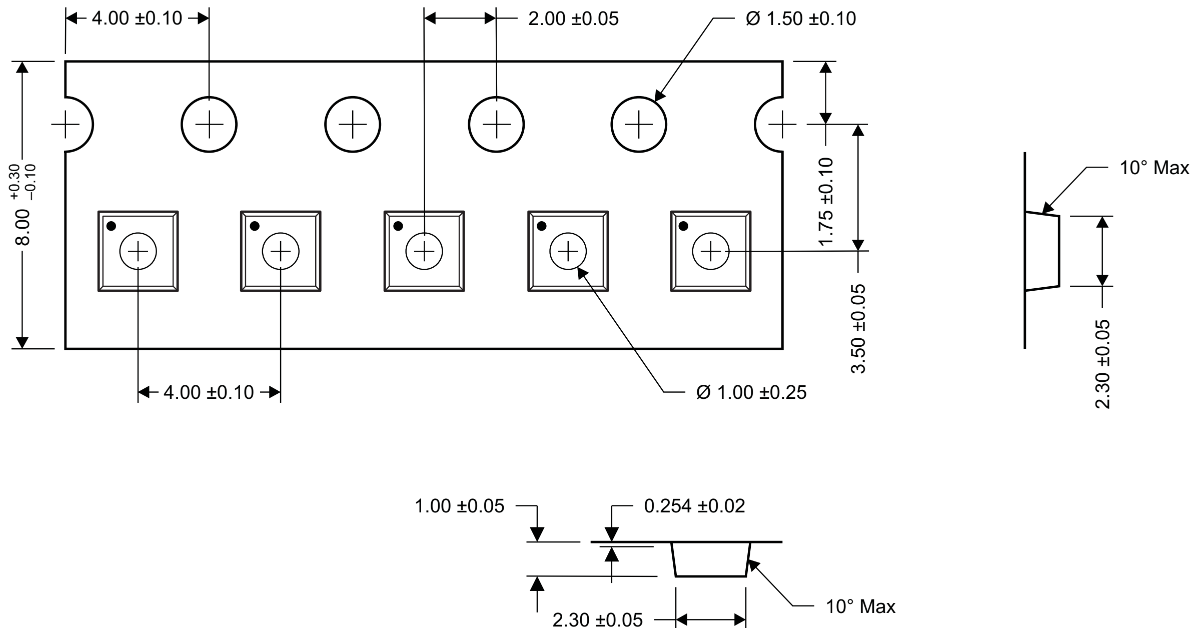
Q2 封装尺寸 (接下页)

7.1.2 推荐的模版布局



1. 具有漏斗形壁和圆角的激光切割窗孔将提供更佳的焊锡膏脱离。IPC-7525 可能提供其他替代性设计建议。

7.2 Q2 卷带信息



Notes: 1. 测自链齿孔中心线到孔眼中心线。
2. 10 个链齿孔的累积容差为 ±0.20。
3. 提供了其他材料。
4. 卷带的 SR 典型值最大为 10^9 OHM/SQ。
5. 所有尺寸单位均为 mm，除非另有说明。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17318Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1718	Samples
CSD17318Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1718	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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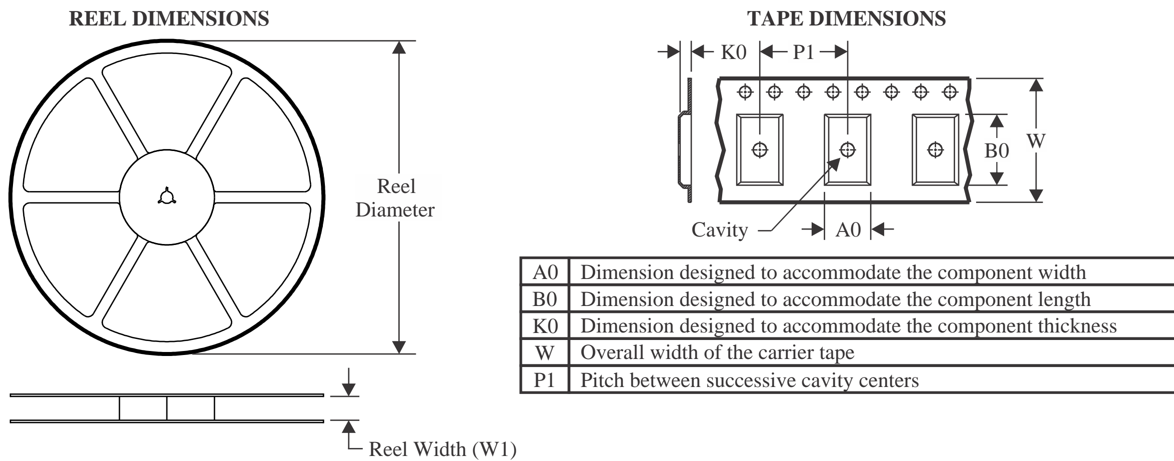
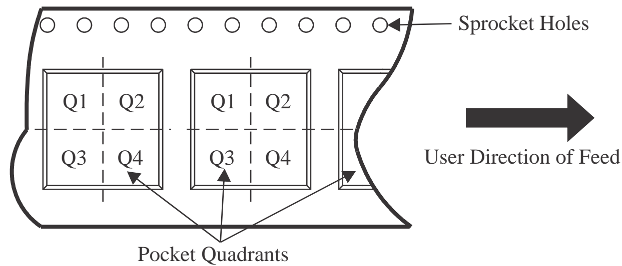
TAPE AND REEL INFORMATION

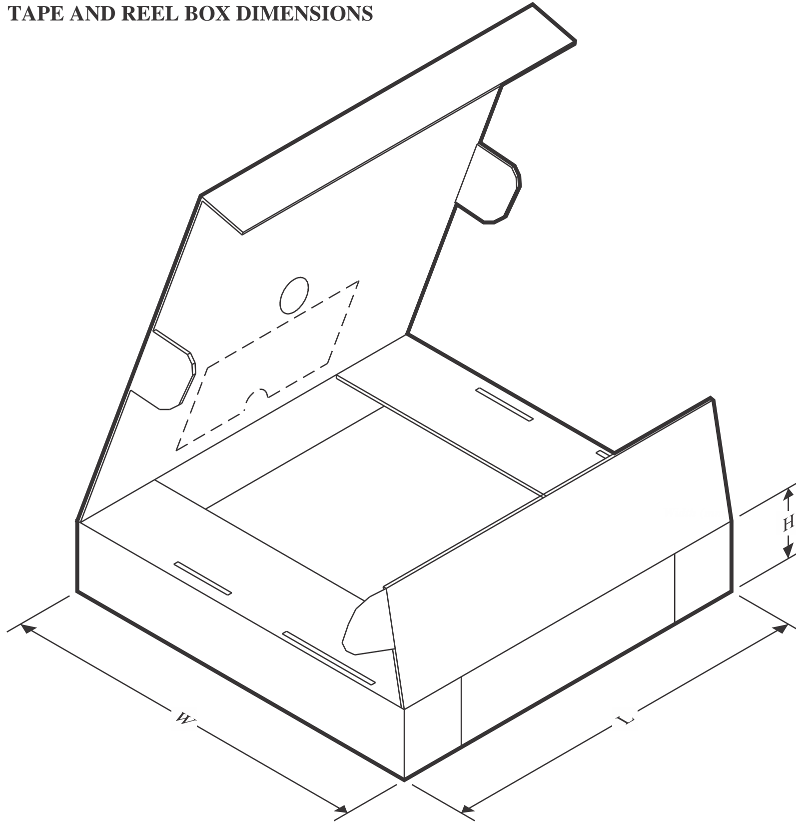




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17318Q2	WSON	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD17318Q2T	WSON	DQK	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17318Q2	WSON	DQK	6	3000	189.0	185.0	36.0
CSD17318Q2T	WSON	DQK	6	250	189.0	185.0	36.0

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