# CSD16401Q5 25V N 沟道 NexFET™ 功率 MOSFET

## 1 特性

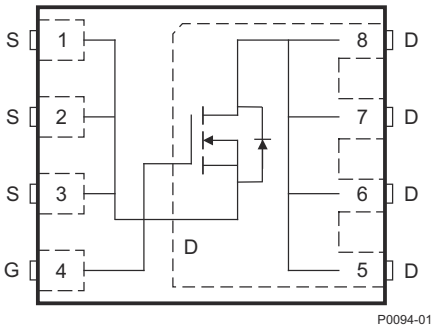
- 超低 $Q_g$ 和 $Q_{gd}$
- 低热阻
- 具有雪崩能力
- SON 5mm × 6mm 塑料封装

## 2 应用

- 网络、电信和计算系统应用中的负载点同步降压转换器
- 针对同步 FET 应用进行了优化

## 3 说明

这款 25V、1.3mΩ、5mm × 6mm SON NexFET™ 功率 MOSFET 旨在更大限度减小功率转换应用中的损耗。




顶视图

**产品概要**

| $T_A$ = 25°C | | 值 | | 单位 |
|---|---|---|---|---|
| $V_{DS}$ | 漏源极电压 | 25 | | V |
| $Q_g$ | 总栅极电荷 (4.5V) | 21 | | nC |
| $Q_{gd}$ | 栅极电荷（栅漏极） | 5.2 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS}$ = 4.5V | 1.8 | mΩ |
| | | $V_{GS}$ = 10V | 1.3 | |
| $V_{GS(th)}$ | 阈值电压 | 1.5 | | V |

**器件信息**(1)

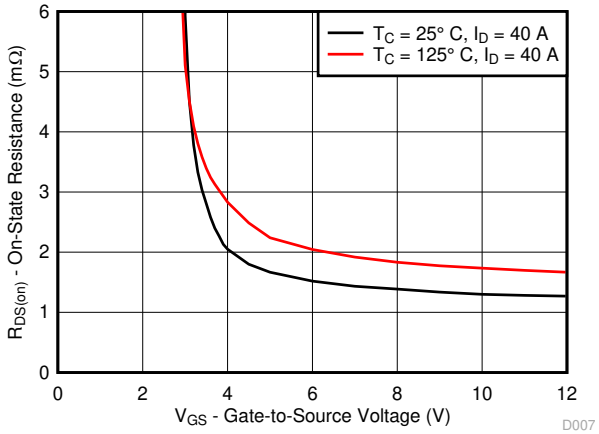
| 器件 | 介质 | 数量 | 封装 | 出货 |
|---|---|---|---|---|
| CSD16401Q5 | 13 英寸卷带 | 2500 | SON 5.00mm × 6.00mm 塑料封装 | 卷带包装 |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

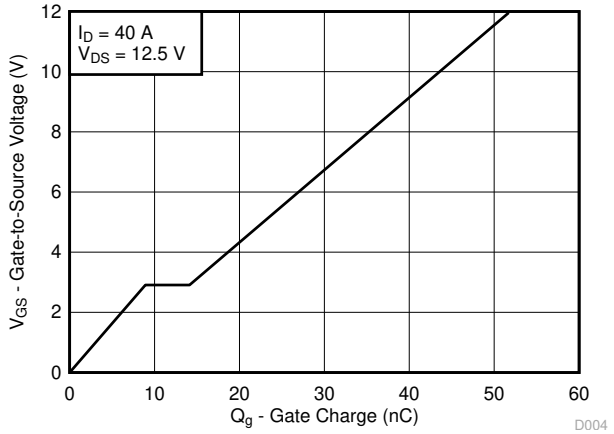
**绝对最大额定值**

| $T_A$ = 25°C | | 值 | 单位 |
|---|---|---|---|
| $V_{DS}$ | 漏源极电压 | 25 | V |
| $V_{GS}$ | 栅源电压 | –12 至 16 | V |
| $I_D$ | 持续漏极电流（受封装限制） | 100 | A) |
| | 持续漏极电流（受器件限制），$T_C$ = 25°C | 261 | |
| | 持续漏极电流(1) | 38 | |
| $I_{DM}$ | 脉冲漏极电流，$T_A$ = 25°C(2) | 240 | A |
| $P_D$ | 功率耗散(1) | 3.1 | W |
| | 功率耗散，$T_C$ = 25°C | 156 | |
| $T_J$，$T_{stg}$ | 工作结温，贮存温度 | –55 至 150 | °C |
| $E_{AS}$ | 雪崩能量，单脉冲 $I_D$ = 100A，L = 0.1mH，$R_G$ = 25Ω | 500 | mJ |

(1) $R_{\theta JA}$ = 40°C/W（在 0.06in (1.52mm) 厚的 FR4 PCB 上安装 1in² (6.45cm²)、2oz (0.071mm) 厚的铜焊盘时）。
(2) 最大 $R_{\theta JC}$ = 0.8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。




$R_{DS(ON)}$与 $V_{GS}$ 间的关系




栅极电荷

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision C (January 2018) to Revision D (October 2023) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |

| Changes from Revision B (August 2015) to Revision C (January 2018) | Page |
|---|---|
| • Added $V_{DS}$ = 5 V to 图 5-3 | 4 |

| Changes from Revision A (September 2010) to Revision B (August 2015) | Page |
|---|---|
| • 向标题添加了器件型号 | 1 |
| • 在 *说明* 部分进行了详述 | 1 |
| • 添加了 *器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 | 1 |
| • 更新了脉冲电流 | 1 |
| • Updated 图 5-1 to a normalized $R_{\theta JC}$ curve | 4 |
| • Updated the SOA in 图 5-10 | 4 |

| Changes from Revision * (August 2009) to Revision A (September 2010) | Page |
|---|---|
| • 删除了“特性”列表中的环境要点 | 1 |


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# 5 Specifications

## 5.1 Electrical Characteristics

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 25 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = –12 V to 16 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.2 | 1.5 | 1.9 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 4.5 V, $I_D$ = 40 A | | 1.8 | 2.3 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 40 A | | 1.3 | 1.6 | |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15 V, $I_D$ = 40 A | | 168 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 12.5 V, $f$ = 1 MHz | | 3150 | 4100 | pF |
| $C_{OSS}$ | Output capacitance | | | 2530 | 3300 | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 175 | 230 | pF |
| $R_g$ | Series gate resistance | | | 1.2 | 2.4 | Ω |
| $Q_g$ | Gate charge total (4.5 V) | $V_{DS}$ = 12.5 V, ID = 40 A | | 21 | 29 | nC |
| $Q_{gd}$ | Gate charge, gate-to-drain | | | 5.2 | | nC |
| $Q_{gs}$ | Gate charge, gate-to-source | | | 8.3 | | nC |
| Qg(th) | Gate charge at Vth | | | 4.8 | | nC |
| $Q_{OSS}$ | Output charge | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | | 55 | | nC |
| $t_{d(on)}$ | Turnon delay time | $V_{DS}$ = 12.5 V, $V_{GS}$ = 4.5 V, $I_D$ = 40 A<br>$R_G$ = 2 Ω | | 16.6 | | ns |
| $t_r$ | Rise time | | | 30 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 20 | | ns |
| $t_f$ | Fall time | | | 12.7 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_S$ = 40 A, $V_{GS}$ = 0 V | | 0.85 | 1 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DD}$ = 15 V, $I_F$ = 40 A, di/dt = 300 A/µs | | 72 | | nC |
| $t_{rr}$ | Reverse recovery time | $V_{DD}$ = 15 V, $I_F$ = 40 A, di/dt = 300 A/µs | | 45 | | ns |

## 5.2 Thermal Information

$T_A$ = 25°C (unless otherwise noted)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal resistance, junction-to-case(1) | | | 0.8 | °C/W |
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient(1) (2) | | | 50 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in (2.54-cm) square, 2-oz(0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 $in^2$ (6.45 $cm^2$) of 2-oz (0.071-mm) thick Cu.

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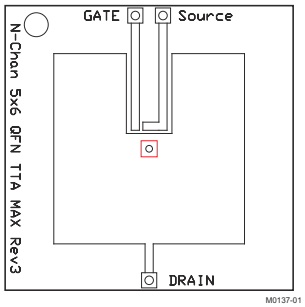
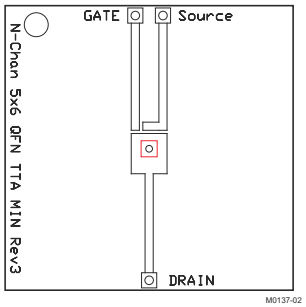



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 $in^2$ (6.45 $cm^2$) of 2-oz (0.071-mm) thick Cu.




Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C (unless otherwise noted)

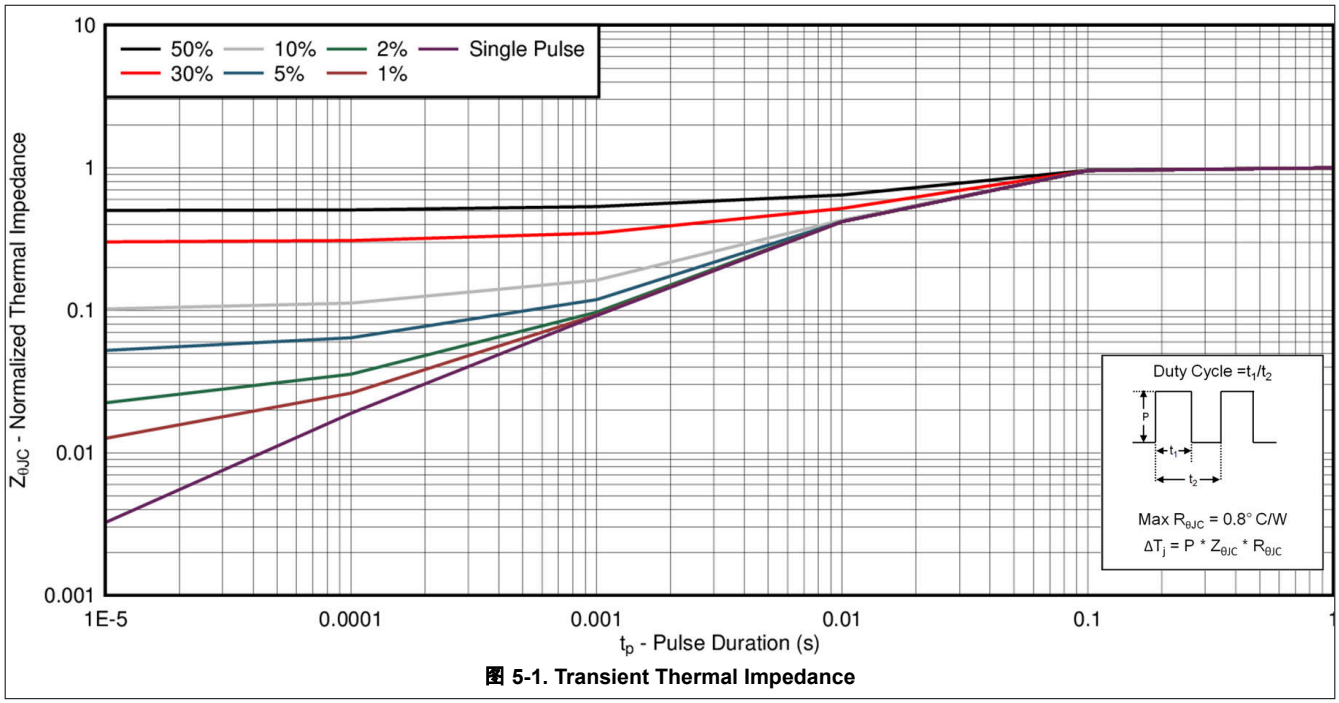



**图 5-1. Transient Thermal Impedance**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## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C (unless otherwise noted)

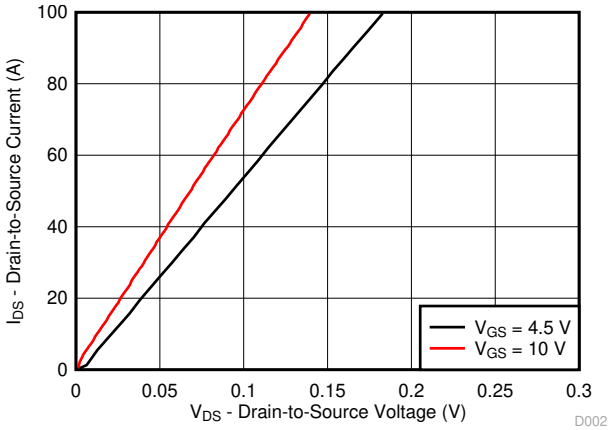
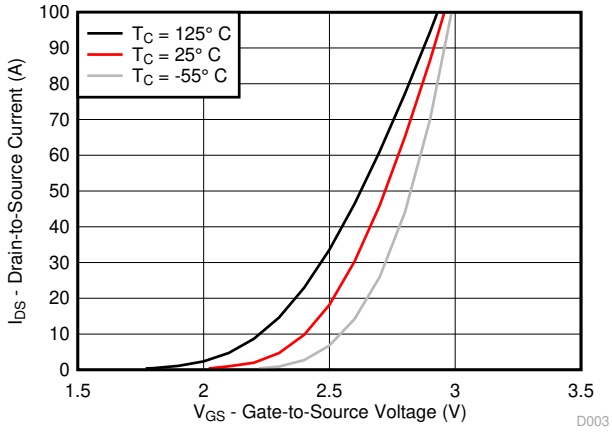
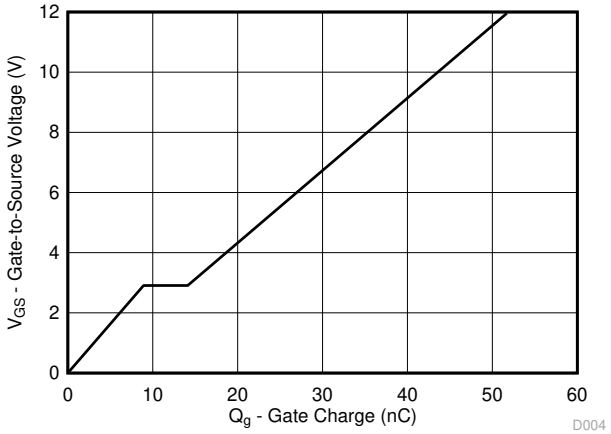



**图 5-2. Saturation Characteristics**




$V_{DS}$ = 5 V

**图 5-3. Transfer Characteristics**




$I_D$ = 40 A $V_{DS}$ = 12.5 V

**图 5-4. Gate Charge**

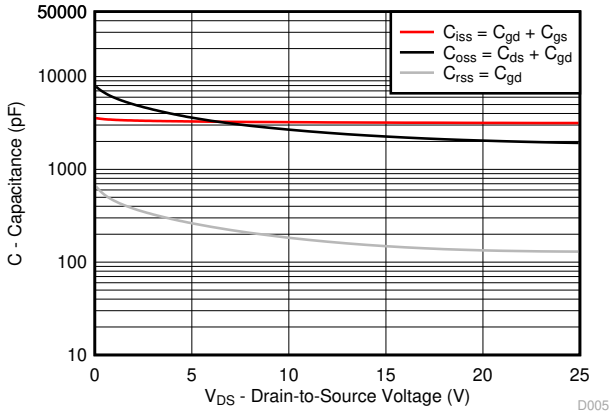
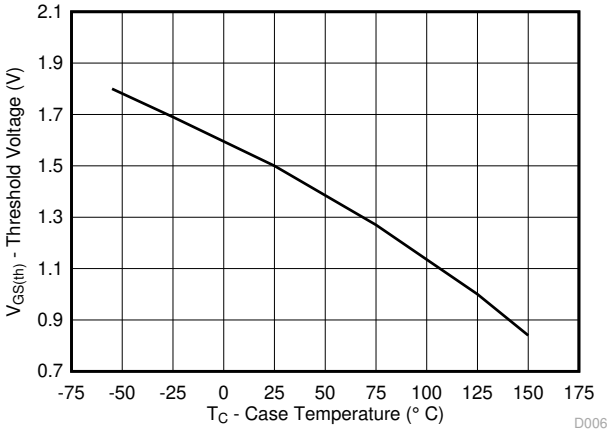



**图 5-5. Capacitance**




$I_D$ = 250 µA

**图 5-6. Threshold Voltage vs Temperature**

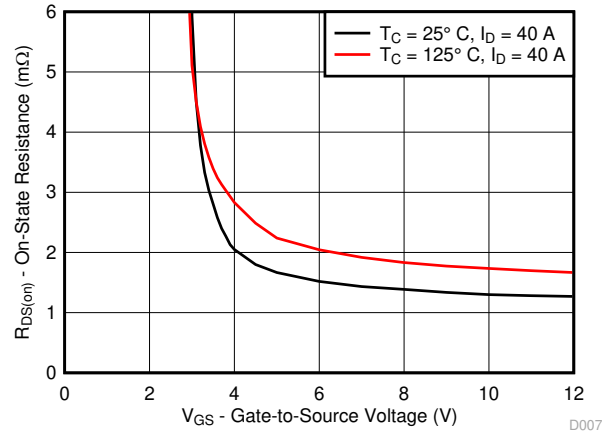



**图 5-7. On-Resistance vs Gate Voltage**

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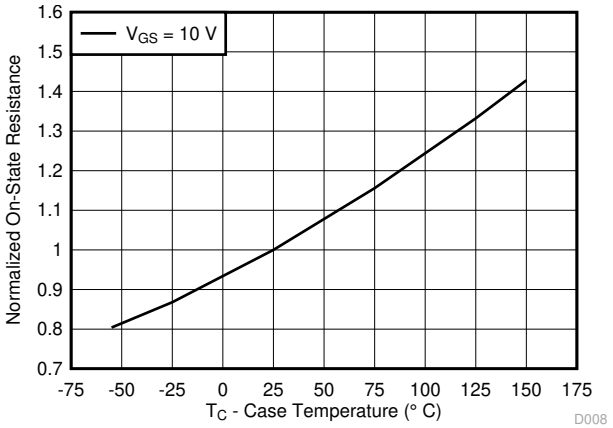
## 5.3 Typical MOSFET Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)




$I_D$ = 40 A

**图 5-8. On-Resistance vs Temperature**

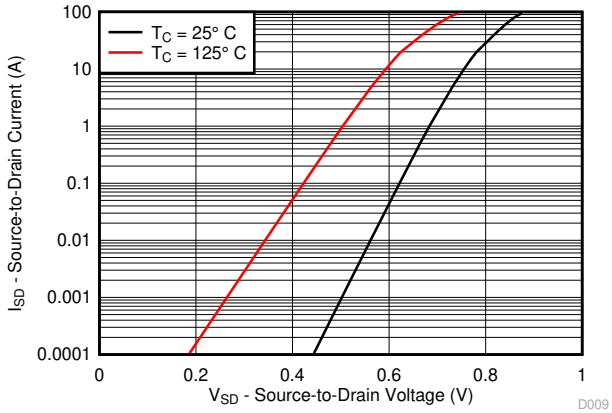
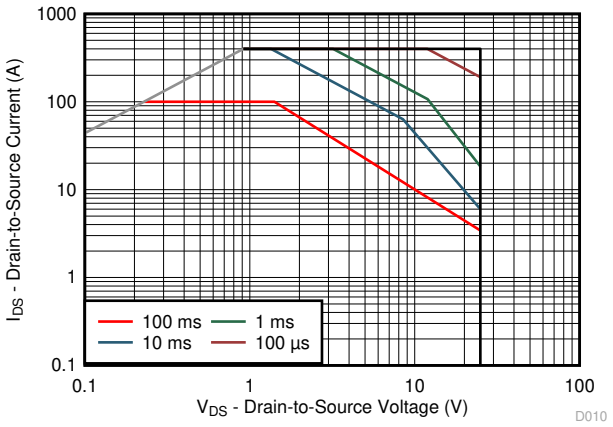



**图 5-9. Typical Diode Forward Voltage**




Single pulse, max $R_{\theta JC}$ = 0.8°C/W

**图 5-10. Maximum Safe Operating Area**

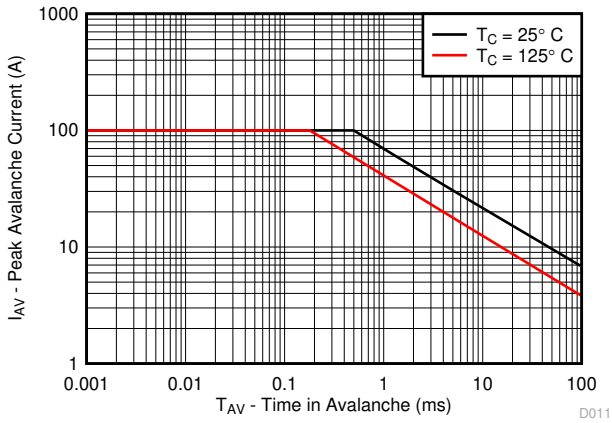



**图 5-11. Single-Pulse Unclamped Inductive Switching**

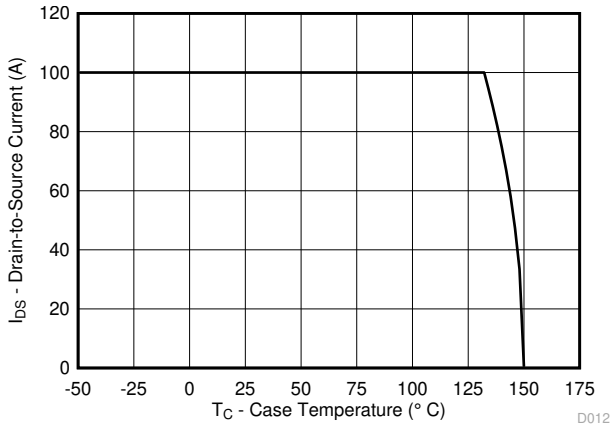



**图 5-12. Maximum Drain Current vs Temperature**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# 6 Device and Documentation Support

## 6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 6.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 6.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CSD16401Q5 | Active | Production | VSON-CLIP (DQH) \| 8 | 2500 \| LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16401 |
| CSD16401Q5.Z | Active | Production | VSON-CLIP (DQH) \| 8 | 2500 \| LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16401 |
| CSD16401Q5T | Active | Production | VSON-CLIP (DQH) \| 8 | 250 \| SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16401 |
| CSD16401Q5T.Z | Active | Production | VSON-CLIP (DQH) \| 8 | 250 \| SMALL T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16401 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

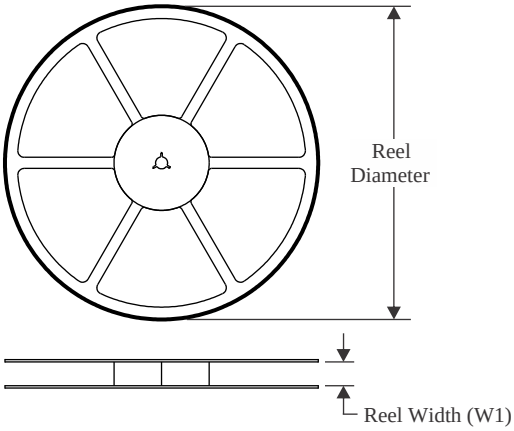
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

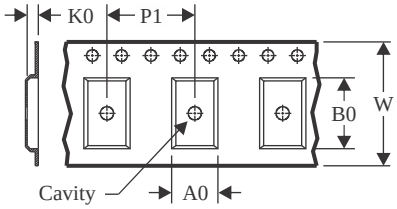
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

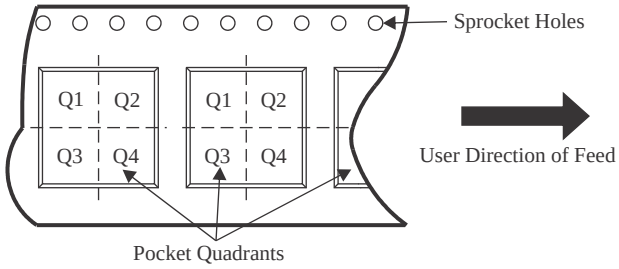



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

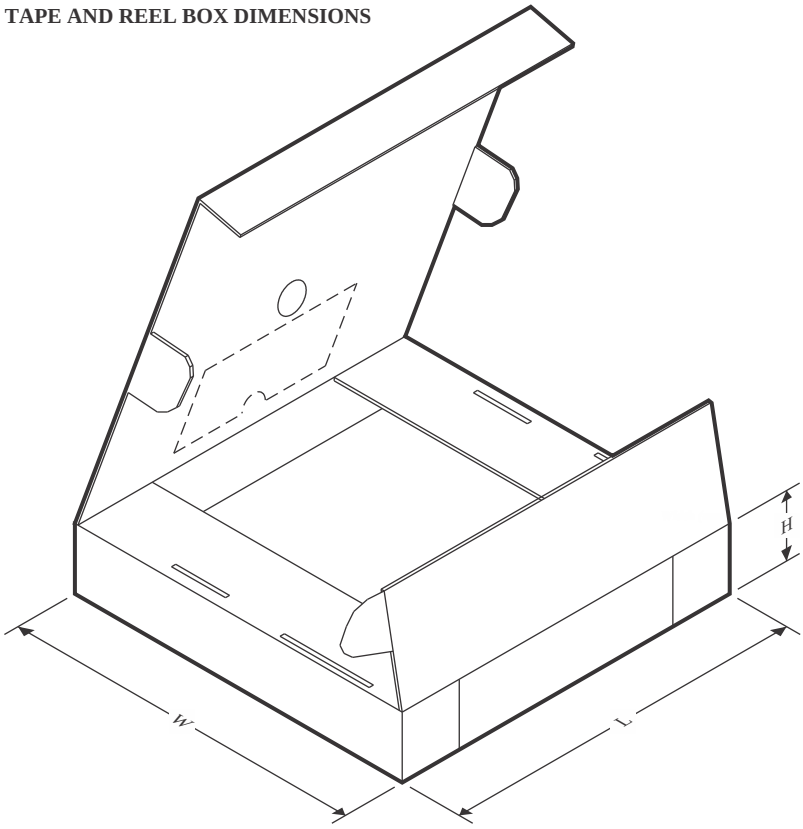
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD16401Q5T | VSON-CLIP | DQH | 8 | 250 | 178.0 | 12.4 | 6.3 | 5.3 | 1.2 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

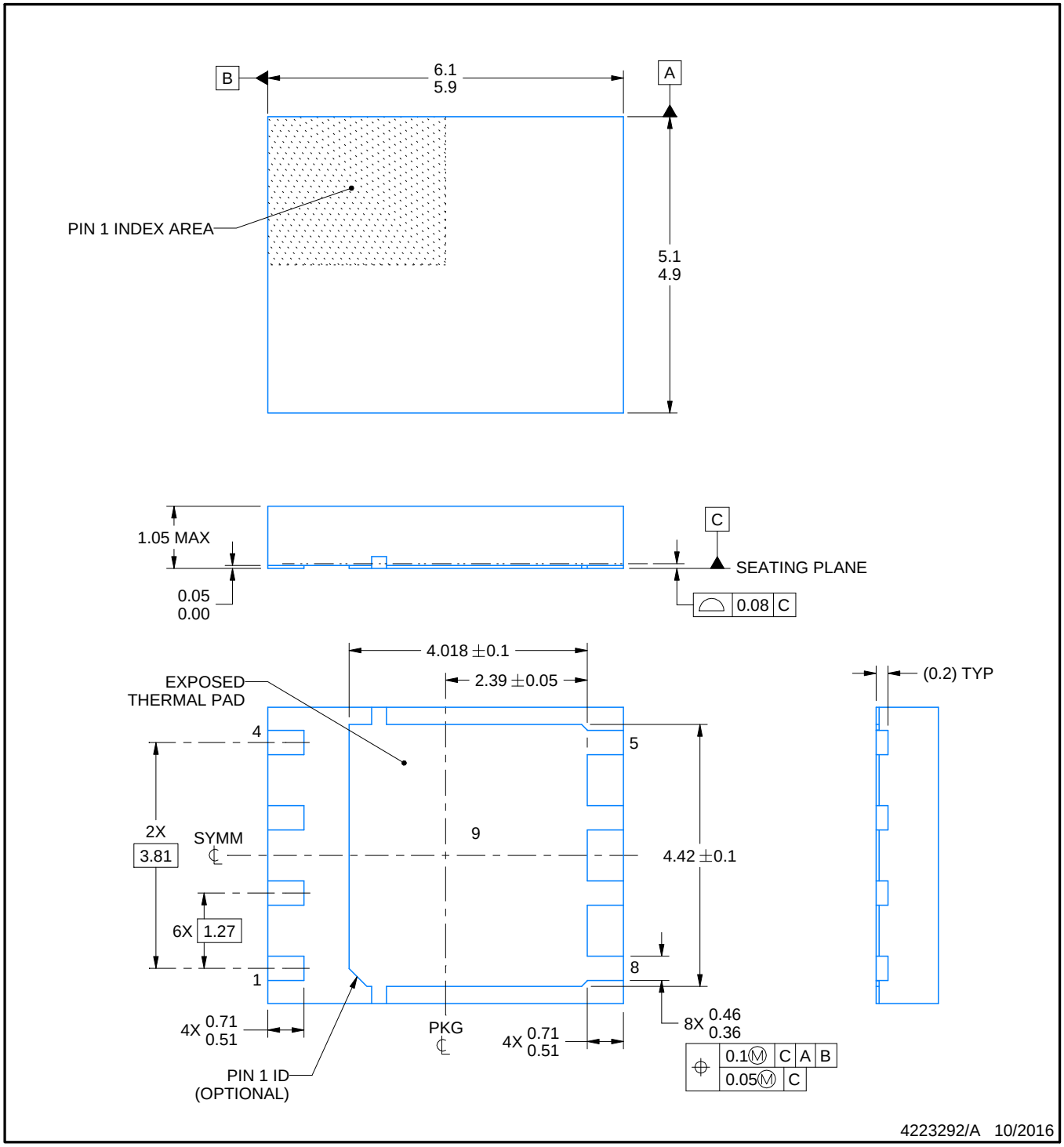
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD16401Q5T | VSON-CLIP | DQH | 8 | 250 | 180.0 | 180.0 | 79.0 |

# PACKAGE OUTLINE

## DQH0008A

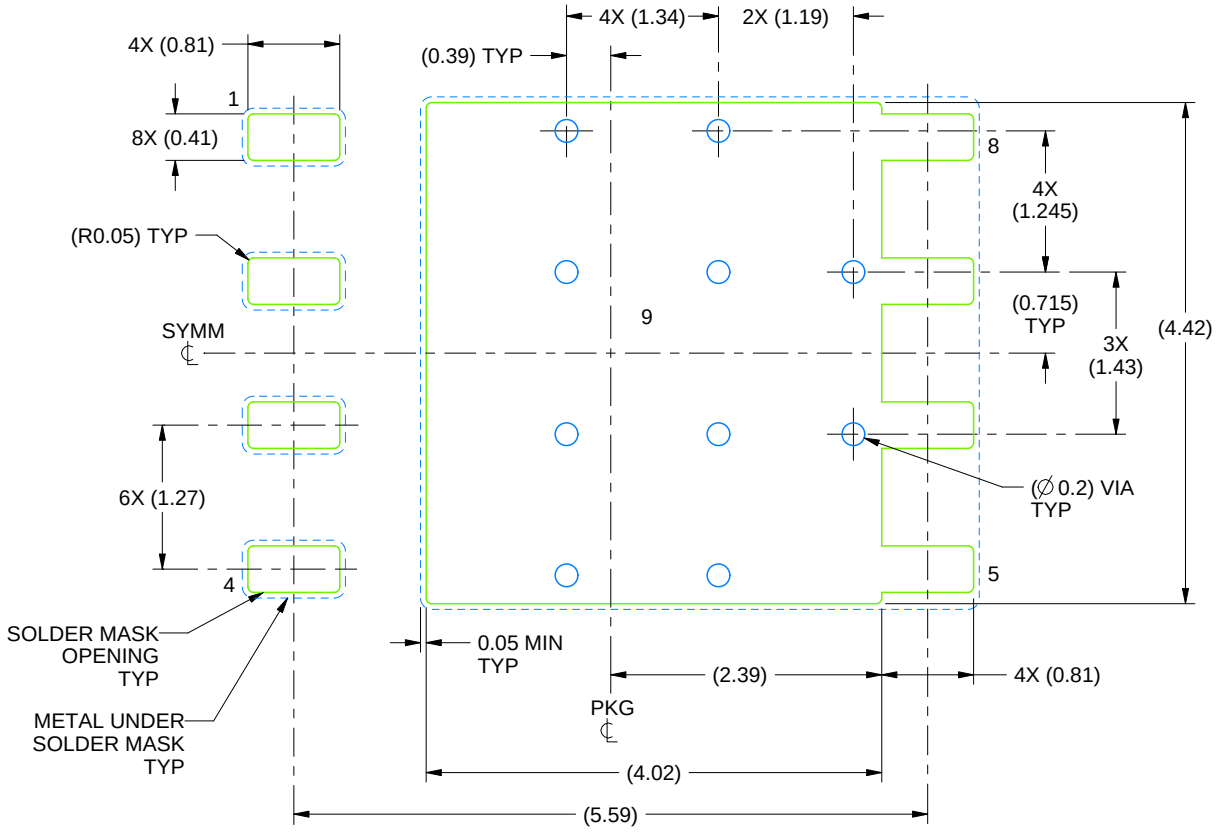
## VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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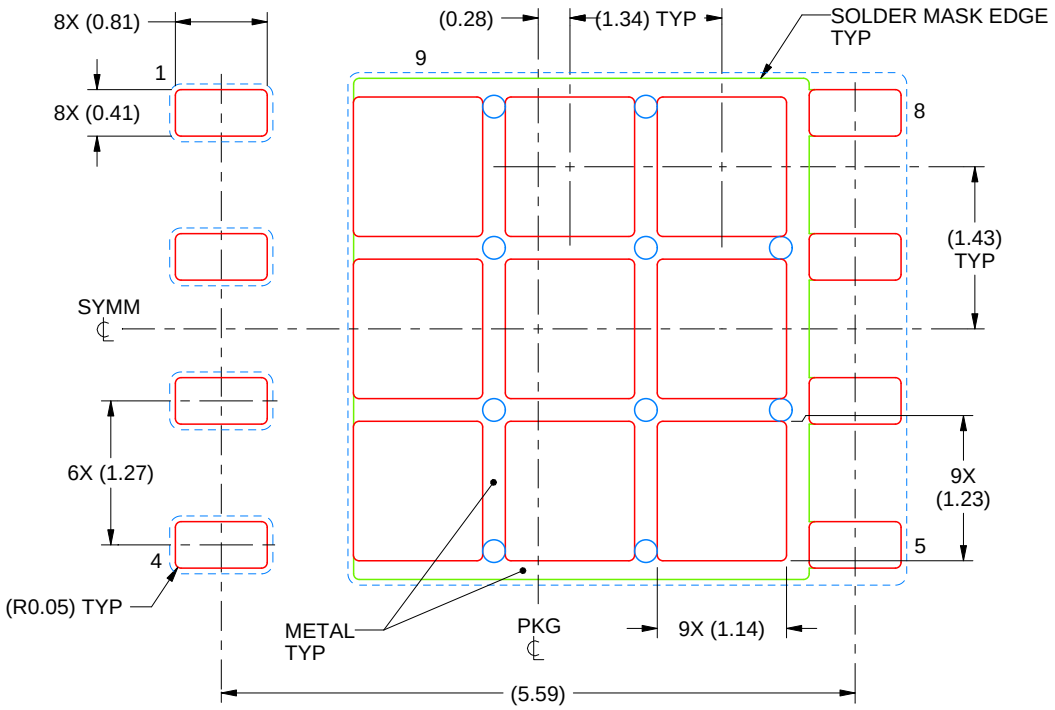
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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