CSD16301Q2 25V N 沟道 NexFET™ 功率 MOSFET

1 特性

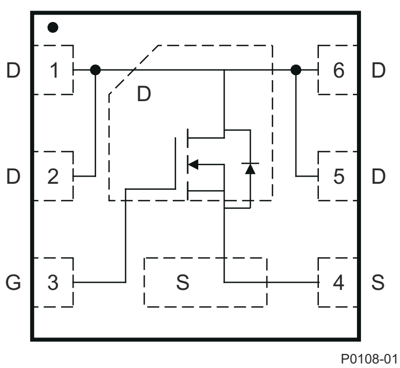
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- SON 2mm × 2mm 塑料封装

2 应用

- 直流/直流转换器
- 电池和负载管理应用

3 说明

该 25V 19mΩ 2mm x 2mm SON NexFET™ 功率 MOSFET 可以极大地降低电源转换和负载管理应用中的损耗。2mm × 2mm SON 封装可提供相对于封装尺寸而言出色的热性能。



顶视图

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	25		V
Q_g	栅极电荷总量 (4.5V)	2		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.4		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 3V	27	mΩ
		V_{GS} = 4.5V	23	
		V_{GS} = 8V	19	
$V_{GS(th)}$	阈值电压	1.1		V

器件信息

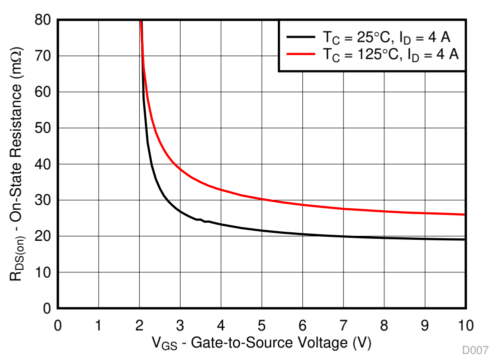
器件	数量	介质	封装[(1)]	运输
CSD16301Q2	3000	7 英寸卷带	SON 2.00mm × 2.00mm 塑料封装	卷带

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

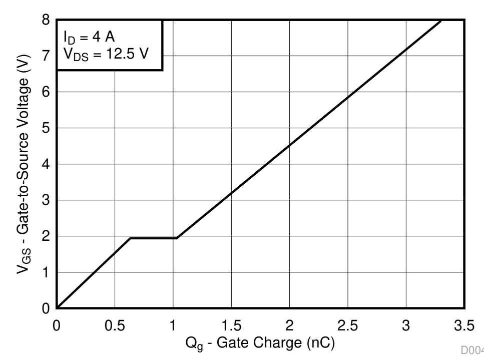
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	25	V
V_{GS}	栅源电压	+10/-8	V
I_D	持续漏极电流（受封装限制）	5	A
	持续漏极电流（受器件限制），T_C = 25°C 时测得	20	
	持续漏极电流[(1)]	8.2	
I_{DM}	脉冲漏极电流[(2)]	85	A
P_D	功率耗散[(1)]	2.5	W
	功率耗散，T_C = 25°C	15	
T_J，T_{STG}	工作结温，贮存温度	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 14A，L = 0.1mH，R_G = 25Ω	10	mJ

(1) 0.06 英寸厚 FR4 PCB 上 1 平方英寸、2oz 铜焊盘上的 $R_{\theta JA}$ = 50°C/W（典型值）。
(2) 最大 $R_{\theta JC}$ = 8.4°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

Table of Contents

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise specified)

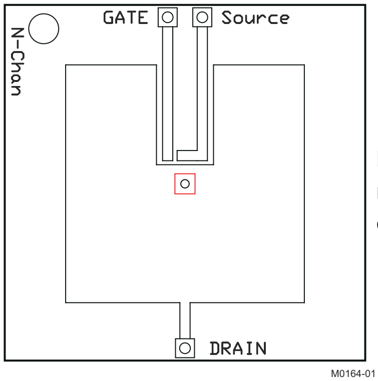
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 20V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = +10/–8V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250μA	0.9	1.1	1.55	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3V, I_{DS} = 4A		27	34	mΩ
		V_{GS} = 4.5V, I_{DS} = 4A		23	29	
		V_{GS} = 8V, I_{DS} = 4A		19	24	
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 4A		16.5		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		260	340	pF
C_{OSS}	Output capacitance			165	215	pF
C_{RSS}	Reverse transfer capacitance			13	17	pF
R_g	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 10V, I_{DS} = 4A		2.0	2.8	nC
Q_{gd}	Gate charge gate-to-drain			0.4		nC
Q_{gs}	Gate charge gate-to-source			0.6		nC
Qg(th)	Gate charge at Vth			0.3		nC
Q_{OSS}	Output charge	V_{DS} = 12.5V, V_{GS} = 0V		3.0		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_{DS} = 4A R_G = 2Ω		2.7		ns
t_r	Rise time			4.4		ns
$t_{d(off)}$	Turnoff delay time			4.1		ns
t_f	Fall time			1.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 4A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 12.5V, I_F = 4A, di/dt = 200A/μs		5.1		nC
t_{rr}	Reverse recovery time			11		ns

4.2 Thermal Information

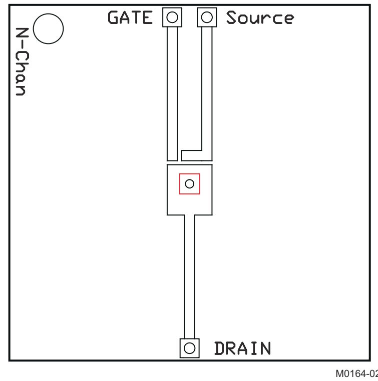
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance[(1)]			8.4	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance[(1) (2)]			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 65°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on minimum pad area of 2oz (0.071mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise specified)

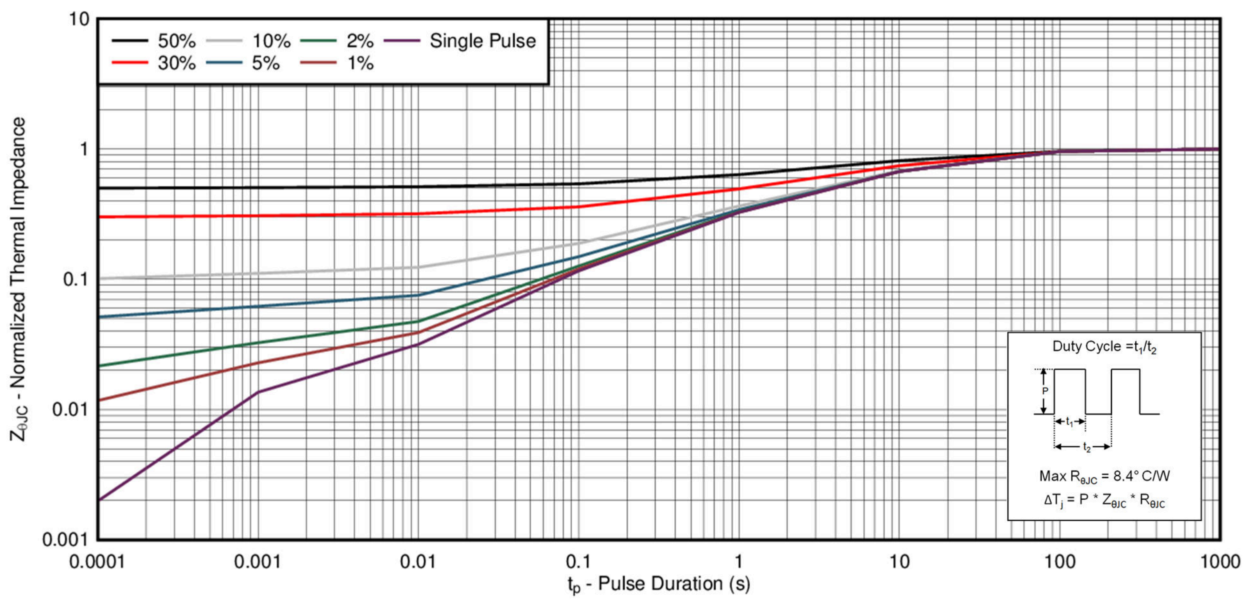


图 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise specified)

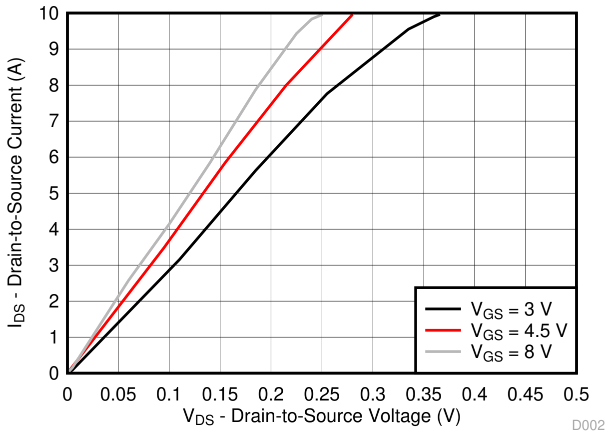
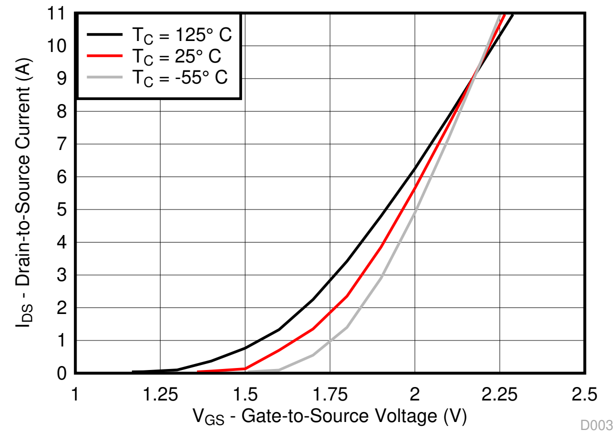
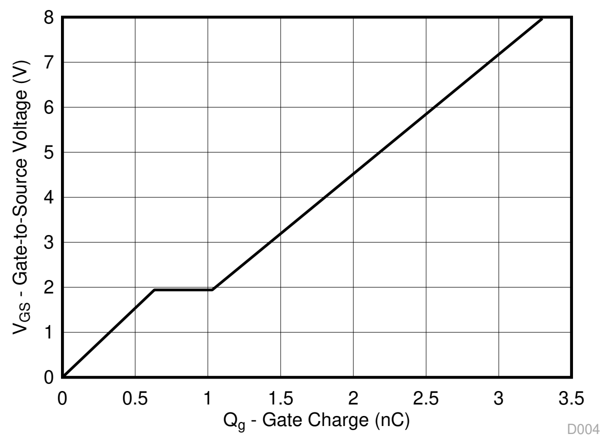


图 **4-2. Saturation Characteristics**



V_{DS} = 5V

图 **4-3. Transfer Characteristics**



I_D = 4A V_{DS} = 50V

图 **4-4. Gate Charge**

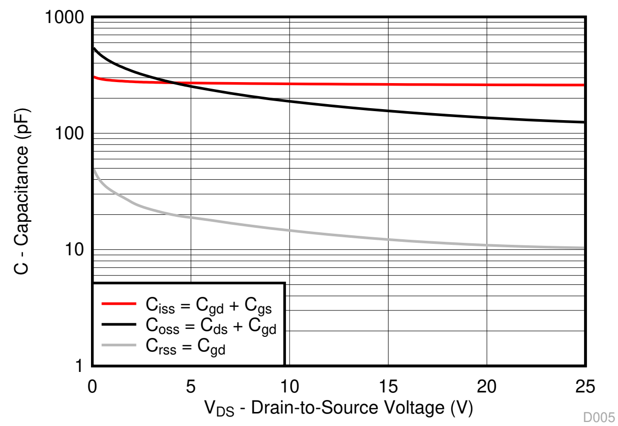
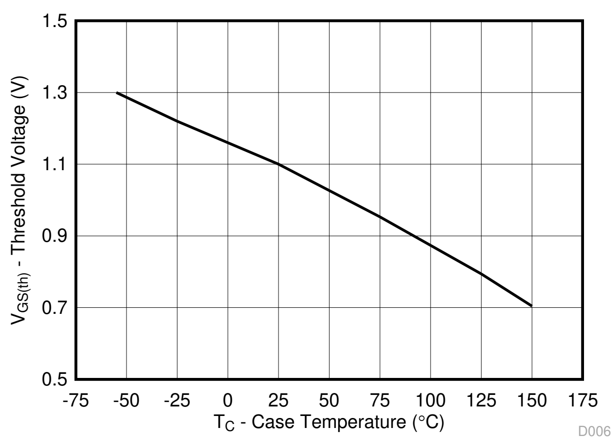


图 **4-5. Capacitance**



I_D = 250µA

图 **4-6. Threshold Voltage vs Temperature**

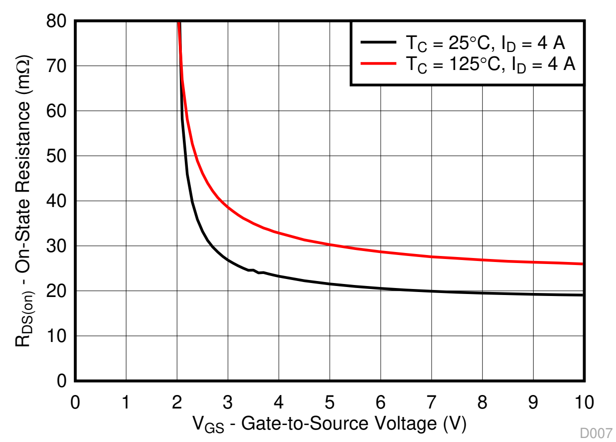
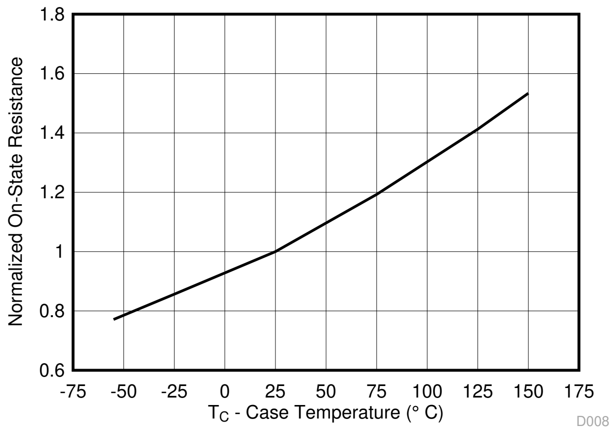


图 **4-7. On-State Resistance vs Gate-to-Source Voltage**

4.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise specified)



V_{GS} = 4.5V I_D = 4A

图 4-8. Normalized On-State Resistance vs Temperature

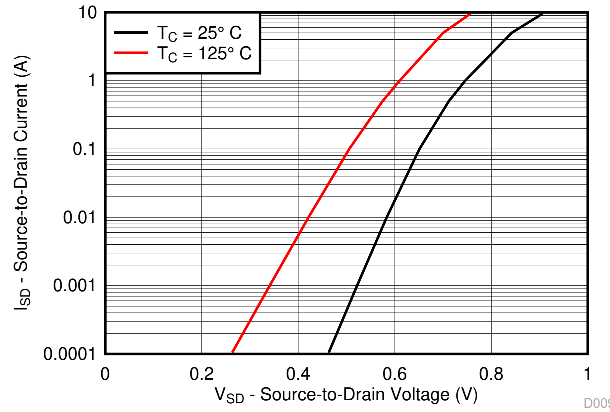
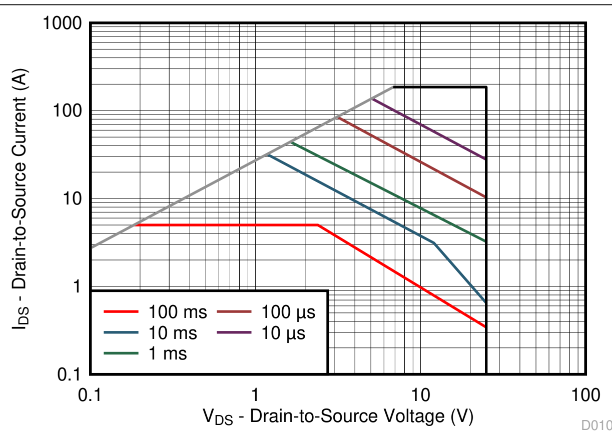


图 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 8.4°C/W

图 4-10. Maximum Safe Operating Area

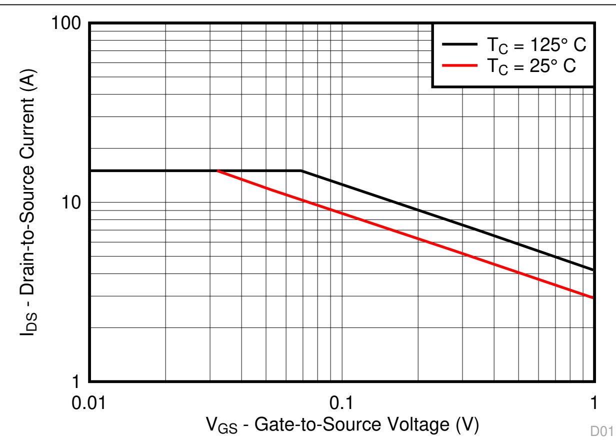


图 4-11. Single Pulse Unclamped Inductive Switching

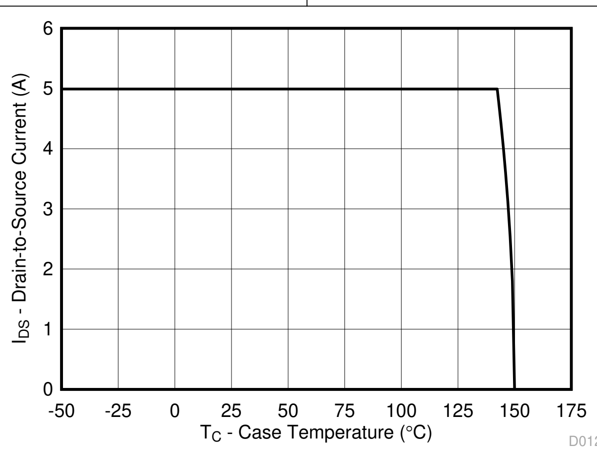


图 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (November 2016) to Revision E (March 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 删除了 CSD16301Q2T 小卷带选项	1

Changes from Revision C (July 2011) to Revision D (November 2016)	Page
• 添加了*器件和文档支持* 部分	1
• 更改了*说明* 文本	1
• 将*产品摘要* 表中的 Q_g 电压条件从 –4.5V 更改为 4.5V	1
• 向*绝对最大额定值* 表中添加了受器件限制的持续漏极电流	1
• 向*绝对最大额定值* 表中添加了 T_C = 25°C 时的最大功率耗散	1
• 更改了*绝对最大额定值* 表中的注释 1 和注释 2	1
• Changed $R_{\theta JA}$ max from 69°C/W : to 65°C/W	3
• Changed 图 4-1 to reflect a transient $R_{\theta JC}$ curve	4
• Changed the safe operating area in 图 4-10 to reflect measured data	4
• Changed *MECHANICAL DATA* section to *Mechanical, Packaging, and Orderable Information* section	9

Changes from Revision B (April 2010) to Revision C (July 2011)	Page
• 在"订购信息"表中添加了 7 英寸卷带选项	1

Changes from Revision A (December 2009) to Revision B (April 2010)	Page
• Added title to 图 4-11 - Single Pulse Unclamped Inductive Switching	4

Changes from Revision * (October 2009) to Revision A (December 2009)	Page
• Changed the Electrical Characteristics table - $V_{GS(th)}$ MAX value From: 1.4V To 1.55V	3

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16301Q2	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1631

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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