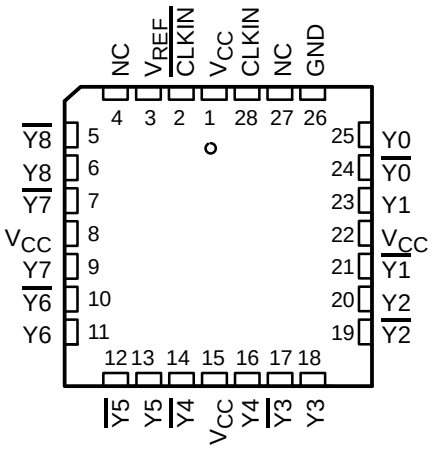
- **Low-Output Skew for Clock-Distribution Applications**
- **Differential Low-Voltage Pseudo-ECL (LVPECL) Compatible Inputs and Outputs**
- **Distributes Differential Clock Inputs to Nine Differential Clock Outputs**
- **Output Reference Voltage (V_{REF}) Allows Distribution From a Single-Ended Clock Input**
- **Packaged In a 28-Pin Plastic Chip Carrier**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The differential LVPECL clock-driver circuit distributes one pair of differential LVPECL clock inputs (CLKIN, $\overline{\text{CLKIN}}$) to nine pairs of differential clock (Y, $\overline{\text{Y}}$) outputs with minimum skew for clock distribution. It is specifically designed for driving 50-Ω transmission lines.

The V_{REF} output can be strapped to the $\overline{\text{CLKIN}}$ input for a single-ended CLKIN input.

The CDCVF111 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUTS	
CLKIN	**$\overline{\text{CLKIN}}$**	**Yn**	**$\overline{\text{Yn}}$**
X	X	L	H
L	H	L	H
H	L	H	L
L	V_{REF}	L	H
H	V_{REF}	H	L
V_{REF}	L	H	L
V_{REF}	H	L	H

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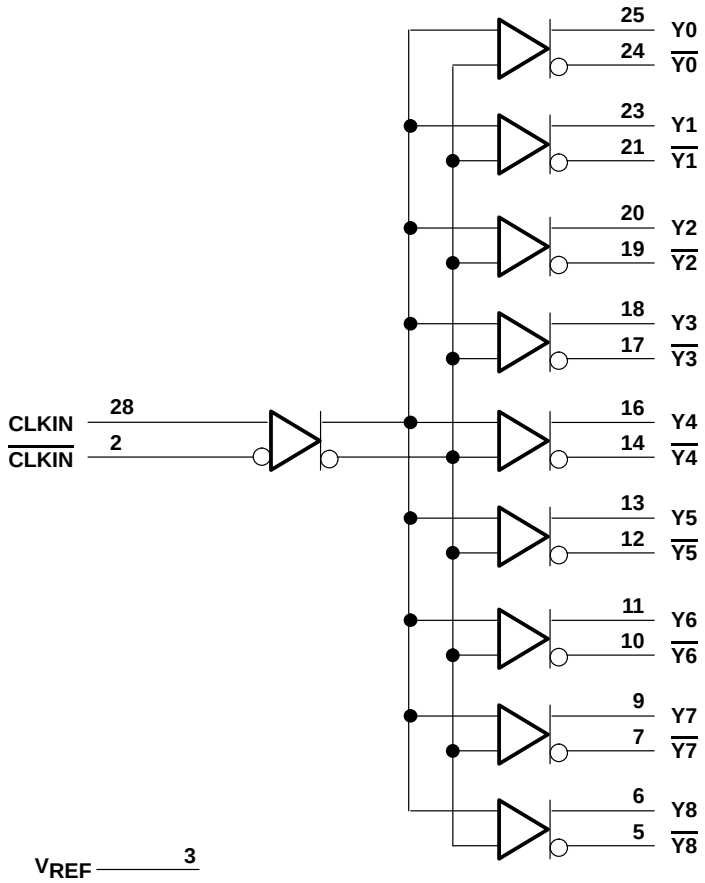
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . –18 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . –50 mA
Continuous current through V_{CC} or GND . . . . . ± 80 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . . 525 mW
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.165	V_{CC}–0.88	V
		V_{CC} = 3.3 V	2.135	2.42	V
V_{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V	V_{CC}–1.81	V_{CC}–1.475	V
		V_{CC} = 3.3 V	1.49	1.825	V
T_A	Operating free-air temperature		–40	85	°C
f_{clock}	Input frequency			650	MHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
V_{REF}	V_{CC} = 3 V to 3.6 V	I_{REF} = 100 µA	V_{CC}–1.38	V_{CC}–1.26	V
	V_{CC} = 3.3 V		1.92	2.04	
V_{OH}	V_{CC} = 3 V to 3.6 V, T_A = 0°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.12	V_{CC}–0.83	V
	V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.15	V_{CC}–0.83	
	V_{CC} = 3.3 V		2.275	2.42	
V_{OL}	V_{CC} = 3 V to 3.6 V T_A = 0°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.86	V_{CC}–1.49	
	V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C, $f_{(max)}$ = 650 MHz		V_{CC}–1.86	V_{CC}–1.52	
	V_{CC} = 3.3 V		1.49	1.68	
I_I	V_I = 2.4 V,	V_{CC} = 3 .6 V		150	µA
I_{CC} (Internal)	I_O = 0,	V_{CC} = 3 .6 V		100	mA

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	CLKIN, $\overline{\text{CLKIN}}$	Y, $\overline{\text{Y}}$	450	600	ps
t_{PHL}					
$t_{sk(o)}$		Y, $\overline{\text{Y}}$		50	ps
$t_{sk(pr)}$		Y, $\overline{\text{Y}}$		150	ps
t_r		Y, $\overline{\text{Y}}$	200	600	ps
t_f					

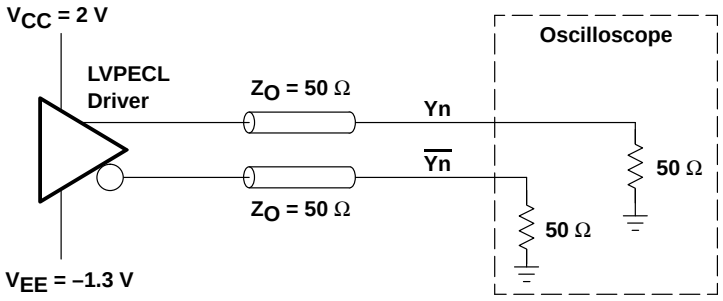
ESD information

ESD MODELS	LIMIT
Human Body Model (HBM)	2.0 kV
Machine Model (MM)	200 V
Charge Device Model (CDM)	2.0 kV

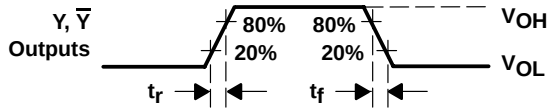
thermal information

CDCVF111 28-PIN PLCC			THERMAL AIR FLOW (CFM)				UNIT
			0	150	250	500	
$R_{\theta JA}$	High K		48	44	42	39	°C/W
$R_{\theta JA}$	Low K		70	58	52	46	°C/W
$R_{\theta JC}$	High K	22					°C/W
$R_{\theta JC}$	Low K	28					°C/W

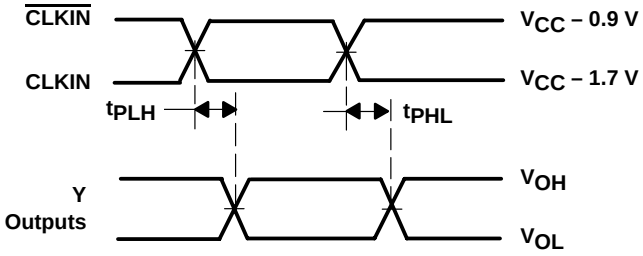
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT (See Note B)



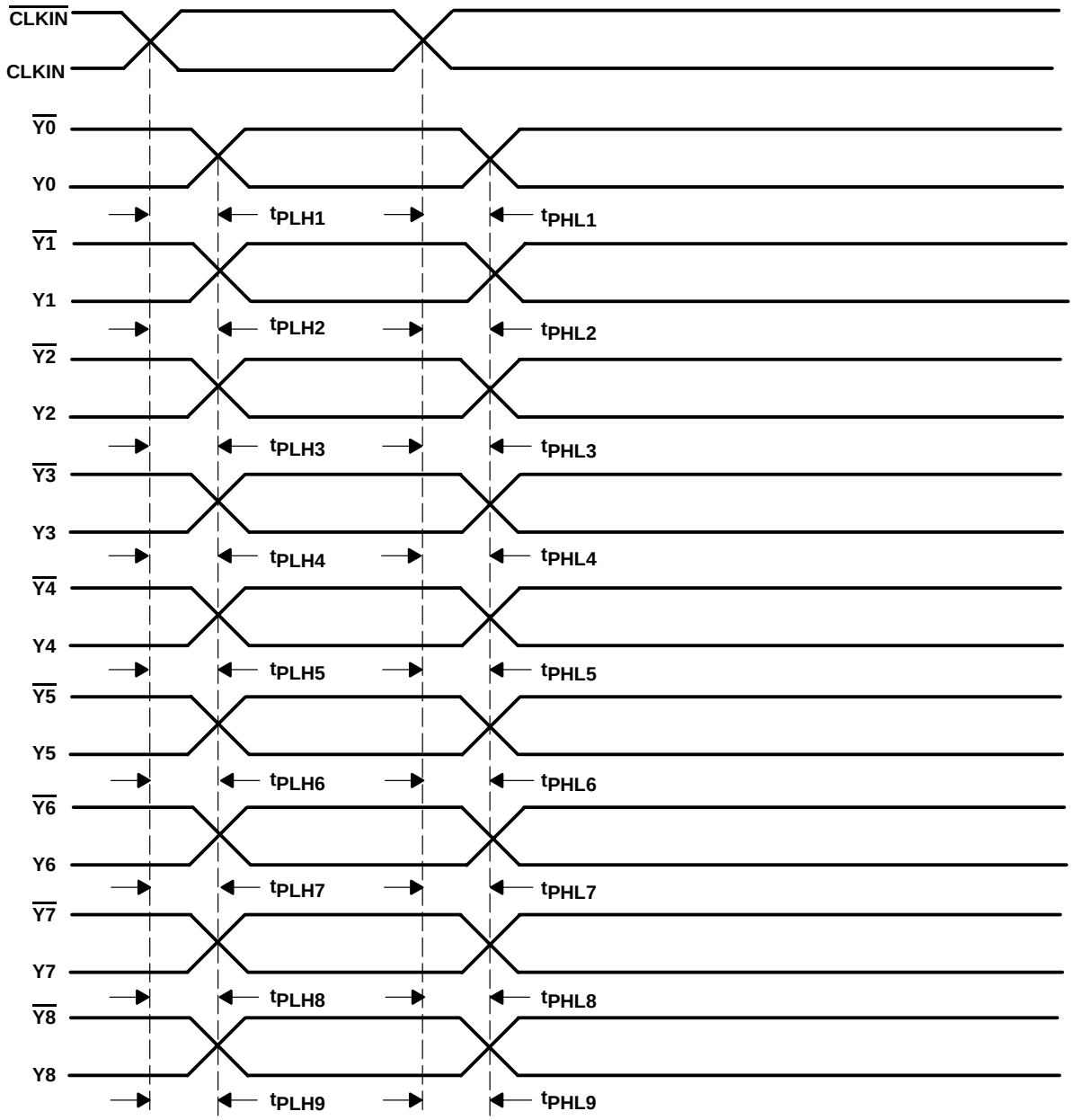
VOLTAGE WAVEFORMS
RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 45 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
B. For additonal signal interface, see the *Interfacing Between LVPECL, LVDS, and CML* application note, Literature Number SCAA056.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest t_{PLHn} (n = 1, 2, . . . 9)
- The difference between the fastest and slowest t_{PHLn} (n = 1, 2, . . . 9) across multiple devices

C. For additional information on skew and propagation delay parameters, see the *Defining Skew, Propagation Delay, Phase-Offset (Phase Error)* application note, literature number SCAA055.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(pr)}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF111FN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI	-40 to 85	CDCVF111	
CDCVF111FNR	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI	-40 to 85	CDCVF111	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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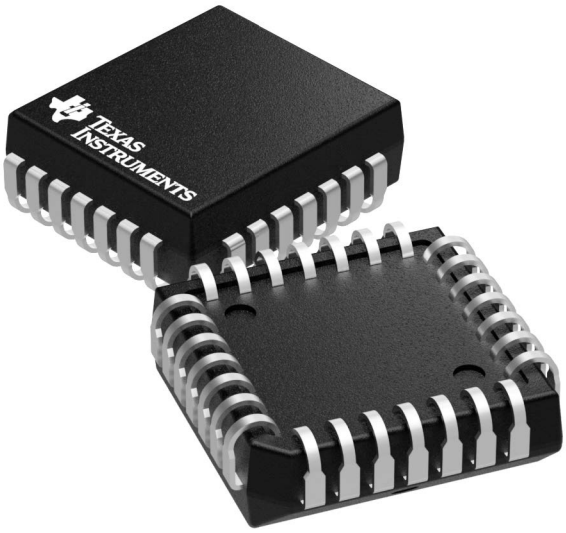
GENERIC PACKAGE VIEW

FN 28

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

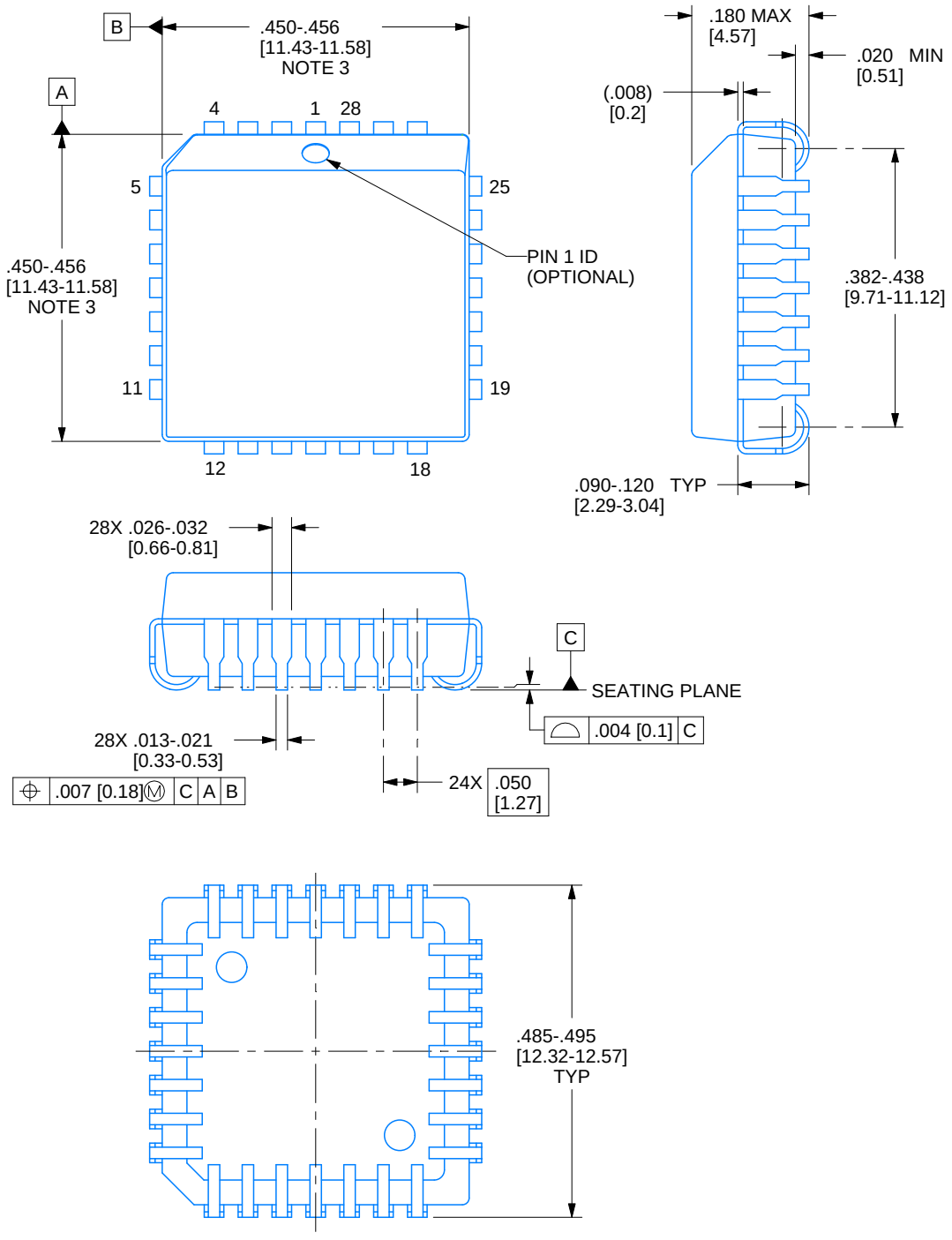
4040005-3/C

PACKAGE OUTLINE

FN0028A

PLCC - 4.57 mm max height

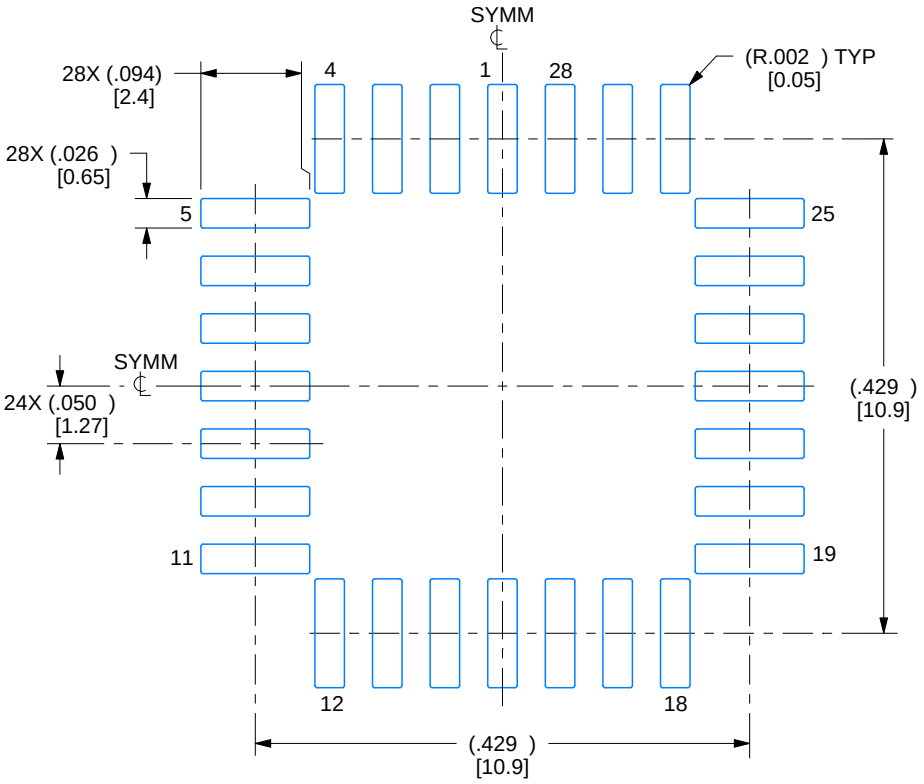
PLASTIC CHIP CARRIER



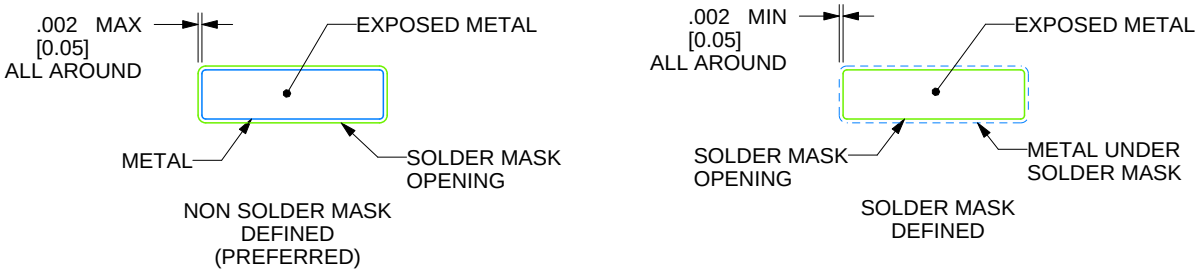
4215153/B 05/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

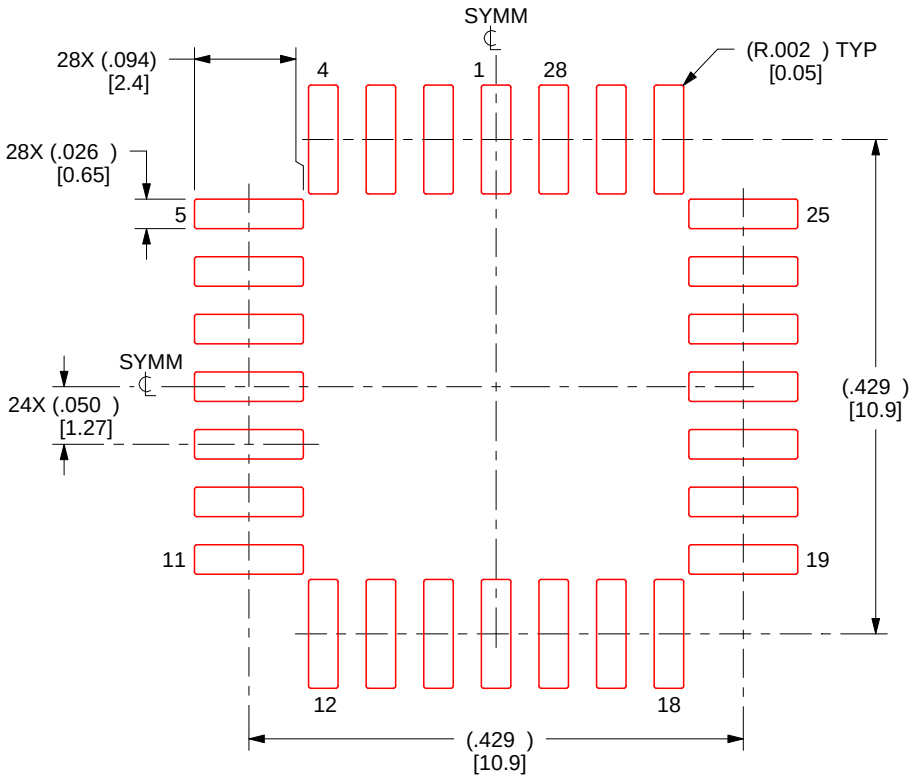


SOLDER MASK DETAILS

4215153/B 05/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215153/B 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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