

## CLOCK MULTIPLIER WITH DELAY CONTROL AND PHASE ALIGNMENT

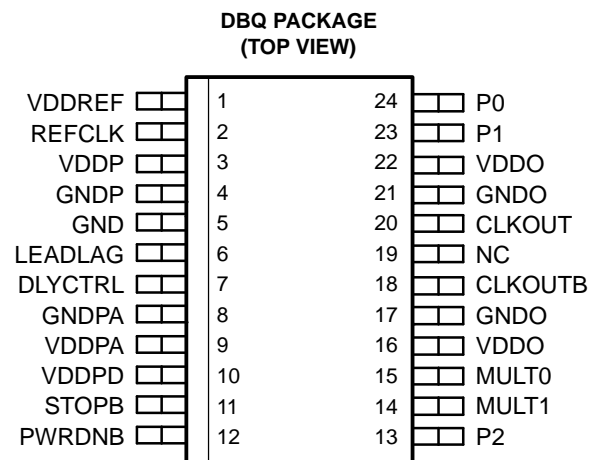
### FEATURES

- Low-Jitter Clock Multiplier: x1, x2, x4, x8
- Fail-Safe Power Up Initialization
- Programmable Bidirectional Delay Steps of 1.3 mUI
- Output Frequency Range of 25 MHz to 280 MHz
- Input Frequency Range of 12.5 MHz to 240 MHz
- Low Jitter Generation
- Single-Ended REFCLK Input With Adjustable Trigger Level (Works With LVTTTL, HSTL, and LVPECL)
- Differential/Single-Ended Output
- Output Can Drive LVPECL, LVDS, and LVTTTL
- Three Power Operating Modes to Minimize Power
- Low Power Consumption (< 190 mW at 280 MHz/3.3 V)
- Packaged in a Shrink Small-Outline Package (DBQ)
- No External Components Required for PLL

- Spread Spectrum Clock Tracking Ability to Reduce EMI (SSC)

### APPLICATIONS

- Video Graphics
- Gaming Products
- Datacom
- Telecom
- Noise Cancellation Created by FPGAs



### DESCRIPTION

The CDCF5801A provides clock multiplication from a reference clock (REFCLK) signal with the unique capability to delay or advance the CLKOUT/CLKOUTB with steps of only 1.3 mUI through a phase aligner. For every rising edge on the DLYCTRL pin the CLKOUT is delayed by a 1.3-mUI step size as long as the LEADLAG input detects a low signal at the time of the DLYCTRL rising edge. Similarly for every rising edge on the DLYCTRL pin the CLKOUT is advanced by a 1.3-mUI step size as long as the LEADLAG pin is high during the transition. This unique capability allows the device to phase align (zero delay) between CLKOUT/CLKOUTB and any one other CLK in the system by feeding the clocks that need to be aligned to the DLYCTRL and the LEADLAG pins. Also it provides the capability to program a fixed delay by providing the proper number of edges on the DLYCTRL pin, while strapping the LEADLAG pin to dc high or low. Further possible applications are:

- Aligning the rising edge of the output clock signal to the input clock rising edge
- Avoiding PLL instability in applications that require very long PLL feedback lines
- Isolation of jitter and digital switching noise
- Limitation of jitter in systems with good ppm frequency stability

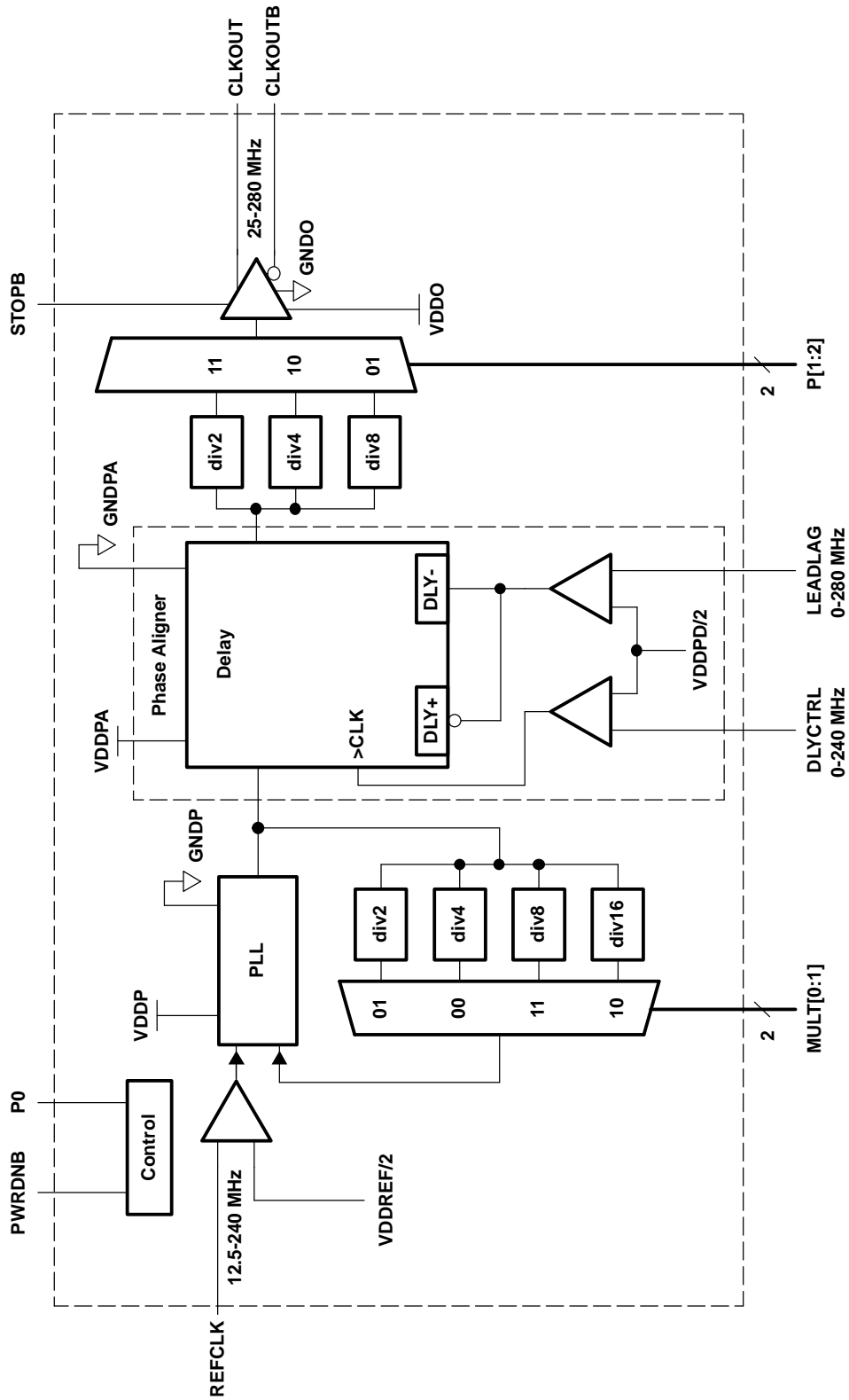
The CDCF5801A has a fail-safe power up initialization state-machine which supports proper operation under all power up conditions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The CDCF5801A provides clock multiplication and division from a reference clock (REFCLK) signal. The device is optimized to have extremely low jitter impact from input to output. The predivider pins MULT[0:1] and post-divider pins P[0:2] provide selection for frequency multiplication and division ratios, generating CLKOUT/CLOUTKB frequencies ranging from 25 MHz to 280 MHz with clock input references (REFCLK) ranging from 12.5 MHz to 240 MHz. See [Table 1](#) for detailed frequency support. The selection of pins MULT[0:1] and P[1:2] determines the multiplication value of 1, 2, 4, or 8. The CDCF5801A offers several power-down/high-impedance modes, selectable by pins P0, STOPB and PWRDN. Another unique capability of the CDCF5801A is the high sensitivity and wide common-mode range of the clock-input pin REFCLK by varying the voltage on the VDDREF pin. The clock signal outputs CLKOUT and CLKOUTB can be used independently to generate single-ended clock signals. The CLKOUT/CLKOUTB outputs can also be combined to generate a differential output signal suitable for LVDS, LVPECL, or HSTL/SSTL signaling. The CDCF5801A is characterized for operation over free-air temperatures of -40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLKOUT CLKOUTB	2018	O	Output CLK signal (low-noise CMOS) Complementary output CLK signal (low-noise CMOS)
DLYCTRL	7	I	Every rising edge on this pin delays/advances the CLKOUT/CLKOUTB signal by 1/768 <sup>th</sup> of the CLKOUT/CLKOUTB period (1.3 mUI). (E.g., for a 90-degree delay or advancement one needs to provide 192 rising edges). See <a href="#">Table 3</a> .
GND	5		GND for VDDREF and VDDPD
GNDO	17, 21		GND for the output pins (CLKOUT, CLKOUTB)
GNDP	4		GND for the PLL
GNDPA	8		GND for phase aligner, digital logic, and inputs P[0:2], MULT[0:1], STOPB, PWRDNB
LEADLAG	6	I	Controls whether the output CLK is delayed or advanced relative to REFCLK. See <a href="#">Table 3</a> .
MULT0 MULT1	15 14	I	PLL multiplication factor select. See <a href="#">Table 1</a> . MULT[0:1] = 10: x16 MULT[0:1] = 11: x8 MULT[0:1] = 00: x4 MULT[0:1] = 01: x2
NC	19		Not connected; leave pin floating or tied to GND.
P0	24	I	Mode control pins (see <a href="#">Table 1</a> ) 0 - Normal operation 1 - High-Z outputs and other special settings
P1  P2	23  13	I	Post divider control (see <a href="#">Table 1</a> ) P[1:2] = 11: div2 P[1:2] = 10: div4 P[1:2] = 01: div8
PWRDNB	12	I	Active-low power-down state. CLKOUT/CLKOUTB goes low, See <a href="#">Table 2</a> . 0 - IC in power down 1 - Normal operation
REFCLK	2	I	Reference input clock
STOPB	11	I	Active low output disabler, PLL and PA still running, CLKOUT and CLKOUTB goes to a dc value as listed in <a href="#">Table 2</a> . 0 - Outputs disabled 1 - Normal operation
VDDO	16, 22		VDD for the output pin (CLKOUT, CLKOUTB) and power down circuit
VDDP	3		VDD for PLL and input buffer
VDDPA	9		VDD for phase aligner, digital logic, and inputs P[0:2], MULT[0:1], and STOPB
VDDPD	10		Reference voltage for inputs LEADLAG and DLYCTRL
VDDREF	1		Reference voltage for REFCLK

**Table 1. Input-to-Output Settings**

INPUT-TO-OUTPUT MULTIPLICATION-RATIO	INPUT FREQUENCY (MHz)		OUTPUT FREQUENCY (MHz)		PREDIVIDER		POST DIVIDER			NOTE
	FROM	TO	FROM	TO	MULT0	MULT1	P0	P1	P2	
8	12.5	35	100	280	1	0	0	1	1	Normal operation <sup>(1)</sup>
4	12.5	39	50	156	1	0		1	0	
	25	70	100	280	1	1		1	1	
2	12.5	39	25	78	1	0		0	1	
	25	78	50	156	1	1		1	0	
	50	140	100	280	0	0		1	1	
1	25	78	25	78	1	1		0	1	
	50	156	50	156	0	0		1	0	
	100	240	100	240	0	1		1	1	
CLKOUT high-impedance					X	X	1	0	0	Special mode of operation
CLOUTB high-impedance										
CLKOUT = high					X	X		0	1	
CLKOUTB = high								1	X	
CLKOUT = P2					X	X				
CLKOUTB = P2										

(1) There is some overlapping of the input frequency ranges for multiplication ratios of 1, 2, and 4. For example, an input frequency of 30 MHz for a multiplication ratio of four falls within both the 12.5 to 39-MHz range and the 25 to 70-MHz range. For best device operation in a case such as this, always select the input frequency range nearer to the top of the table.

## PLL DIVIDER/MULTIPLIER SELECTION

**Table 2. Power Down Modes**

STATE	PWRDNB	STOPB	CLKOUT and CLKOUTB
Power down	0	X	GNDO
Clock stop	1	0	V <sub>O</sub> , STOP
Normal	1	1	See <a href="#">Table 1</a>

**Table 3. Programmable Delay and Phase Alignment**

DLYCTR	NOTE	LEADLAG	CLKOUT and CLKOUTB
Each rising edge+	For every 32 edges, there are one or two edges for which the phase aligner does not update the phase. Therefore, CLKOUT phase is not updated for every 32 <sup>nd</sup> edge. The frequency of the DLYCTRL pin should always be equal to or less than the frequency of the LEADLAG pin.	HI	Advanced by one step: step size: 1/768 of the CLKOUT period (1.3 mUI) at P[1:2] = 11 1/1536 of the CLKOUT period (0.65 mUI) at P[1:2] = 10 1/3072 of the CLKOUT period (0.325 mUI) at P[1:2] = 01
Each rising edge+		LO	Delayed by one step: step size: 1/768 of the CLKOUT period (1.3 mUI) at P[1:2] = 11 1/1536 of the CLKOUT period (0.65 mUI) at P[1:2] = 10 1/3072 of the CLKOUT period (0.325 mUI) at P[1:2] = 01

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

$V_{DDx}$ <sup>(2)</sup>	Supply voltage range	-0.5 V to 4 V
	Voltage range at any output terminal	-0.5 V to $V_{DD} + 0.5$ V
	Voltage range at any input terminal	-0.5 V to $V_{DD} + 0.5$ V
$T_{stg}$	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under „absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under „recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.

### POWER DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>(1)</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
DBQ	830 mW	8.3 mW/°C	332 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VDDP, VDDPA, VDDO	Supply voltage	3	3.3	3.6	V
$V_{IH}$ (CMOS)	High-level input voltage	0.7 VDD			V
$V_{IL}$ (CMOS)	Low-level input voltage			0.3 VDD	V
$V_{IL}$ (DLYCTRL, LEADLAG)	Input signal low voltage			$\frac{VDDPD}{2} - 0.2$	V
$V_{IH}$ (DLYCTRL, LEADLAG)	Input signal high voltage			$\frac{VDDPD}{2} + 0.2$	V
(VDDPD)	Input reference voltage for DLYCNTRL and LEADLAG	1.2		VDD	V
$I_{OH}$	High-level output current			-16	mA
$I_{OL}$	Low-level output current			16	mA
(VDDREF) (see Application section)	Input reference voltage for REFCLK	1.2		VDD	V
$V_{IL}$ (see Application section)	REFCLK input low voltage			$\frac{VDDREF}{2} - 0.2$	V
$V_{IH}$ (see Application section)	REFCLK input high voltage			$\frac{VDDREF}{2} + 0.2$	V
$T_A$	Operating free-air temperature	-40		85	°C

## TIMING REQUIREMENTS

	PARAMETER	MIN	MAX	UNIT
$F_{mod}$	Input frequency of modulation, (if driven by SSC CLKIN)		33	kHz
	Modulation index, nonlinear maximum 0.5%		0.6%	
SR	Input slew rate	1	4	V/ns
	Input duty cycle on REFCLK	40%	60%	
	Input frequency on REFCLK	12.5	240	MHz
	Output frequency on CLKOUT and CLKOUTB	25	280	MHz
	Allowable frequency on DLYCTRL		240	MHz

## TIMING REQUIREMENTS (continued)

PARAMETER	MIN	MAX	UNIT
Allowable frequency on LEADLAG		280	MHz
Allowable duty cycle on DLYCTRL and LEADLAG pins	25%	75%	

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
V <sub>O(STOP)</sub>	Output voltage during Clkstop mode	See Figure 1	1.1	2	V	
V <sub>O(X)</sub>	Output crossing-point voltage	See Figure 1 and Figure 4	$\frac{V_{DDO}}{2} - 0.2$	$\frac{V_{DDO}}{2} + 0.2$	V	
V <sub>O</sub>	Output voltage swing (V <sub>OH</sub> - V <sub>OL</sub> )	See Figure 1	1.7	2.9	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>DD</sub> = 3 V, I <sub>I</sub> = -18 mA		-1.2	V	
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 3 to 3.6 V, See Figure 1	2	2.5	V	
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = -16 mA	2.2			
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 3 to 3.6 V, See Figure 1	0.4	0.6	V	
		V <sub>DD</sub> = 3 V, I <sub>OH</sub> = 16 mA		0.5		
I <sub>OH</sub>	High-level output current	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1 V	-32	-52	mA	
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		-51		
		V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 3.135 V	-14.5	-21		
I <sub>OL</sub>	Low-level output current	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1.95 V	43	61.5	mA	
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		65		
		V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 0.4 V	25.5	40		
I <sub>OZ</sub>	High-impedance-state output current	P0 = 1, P1 = P2 = 0		±10	µA	
I <sub>OZ(STOP)</sub>	High-impedance-state output current during Clk Stop	Stop = 0, V <sub>O</sub> = GND or V <sub>DD</sub>		±100	µA	
I <sub>OZ(PD)</sub>	High-impedance-state output current in power-down state	PWRDNB = 0, V <sub>O</sub> = GND or V <sub>DD</sub>	-10	100	µA	
I <sub>IH</sub>	High-level input current	REFCLK; STOPB; PWRDNB; P[0:2]; MULT[0:1]; DLYCTRL; LEADLAG	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = V <sub>DD</sub>		10	µA
I <sub>IL</sub>			V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0		-10	µA
Z <sub>O</sub>	Output impedance (single ended)	High state	R <sub>I</sub> at I <sub>O</sub> -14.5 mA to -16.5 mA	15	35	Ω
		Low state	R <sub>I</sub> at I <sub>O</sub> 14.5 mA to 16.5 mA	10	17	
I <sub>REF</sub>	Reference current	V <sub>DDREF</sub> ; VDDPD	V <sub>DD</sub> = 3.6 V	PWRDNB = 0	50	µA
				PWRDNB = 1	0.5	mA
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = V <sub>DD</sub> or GND		2	pF	
C <sub>O</sub>	Output capacitance	V <sub>O</sub> = GND or V <sub>DD</sub>		3	pF	
I <sub>DD(PD)</sub>	Supply current in power-down state	REFCLK = 0 MHz to 280 MHz; PWRDNB = 0; STOPB = 1		4	mA	
I <sub>DD(CLKSTOP)</sub>	Supply current in CLK stop state	BUSCLK configured for 280 MHz		44	mA	
I <sub>DD(NORMAL)</sub>	Supply current (normal operation mode)	BUSCLK 280 MHz, MULT[0:1] = 10; P[0:2] = 011; Load, See Figure 1		75	mA	

(1) V<sub>DD</sub> refers to any of the following; VDDP, VDDREF, VDDO, VDDPD, and VDDPA

(2) All typical values are at V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**JITTER SPECIFICATION**

over recommended free-air temperature range and  $V_{CC}$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				NOTES	TYP (ps)	MAX (ps)
		REFCLK (MHz)	CLKOUT (MHz)	MULT[0:1]	P[0:2]			
$t_{(jitter)}$	Period rms (1-sigma jitter, full frequency band)	25	25	11	001	Phase aligner running (CLKOUT tight to LEADLAG; REFCLK tight to DLYCTRL). All typical values are at $V_{DD} = 3.3 V$ , $T_A = 25^{\circ}C$ .	20	48
	Period p-p						120	225
	Cycle to cycle +						70	165
	Cycle to cycle -						70	165
	RMS phase jitter (accumulated, 100 kHz-12.5 MHz)						80	160
	Period rms (1-sigma jitter, full frequency band)	50	50	11	001		7	15
	Period p-p						37	75
	Cycle to cycle +						27	55
	Cycle to cycle -						27	55
	RMS phase jitter (accumulated, 100 kHz-25 MHz)						27	65
	Period rms (1-sigma jitter, full frequency band)	100	100	00	010		5	14
	Period p-p						30	65
	Cycle to cycle +						24	55
	Cycle to cycle -						24	55
	RMS phase jitter (accumulated, 100 kHz-40 MHz)						35	65
	Period rms (1-sigma jitter, full frequency band)	156	156	00	010		4	8
	Period p-p						20	40
	Cycle to cycle +						17	40
	Cycle to cycle -						17	40
	RMS phase jitter (accumulated, 100 kHz-40 MHz)						15	35
Period rms (1-sigma jitter, full frequency band)	200	200	01	011	8	15		
Period p-p					38	60		
Cycle to cycle +					5	55		
Cycle to cycle -					35	55		
RMS phase jitter (accumulated, 100 kHz-40 MHz)					30	60		



## JITTER SPECIFICATION (continued)

over recommended free-air temperature range and  $V_{CC}$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				NOTES	TYP (ps)	MAX (ps)
		REFCLK (MHz)	CLKOUT (MHz)	MULT[0:1]	P[0:2]			
$t_{(jitter)}$	Period rms (1-sigma jitter, full frequency band)	25	200	10	011	Phase aligner not running (LEADLAG = 0, DLYCTRL = 0). All typical values are at $V_{DD} = 3.3V$ , $T_A = 25^\circ C$ .	4	11
	Period p-p						20	48
	Cycle to cycle +						16	45
	Cycle to cycle -						16	45
	Period rms (1-sigma jitter, full frequency band)	25	100	10	010		4	11
	Period p-p						22	55
	Cycle to cycle +						15	45
	Cycle to cycle -						15	45
	Period rms (1-sigma jitter, full frequency band)	70	280	11	011		4	11
	Period p-p						18	48
	Cycle to cycle +						15	45
	Cycle to cycle -						15	45
	Period rms (1-sigma jitter, full frequency band)	25	50	10	001		6	16
	Period p-p						34	75
	Cycle to cycle +						20	65
	Cycle to cycle -						20	65
	Period rms (1-sigma jitter, full frequency band)	78	156	11	010		3	11
	Period p-p						15	44
	Cycle to cycle +						13	40
	Cycle to cycle -						13	40
Period rms (1-sigma jitter, full frequency band)	62.5	125	00	011	6	20		
Period p-p					35	80		
Cycle to cycle +					25	75		
Cycle to cycle -					25	75		

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DC)}$	Output duty cycle over 1000 cycles	See <a href="#">Figure 3</a>	42%		58%	
$t_r, t_f$	Output rise and fall times (measured at 20%-80% of output voltage)	See <a href="#">Figure 5</a>	150	250	350	ps

## STATE TRANSITION LATENCY SPECIFICATIONS

PARAMETER		FROM	TO	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB $\uparrow$ to CLKOUT / CLKOUTB settled	Power down	Normal	See <a href="#">Figure 6</a>			3	ms
	Delay time, PWRDNB $\uparrow$ to internal PLL and clock are on and settled						3	

**STATE TRANSITION LATENCY SPECIFICATIONS (continued)**

PARAMETER		FROM	TO	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{(VDDpowerup)}$	Delay time, power up to CLKOUT output settled	$V_{DD}$	Normal	See Figure 6			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLKOUT output resettled	Normal	Normal	See Figure 7			1	ms
$t_{(CLKON)}$	STOPB $\uparrow$ to CLKOUT glitch-free clock edges	CLK stop	Normal	See Figure 8			10	ns
$t_{(CLKSETL)}$	STOPB $\uparrow$ to CLKOUT output settled to within 50 ps of the phase before STOPB was disabled	CLK stop	Normal	See Figure 8			20	cycles
$t_{(CLKOFF)}$	STOPB $\downarrow$ to CLKOUT output disabled	Normal	CLK stop	See Figure 8			5	ns
$t_{(powerdown)}$	Delay time, PWRDNB $\downarrow$ to the device in the power-down mode	Normal	Power down	See Figure 6			1	ms
$t_{(STOP)}$	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 8	100			$\mu$ s
$t_{(ON)}$	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK stop	See Figure 8	100			ms

**PARAMETER MEASUREMENT INFORMATION**

**TESTING CONDITIONS**

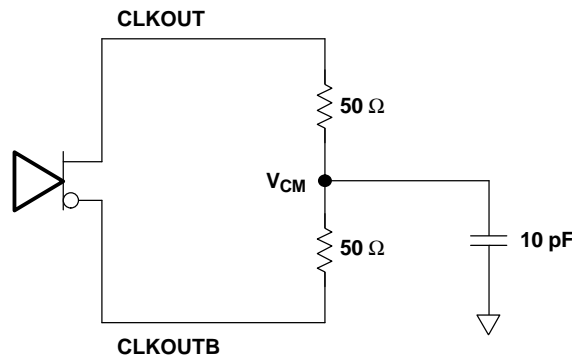
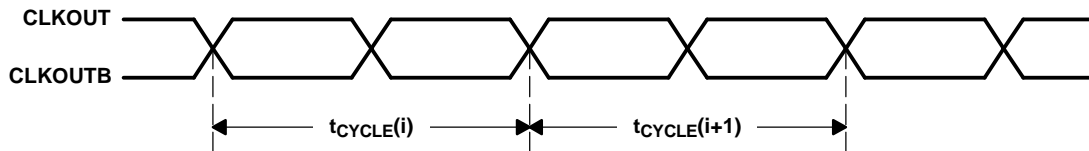


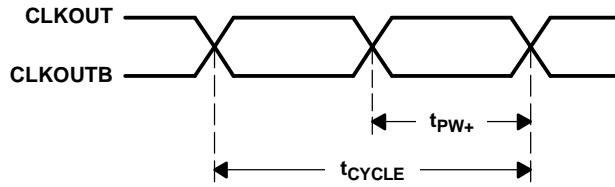
Figure 1. Test Load and Voltage Definitions  $V_{OH}$ ,  $V_{OL}$ ,  $V_{O(STOP)}$



Cycle-to-Cycle Jitter ( $t_{(jitter)}$ ) =  $|t_{CYCLE(i)} - t_{CYCLE(i+1)}|$  over 1000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION (continued)



Duty Cycle =  $(t_{PW+}/t_{CYCLE})$

Figure 3. Output Duty Cycle

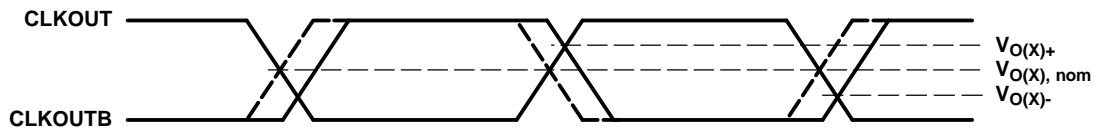


Figure 4. Crossing Point Voltage



Figure 5. Voltage Waveforms

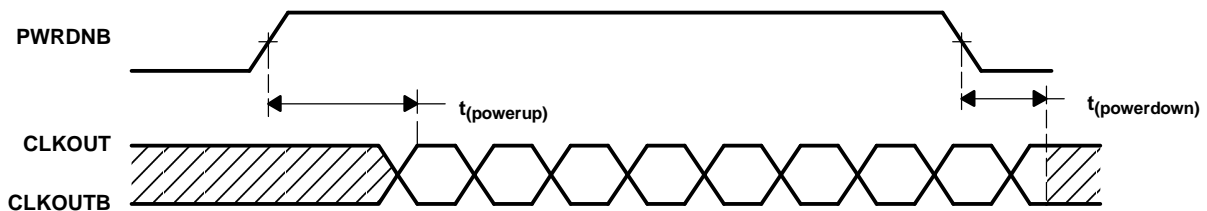


Figure 6. PWRDNB Transition Timings

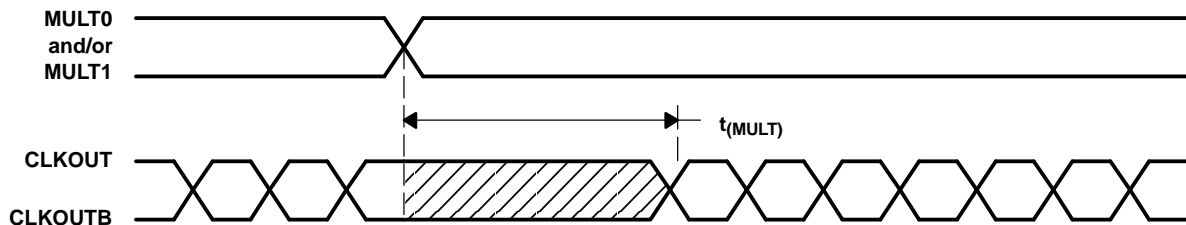
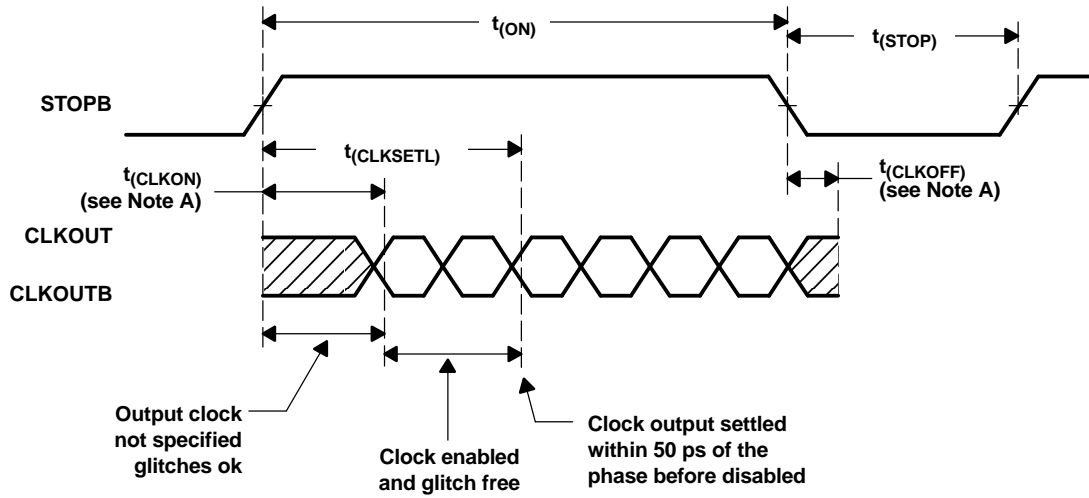


Figure 7. MULT Transition Timings

PARAMETER MEASUREMENT INFORMATION (continued)



A.  $V_{ref} = V_O \pm 200 \text{ mV}$

Figure 8. STOPB Transition Timings

## APPLICATION INFORMATION

### APPLICATION EXAMPLE

The following figure shows an example of using the CDCF5801A as a phase aligner de-skewing the unknown buffer delay of the two CDCV304s in the circuit. This circuitry would not be possible with a simple PLL because the feedback of the PLL would have the second CDCV304 in the loop, causing instability of the PLL due to a long delay.

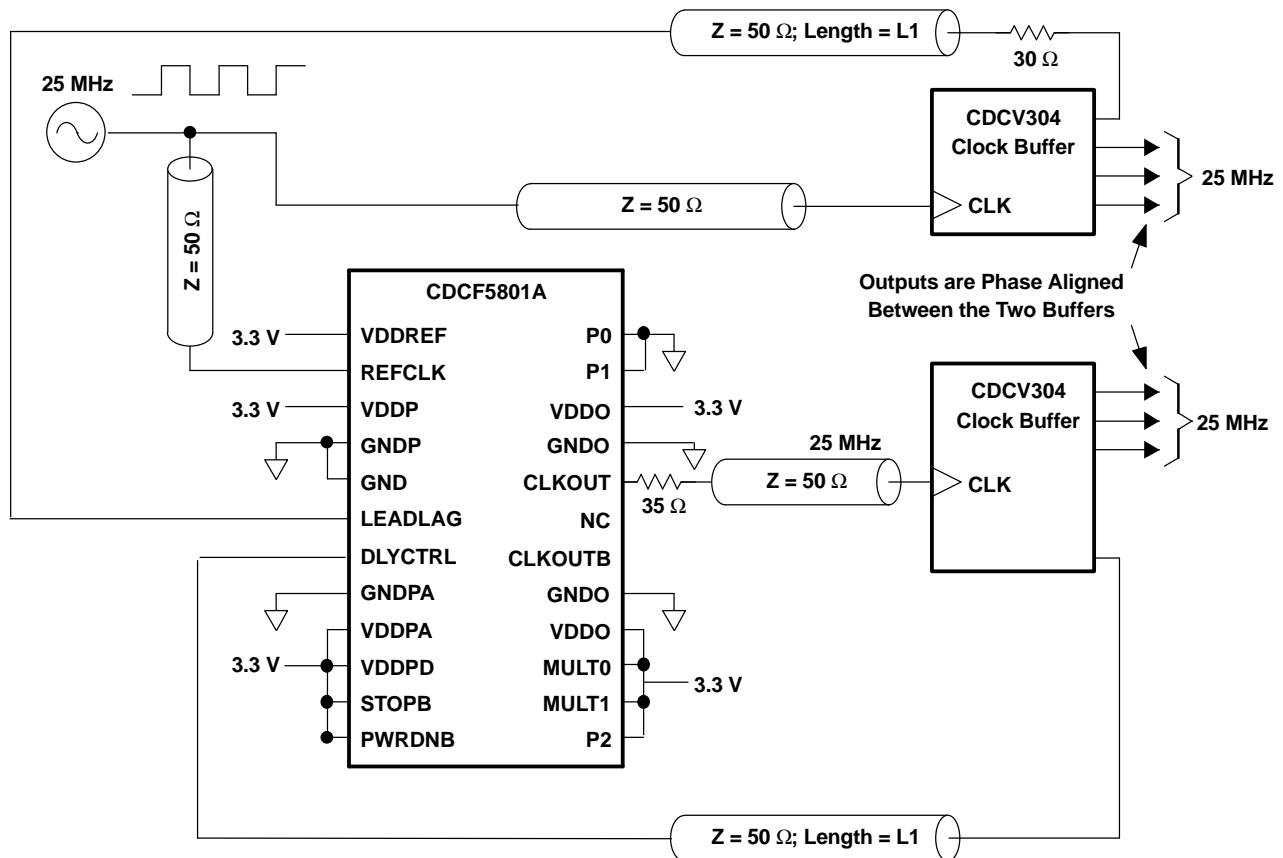


Figure 9. Application Example

#### NOTE:

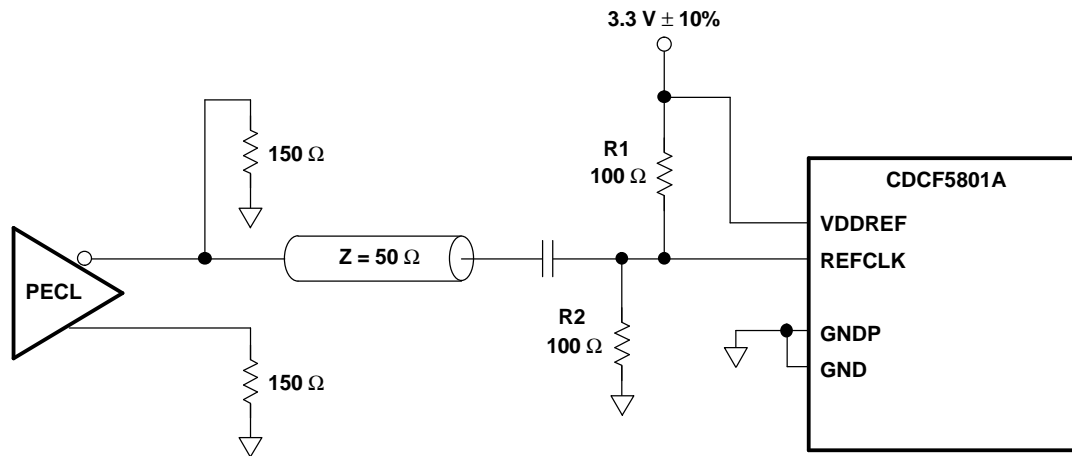
If an active element (microcontroller, ASIC, DSP, FPYA, DSP, etc.) is used in the CDCF5801A CLKOUT to DLYCTRL feedback loop, see application report SCAA075.

### SELECTING VDDREF

Generally, VDDREF can be set to any value between 1.2 V and VDD. The setting of VDDREF directly influences the trigger voltage of the input. Special care must be taken when using small signal swings to drive the CDCF5801 input (e.g., PECL). It is recommended to connect VDDREF directly to VDD, ac-couple the REFCLK input, and rebias the signal.

The following circuit is recommended to drive the CDCF5801A from a differential clock signal like PECL.

APPLICATION INFORMATION (continued)



- A. NOTE: If more signal swing is required and an unterminated transmission is on option, then R1 and R2 can both be replaced with 10-k $\Omega$  resistors.

**Figure 10. Driving the CDCF5801A From a Differential Clock Signal**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CDCF5801ADBQ</a>	Active	Production	SSOP (DBQ)   24	50   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801A
<a href="#">CDCF5801ADBQR</a>	Active	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCF5801A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCF5801ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCF5801ADBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDCF5801ADBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32
CDCF5801ADBQG4	DBQ	SSOP	24	50	506.6	8	3940	4.32



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated