

## CD74HC4538-Q1 汽车类高速 CMOS 逻辑双通道可重触发精密单稳多谐振荡器

### 1 特性

- 符合汽车应用要求
- 符合汽车应用的可重触发/可复位功能要求
- 触发和复位传播延迟不受  $R_X$ 、 $C_X$  的影响
- 从前沿或后沿触发
- 提供  $Q$  和  $\bar{Q}$  缓冲输出
- 单独复位
- 宽范围的输出脉冲宽度
- A 和 B 输入端的施密特触发器输入
- 再触发时间与  $C_X$  无关
- 扇出 (在温度范围内)
  - 标准输出 10 个 LSTTL 负载
  - 总线驱动器输出 15 个 LSTTL 负载

- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比, 可显著降低功耗
- $V_{CC}$  电压 = 2V 至 6V
- 高抗噪性,  $N_{IL}$  或  $N_{IH} = V_{CC}$  的 30%,  $V_{CC} = 5V$

### 2 说明

CD74HC4538 是一款适用于固定电压时序应用的双路可重触发/可复位精密单稳多谐振荡器。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸
CD74HC4538-Q1	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.90mm
	PW (TSSOP, 16)	5mm × 6.4mm	5.00mm × 4.40mm

- (1) 如需了解更多信息, 请参阅[机械、封装和可订购信息](#)。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。



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### 3 Pin Configuration and Functions

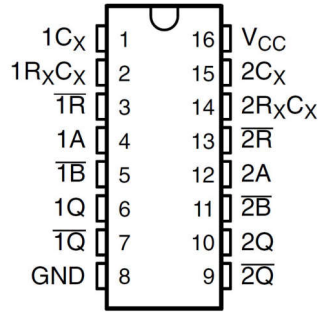


图 3-1. D or PW Package; 16-Pin SOIC or TSSOP (Top View)

表 3-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1C <sub>x</sub>	1	—	Connects to external capacitor
1R <sub>x</sub> C <sub>x</sub>	2	—	Connects to external capacitor and resistor
1 $\overline{R}$	3	—	Connects to external resistor
1A	4	I	Ch1 Rising edge input
1B	5	I	Ch1 Falling edge input
1Q	6	O	Ch1 Output
$\overline{1Q}$	7	O	Ch1 Inverted Output
GND	8	—	Ground
$\overline{2Q}$	9	O	Ch2 Inverted Output
2Q	10	O	Ch2 Output
$\overline{2B}$	11	I	Ch2 Falling edge input
2A	12	I	Ch2 Rising edge input
2R	13	—	Connects to external resistor
2R <sub>x</sub> C <sub>x</sub>	14	—	Connects to external capacitor and resistor
2C <sub>x</sub>	15	—	Connects to external capacitor
V <sub>CC</sub>	16	—	Power Pin

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		- 0.5	7	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> + 0.5V)		±20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V)		±20	mA
I <sub>O</sub>	Switch current per output pin	(V <sub>O</sub> > -0.5V or V <sub>O</sub> < V <sub>CC</sub> + 0.5V)		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Maximum junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		- 65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are referenced to GND, unless otherwise specified.

### 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±1500	V
		Charged device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 4.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2V	1.5		V
		V <sub>CC</sub> = 4.5V	3.15		
		V <sub>CC</sub> = 6V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2V		0.5	V
		V <sub>CC</sub> = 4.5V		1.35	
		V <sub>CC</sub> = 6V		1.8	
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
t <sub>t</sub>	Reset input	V <sub>CC</sub> = 2V	0	1000	ns
		V <sub>CC</sub> = 4.5V	0	500	
		V <sub>CC</sub> = 6V	0	400	
	Trigger inputs A or B	V <sub>CC</sub> = 2V	0	Unlimited	
		V <sub>CC</sub> = 4.5V	0	Unlimited	
		V <sub>CC</sub> = 6V	0	Unlimited	
R <sub>X</sub>	External timing resistor <sup>(1)</sup>		5		k Ω
C <sub>X</sub>	External timing capacitor <sup>(1)</sup>		0		F
T <sub>A</sub>	Operating free-air temperature		- 40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74HC4538-Q1		UNIT
		D	PW	
		16 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$I_{OM}$	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	CMOS loads	2 V	1.9	1.9	1.9			V	
			4.5 V	4.4	4.4	4.4				
			6 V	5.9	5.9	5.9				
		TTL loads	- 4	4.5 V	3.98	3.84	3.7			
-5.2	6 V		5.48	5.34	5.2					
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	CMOS loads	2 V		0.1	0.1	0.1	V		
			4.5 V		0.1	0.1	0.1			
			6 V		0.1	0.1	0.1			
		TTL loads	4	4.5 V	0.26	0.33	0.4			
5.2	6 V		0.26	0.33	0.4					
$I_I$	$V_I = V_{CC}$ or GND	A, $\bar{B}$ , R	6 V		$\pm 1$	$\pm 1$	$\pm 1$	$\mu\text{A}$		
		$R_X C_X$ <sup>(1)</sup>	6 V		$\pm 0.05$	$\pm 0.05$	$\pm 0.05$			
$I_{CC}$	$V_I = V_{CC}$ or GND	Quiescent	0	6 V	8	80	160	$\mu\text{A}$		
		Active, Q = high, Pins 2 and 14 at $V_{CC}/4$	0	6 V	0.6	0.8	1	mA		
$C_{IN}$	$C_L = 50\text{ pF}$				10	10	10	pF		

(1) When testing  $I_{IL}$ , the Q output must be high. If Q is low (device not triggered), the pullup P device is ON and the low-resistance path from  $V_{DD}$  to the test pin causes a current far exceeding the specification.

## 4.6 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_w$	Input pulse width	2 V	80		100		120		ns
		4.5 V	16		20		24		
		6 V	14		17		20		
$t_{su}$	Reset setup time	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
$t_{rr}$	Retrigger time	5 V		175				ns	
	Output pulse-width match, same package			$\pm 1$				%	

## 4.7 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A, $\bar{B}$	Q or $\bar{Q}$	$C_L = 50\text{ pF}$	2 V		250		315		375	ns	
				4.5 V		50		63		75		
				6 V		43		54		64		
	$\bar{R}$	Q or $\bar{Q}$	$C_L = 50\text{ pF}$	5 V		21						
				2 V		250		315		375		
				4.5 V		50		63		75		
$t_t$			$C_L = 50\text{ pF}$	6 V		43		54		64	ns	
				2 V		75		95		110		
				4.5 V		15		19		22		
$\tau^{(1)}$			$C_L = 50\text{ pF}$	3 V	0.64	0.78	0.612	0.812	0.605	0.819	ms	
				5 V	0.63	0.77	0.602	0.798	0.595	0.805		

(1) Output pulse width with  $R_X = 10\text{ k}\Omega$  and  $C_X = 0.1\text{ }\mu\text{F}$

## 4.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , input  $t_r$ ,  $t_f = 6\text{ ns}$ ,  $C_L = 15\text{ pF}$

PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	136	pF

### 备注

- $C_{pd}$  is used to determine the dynamic power consumption, per one shot.
- $P_D = (C_{pd} + C_X) V_{CC} 2 f_I \approx (C_L V_{CC} 2 f_O)$
- $f_I$  = input frequency
- $f_O$  = output frequency
- $C_L$  = output load capacitance
- $C_X$  = external capacitance
- $V_{CC}$  = supply voltage, assuming  $f_I \ll \tau$

### 4.9 Typical Characteristics

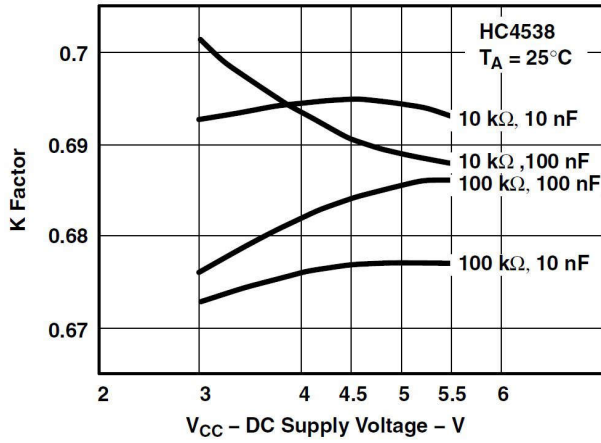


图 4-1. K Factor vs DC Supply Voltage

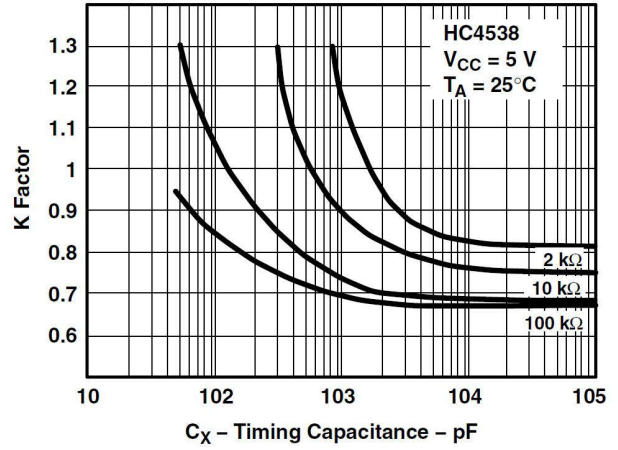


图 4-2. K Factor vs  $C_X$

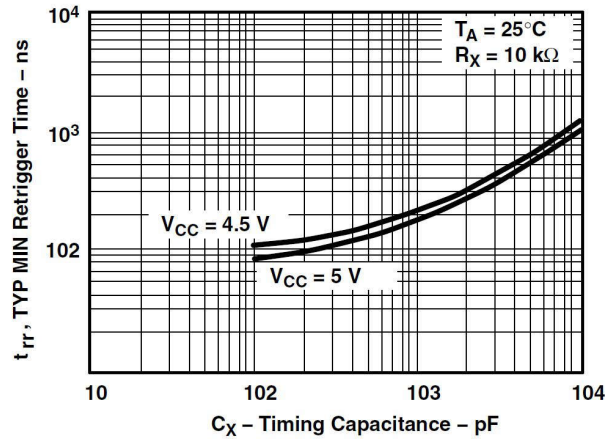
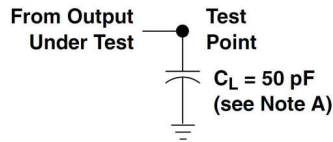


图 4-3. Minimum Retrigger Time vs Timing Capacitance

## 5 Parameter Measurement Information

### Load Circuit and Voltage Waveforms



LOAD CIRCUIT

图 5-1. Load Circuit

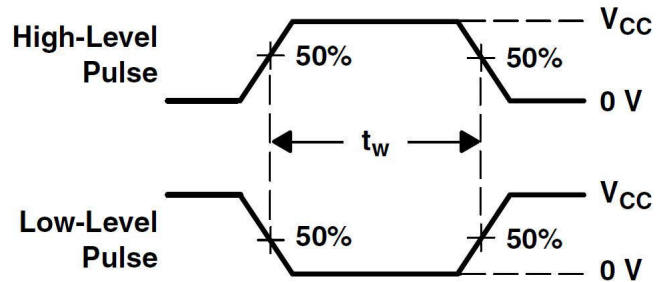


图 5-2. Voltage Waveforms Pulse Durations

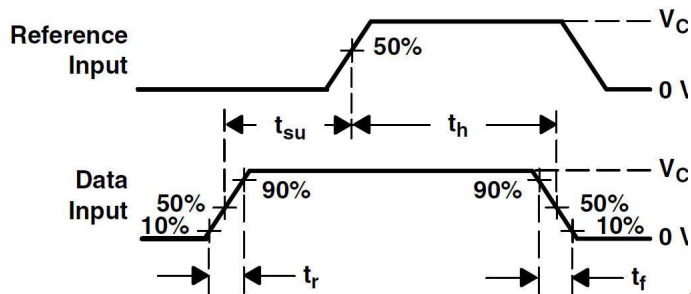


图 5-3. Voltage Waveforms Setup and Hold and Input Rise and Fall Times

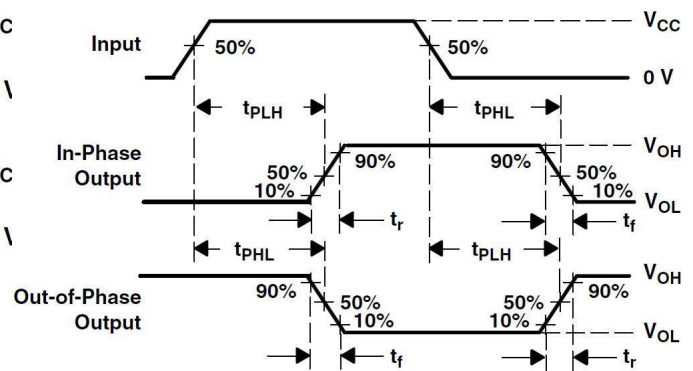


图 5-4. Voltage Waveforms Propagation Delay and Output Transition Times

#### 备注

- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \ \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- The outputs are measured one at a time, with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .





### 6.3 Device Functional Modes

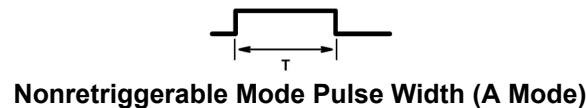
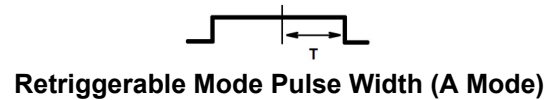
表 6-1. Function Table

INPUTS			OUTPUTS	
$\bar{R}$	A	$\bar{B}$	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⌋	⌋
H	↑	H	⌋	⌋

表 6-2. Functional Terminal Connections

FUNCTION	V <sub>CC</sub> TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	MONO <sup>(1)</sup>	MONO <sup>(2)</sup>	MONO <sup>(1)</sup>	MONO <sup>(2)</sup>	MONO <sup>(1)</sup>	MONO <sup>(2)</sup>	MONO <sup>(1)</sup>	MONO <sup>(2)</sup>
Leading-edge trigger/retriggerable	3, 5	11, 13			4	12		
Leading-edge trigger/nonretriggerable	3	13			4	12	5-7	11-9
Trailing-edge trigger/retriggerable	3	13	4	12	5	11		
Trailing-edge trigger/nonretriggerable	3	13			5	11	4-6	12-10

- (1) A retriggerable one-shot multivibrator has an output pulse width that is extended one full time period (T) after application of the last trigger pulse.
- (2) A nonretriggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Typical Application

#### Power-Down Mode

During a rapid power-down condition (as would occur with a power-supply short circuit with a poorly filtered power supply), the energy stored in  $C_X$  could discharge into pin 2 or pin 14. To avoid possible device damage in this mode when  $C_X$  is  $\geq 0.5 \mu\text{F}$ , a protection diode with a 1-A rating or higher (1N5395 or equivalent) and a separate ground return for  $C_X$  should be provided. [Rapid-Power-Down Protection Circuit](#)

An alternate protection method is shown in [Alternative Rapid-Power-Down Protection Circuit](#), where a  $51\text{-}\Omega$  current-limiting resistor is inserted in series with  $C_X$ . Note that a small pulse-duration decrease occurs, however, and  $R_X$  must be increased appropriately to obtain the originally desired pulse duration.

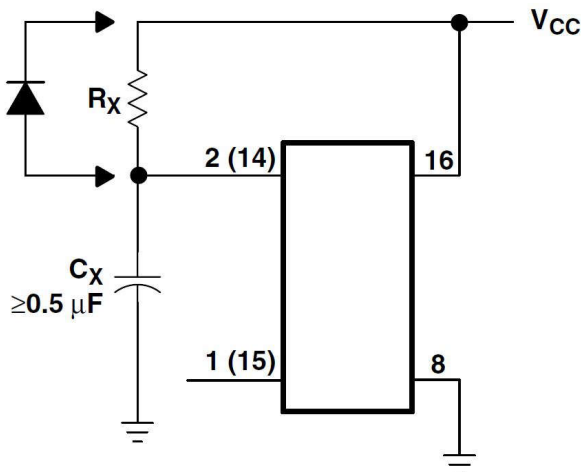


图 7-1. Rapid-Power-Down Protection Circuit

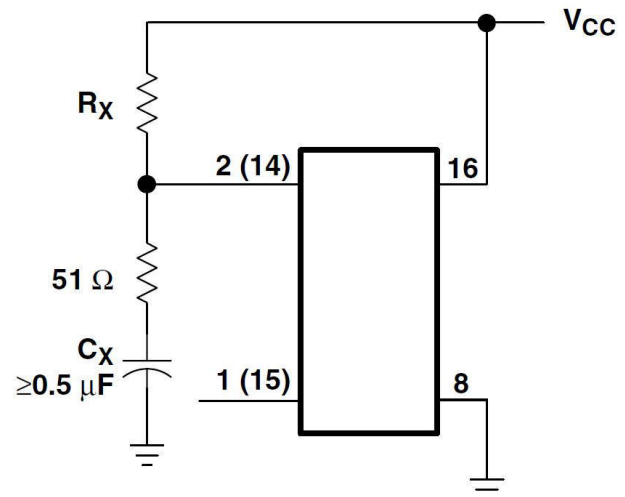


图 7-2. Alternative Rapid-Power-Down Protection Circuit

### 7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\text{-}\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\text{-}\mu\text{F}$  and  $1\text{-}\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

### 7.3 Layout

#### 7.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used,

or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74HC4538-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

Changes from Revision A (April 2008) to Revision B (August 2024)	Page
• 添加了 <a href="#">封装信息表</a> 、 <a href="#">引脚功能表</a> 、 <a href="#">ESD 等级表</a> 、 <a href="#">热性能信息表</a> 、 <a href="#">器件功能模式</a> 、“ <a href="#">应用和实施</a> ”部分、 <a href="#">器件和文档支持</a> 部分以及 <a href="#">机械、封装和可订购信息</a> 部分.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD74HC4538QM96G4Q</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
<a href="#">CD74HC4538QPWRG4C</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M
<a href="#">CD74HC4538QPWRQ1</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4538M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD74HC4538-Q1 :**

- Catalog : [CD74HC4538](#)

- Military : [CD54HC4538](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4538QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4538QPWRG4Q1	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4538QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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