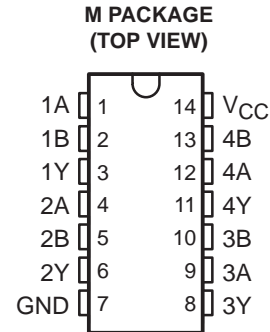


# CD74HC08-EP QUADRUPLE 2-INPUT POSITIVE-AND GATES

SCLS477B – APRIL 2003 – REVISED APRIL 2004

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of Up To  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Buffered Inputs**
- **Typical Propagation Delay 7 ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^{\circ}\text{C}$**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **2-V to 6-V  $V_{CC}$  Operation**
- **High Noise Immunity  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$**
- **CMOS Input Compatibility,  $I_I \leq 1\ \mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



## description/ordering information

The CD74HC08 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. All devices can drive 10 LSTTL loads.

### ORDERING INFORMATION

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – M	Tape and reel	CD74HC08QM96EP	HC08QEP
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – M	Tape and reel	CD74HC08MM96EP§	HC08MEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

§ Product Preview

**FUNCTION TABLE**  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# CD74HC08-EP

## QUADRUPLE 2-INPUT POSITIVE-AND GATES

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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	180°C/W
Maximum junction temperature, $T_J$ .....	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ( $1,59 \pm 0,79$ mm) from case for 10 s max .....	300°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 6$ V		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		400	
$T_A$	Operating free-air temperature	Q suffix	-40	125	°C
		M suffix	-55	125	

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# CD74HC08-EP QUADRUPLE 2-INPUT POSITIVE-AND GATES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I <sub>O</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9			1.9	V	
			-0.02	4.5 V	4.4			4.4		
			-0.02	6 V	5.9			5.9		
		TTL loads	-4	4.5 V	3.98			3.7		
			-5.2	6 V	5.48			5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V	0.1			0.1	V	
			0.02	4.5 V	0.1			0.1		
			0.02	6 V	0.1			0.1		
		TTL loads	4	4.5 V	0.26			0.4		
			5.2	6 V	0.26			0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			6 V	±0.1			±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		0	6 V	2			40	μA	
C <sub>i</sub>					10			10	pF	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t <sub>pd</sub>	A or B	Y	C <sub>L</sub> = 50 pF	2 V	90			135	ns	
				4.5 V	18			27		
				6 V	15			23		
			C <sub>L</sub> = 15 pF	5 V	7					
t <sub>t</sub>	A or B	Y	C <sub>L</sub> = 50 pF	2 V	75			110	ns	
				4.5 V	15			22		
				6 V	13			19		

operating characteristics, T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate (see Note 4)	No load	37	pF

NOTE 4: C<sub>pd</sub> is used to determine the dynamic power consumption, per gate.

$$P_D = V_{CC}^2 f_I (C_{pd} + C_L)$$

f<sub>I</sub> = input frequency

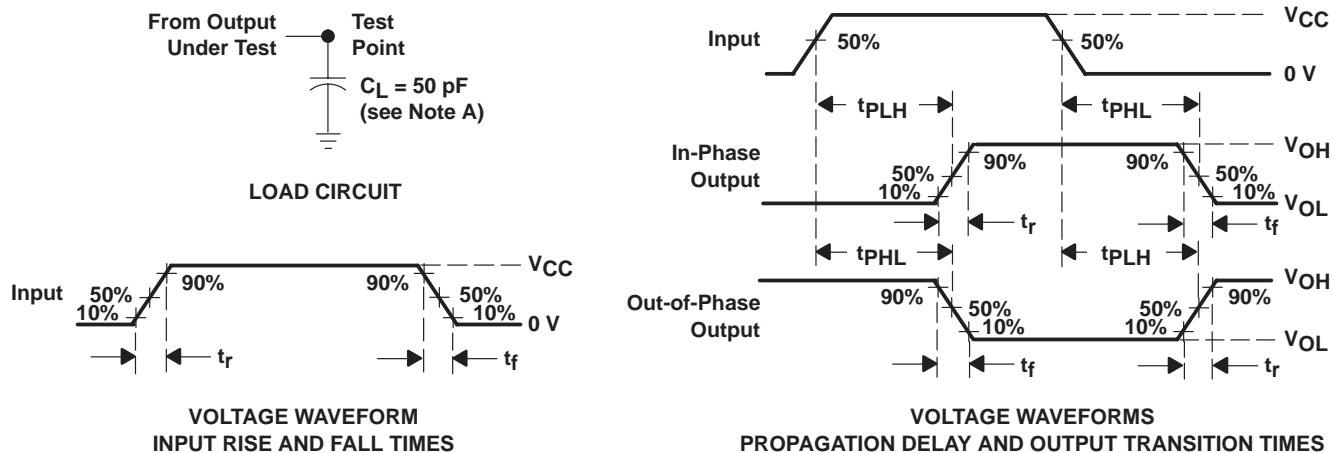
C<sub>L</sub> = output load capacitance

V<sub>CC</sub> = supply voltage

# CD74HC08-EP QUADRUPLE 2-INPUT POSITIVE-AND GATES

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time, with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD74HC08QM96EP</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC08QEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD74HC08-EP :**

- Catalog : [CD74HC08](#)
- Automotive : [CD74HC08-Q1](#)

- Military : [CD54HC08](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC08QM96EP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC08QM96EP	SOIC	D	14	2500	340.5	336.1	32.0



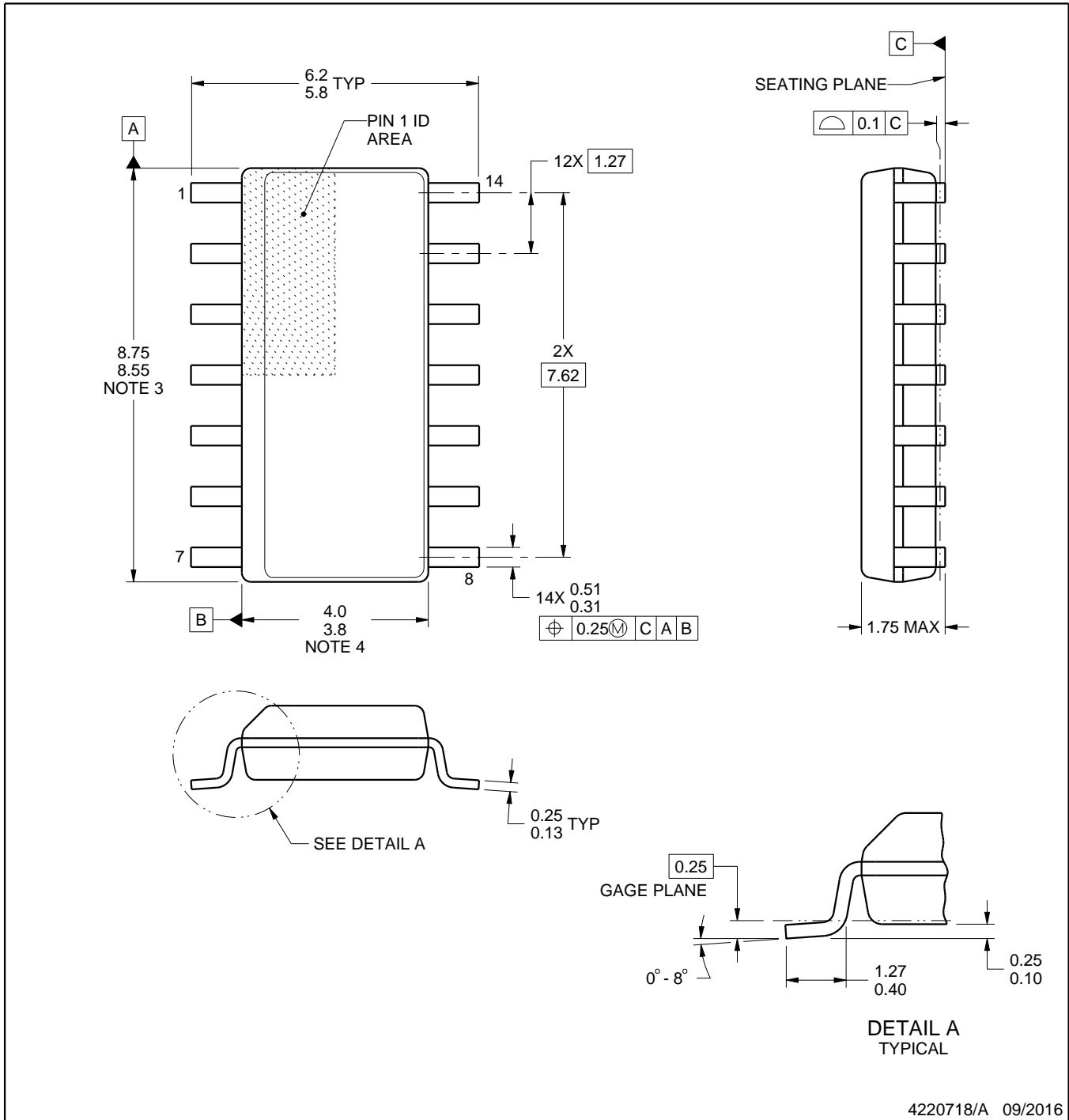
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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