

CDx4HC11 三路 3 输入与门

1 特性

- 缓冲输入
- 宽工作电压范围：2V 至 6V
- 宽工作温度范围：
-55°C 至 +125°C
- 支持多达 10 个 LSTTL 负载的扇出
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗

2 应用

- 将电源正常信号进行结合
- 使能数字信号

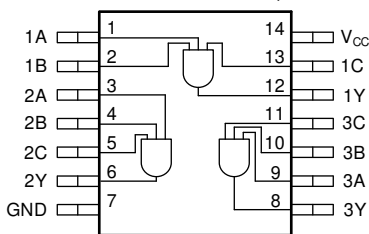
3 说明

此器件包含三个独立 3 输入与门。每个逻辑门以正逻辑执行布尔函数 $Y = A \bullet B \bullet C$ 。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
CD74HC11M	SOIC (14)	8.70mm × 3.90mm
CD74HC11E	PDIP (14)	19.30mm × 6.40mm
CD54HC11F	CDIP (14)	21.30mm × 7.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能引脚分配



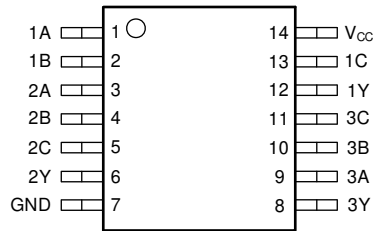
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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2003) to Revision F (April 2021)	Page
• 更新了整个文档的表、图和交叉参考的编号格式.....	1
• 更新至全新的数据表标准.....	1
• 将 HCT 器件移至单独的数据表 (SCHS405).....	1
• $R_{\theta JA}$ increased for the D package (86 to 133.6 °C/W) and decreased for the N package (80 to 65.2 °C/W).....	5



**图 5-1. D, N, or J Package
 14-Pin SOIC, PDIP, or CDIP
 Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
2A	3	Input	Channel 2, Input A
2B	4	Input	Channel 2, Input B
2C	5	Input	Channel 2, Input C
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
3C	11	Input	Channel 3, Input C
1Y	12	Output	Channel 1, Output Y
1C	13	Input	Channel 1, Input C
V _{CC}	14	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < - 0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _{OK}	Output clamp current ⁽²⁾	V _O < - 0.5 V or V _O > V _{CC} + 0.5 V		±20 mA
I _O	Continuous output current	V _O > - 0.5 V or V _O < V _{CC} + 0.5 V		±25 mA
Continuous current through V _{CC} or GND				±50 mA
T _J	Junction temperature ⁽³⁾	Plastic package	150	°C
		Hermetic package or die	175	
	Lead temperature (soldering 10s)	SOIC - lead tips only		300 °C
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 4.5 V	3.15		
		V _{CC} = 6 V	4.2		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 4.5 V		1.35	
		V _{CC} = 6 V		1.8	
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
t _t	Input transition time	V _{CC} = 2 V		1000	ns
		V _{CC} = 4.5 V		500	
		V _{CC} = 6 V		400	
T _A	Operating free-air temperature	- 55		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD74HC11		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.9	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.5	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.7	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
			25°C			- 40°C to 85°C			- 55°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	2 V	1.9		1.9		1.9			V
				4.5 V	4.4		4.4		4.4			
				6 V	5.9		5.9		5.9			
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	2 V		0.1		0.1		0.1	V	
				4.5 V		0.1		0.1		0.1		
				6 V		0.1		0.1		0.1		
I_I	Input leakage current	$V_I = V_{CC}$ or GND	6 V			± 0.1		± 1		± 1	μA	
						2		20		40		
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	$I_O = 0$	6 V							μA	
C_i	Input capacitance			5 V							pF	

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			- 40°C to 85°C			- 55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	A, B, or C	Y	$C_L = 50 \text{ pF}$	2 V		100		125		150	ns		
					4.5 V		20		25		30			
					6 V		17		21		26			
		A, B, or C	Y	$C_L = 15 \text{ pF}$	5 V		8							

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			- 40°C to 85°C			- 55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_t	Transition-time	Y	$C_L = 50\text{ pF}$	2 V	75			95			110			ns
				4.5 V	15			19			22			
				6 V	13			16			19			

5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate No load	2 V to 6 V		26		pF

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

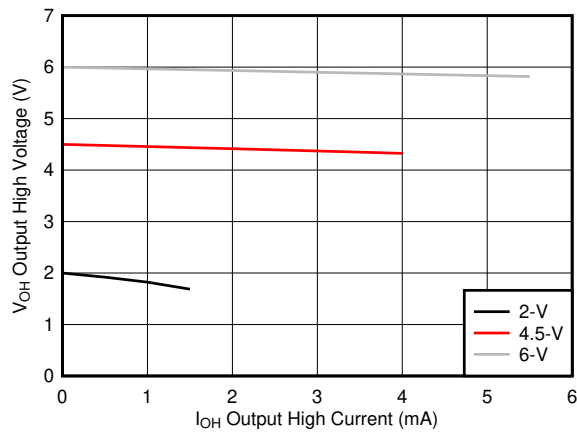


图 5-1. Typical output voltage in the high state (V_{OH})

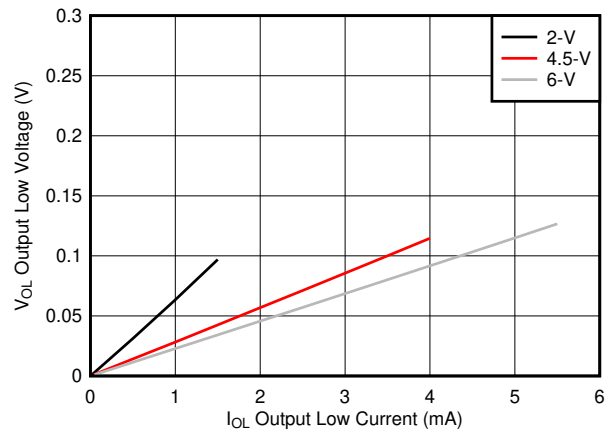
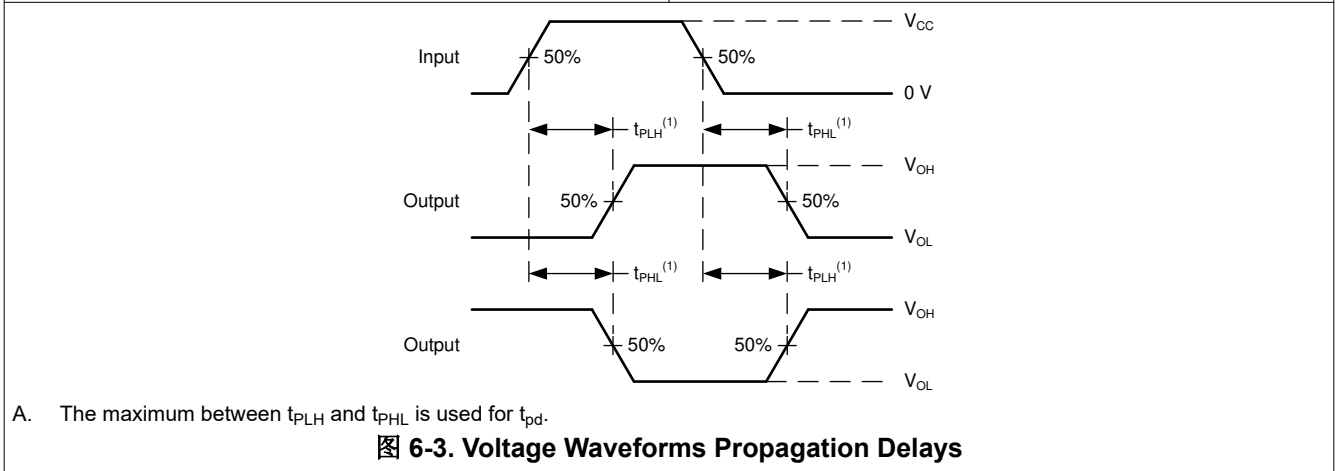
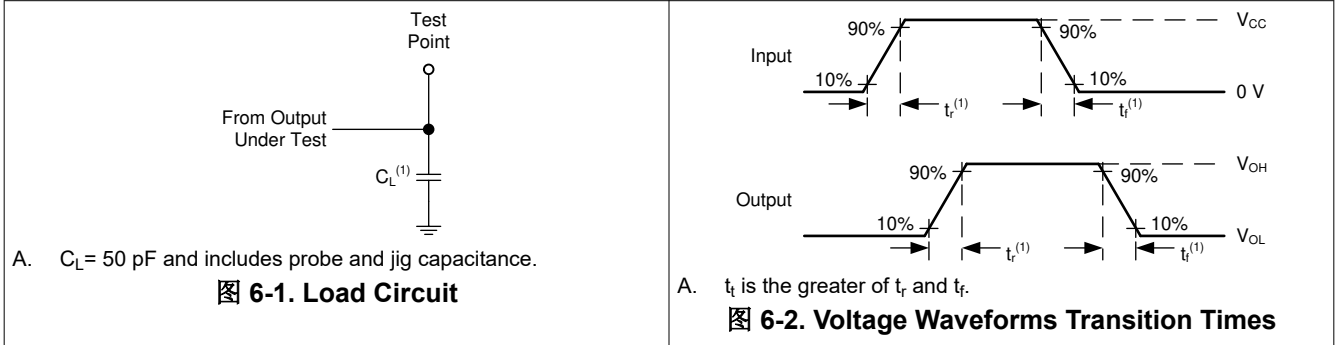


图 5-2. Typical output voltage in the low state (V_{OL})

6 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.

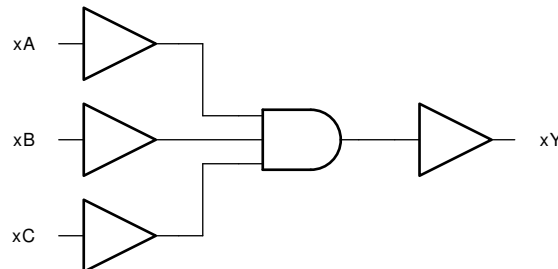


7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function $Y = A \bullet B \bullet C$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The CD74HC11 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Switching Characteristics](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 7-1.

CAUTION

Voltages beyond the values specified in the 节 5.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



图 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

8.2 Typical Application

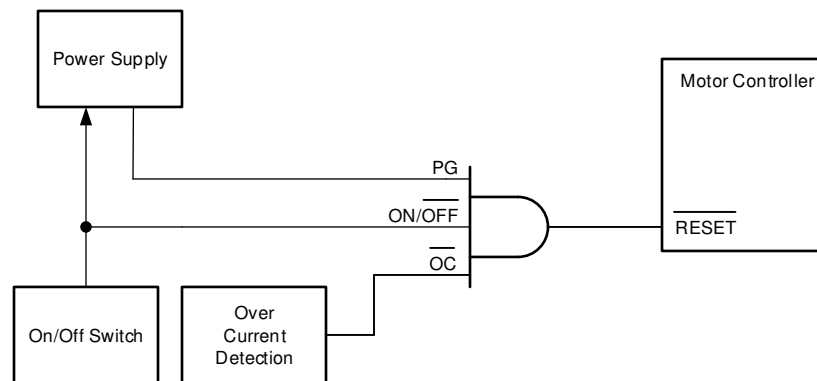


图 8-1. Typical application schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC11 plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\max)$ listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used

for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC11, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The CD74HC11 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the [Recommended Operating Conditions](#).

Refer to [# 7.3](#) for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [# 7.3](#) for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in [# 9](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC11 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

8.2.3 Application Curves

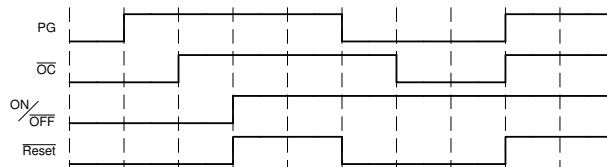


图 8-2. Typical application timing diagram

Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [# 5.3](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [图 9-1](#).

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

9.2 Layout Example

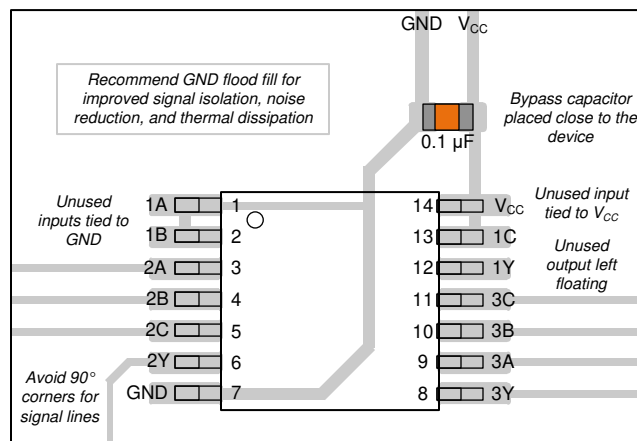


图 9-1. Example layout for the CD74HC11

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- [HCMOS Design Considerations](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

10.7 Community Resources

10.8 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC11F	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC11F
CD54HC11F3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404801CA CD54HC11F3A
CD74HC11E	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC11E
CD74HC11M	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HC11M
CD74HC11M96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC11M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC11, CD74HC11 :

- Catalog : [CD74HC11](#)
- Military : [CD54HC11](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC11M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC11M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC11E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC11E	N	PDIP	14	25	506	13.97	11230	4.32



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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