CDx4AC74 具有清零和预置功能的双路正边沿触发式 D 类触发器

1 特性

- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- ±24mA 输出驱动电流 – 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计

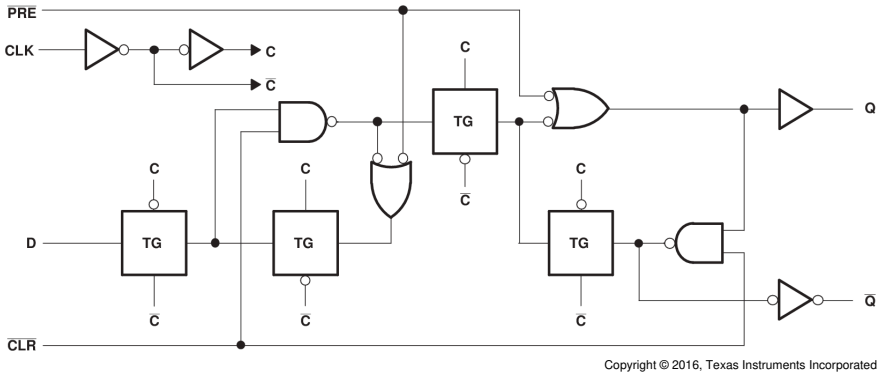
2 说明

AC74 双路正边沿触发器件是 D 型触发器。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
CDx4AC74	J（CDIP，14）	19.56mm × 7.9mm	19.56mm × 6.67mm
	N（PDIP，14）	19.3mm x 9.4mm	19.3mm x 6.35mm
	D（SOIC，14）	8.65mm x 6mm	8.65mm x 3.9mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



展示各触发器的逻辑图（正逻辑）

Table of Contents

3 Pin Configuration and Functions

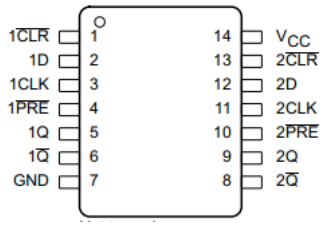


图 3-1. CD54AC74 F Package, 14-Pin CDIP; CD74AC74 E or M Package, 14-Pin PDIP or SOIC (Top View)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1 $\overline{CLR}$	1	Input	Channel 1, Clear Input, Active Low
1D	2	Input	Channel 1, Data Input
1CLK	3	Input	Channel 1, Positive edge triggered clock input
1 $\overline{PRE}$	4	Input	Channel 1, Preset Input, Active Low
1Q	5	Output	Channel 1, Output
1 $\overline{Q}$	6	Output	Channel 1, Inverted Output
GND	7	—	Ground
2 $\overline{Q}$	8	Output	Channel 2, Inverted Output
2Q	9	Output	Channel 2, Output
2 $\overline{PRE}$	10	Input	Channel 2, Preset Input, Active Low
2CLK	11	Input	Channel 2, Positive edge triggered clock input
2D	12	Input	Channel 2, Data Input
2 $\overline{CLR}$	13	Input	Channel 2, Clear Input, Active Low
V_{CC}	14	—	Positive Supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6	V
I_{IK} [1]	Input clamp current	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK} [1]	Output clamp current	(V_O < 0 or V_O > V_{CC})		±50	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			T_A = 25°C		−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		1.2		1.2		V
		V_{CC} = 3 V	2.1		2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 1.5 V		0.3		0.3		0.3	V
		V_{CC} = 3 V		0.9		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 4.5 V to 5.5 V		−24		−24		−24	mA
I_{OL}	Low-level output current	V_{CC} = 4.5 V to 5.5 V		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50		50		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20		20		20	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC[1]		CDx4AC74		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80	119.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		−55°C to 125°C		−40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −50 µA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I_{OH} = −4 mA	3 V	2.58		2.4		2.48		
		I_{OH} = −24 mA	4.5 V	3.94		3.7		3.8		
		I_{OH} = −50 mA [1]	5.5 V			3.85				
		I_{OH} = −75 mA [1]	5.5 V					3.85		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 50 µA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V		0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V		0.36		0.5		0.44	
		I_{OL} = 50 mA [1]	5.5 V				1.65			
		I_{OL} = 75 mA [1]	5.5 V						1.65	
I_I	V_I = V_{CC} or GND		5.5 V		±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V		4		80		40	µA
C_i					10		10		10	pF

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

4.6 Timing Requirements, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V (unless otherwise noted)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			9		10	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	50		44		ns
		CLK	56		49		
t_{su}	Setup time	Data	44		39		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive					ns
t_h	Hold time	Data after CLK ↑	0		0		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑ or $\overline{PRE}$ ↑	34		30		ns

4.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			79		90	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.6		4.9		ns
		CLK	6.3		5.5		
t_{su}	Setup time	Data	4.9		4.3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive					ns
t_h	Hold time	Data after CLK ↑	0		0		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑ or $\overline{PRE}$ ↑	4.7		4.1		ns

4.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			110		125	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4		3.5		ns
		CLK	4.5		3.9		
t_{su}	Setup time	Data	3.5		3.1		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive					ns
t_h	Hold time	Data after CLK ↑	0		0		ns
t_{rec}	Recovery time, before CLK ↑	$\overline{CLR}$ ↑ or $\overline{PRE}$ ↑	2.7		2.4		ns

4.9 Switching Characteristics, V_{CC} = 1.5 V

over recommended operating free-air temperature range, V_{CC} = 1.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			9		10		MHz
t_{PLH}	CLK	Q or $\overline{Q}$		125		114	ns
t_{PHL}				125		114	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$		132		120	ns
t_{PHL}				144		131	

4.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			79		90		MHz

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	14	3.6	12.7	ns
t_{PHL}			3.5	14	3.6	12.7	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.7	14.7	3.8	13.4	ns
t_{PHL}			4	16.1	4.1	14.6	

4.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

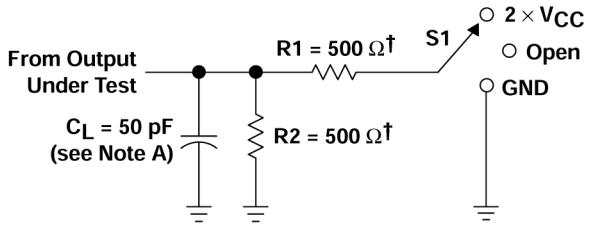
PARAMETER	FROM (INPUT)	TO (OUTPUT)	−55°C to 125°C		−40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			110		125		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	2.5	10	2.6	9.1	ns
t_{PHL}			2.5	10	2.6	9.1	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.6	10.5	2.7	9.5	ns
t_{PHL}			2.9	11.5	3	10.4	

4.12 Operating Characteristics

T_A = 25°C

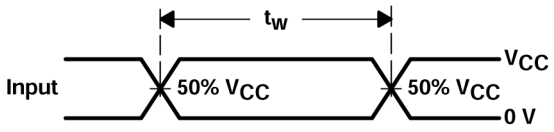
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	55	pF

5 Parameter Measurement Information

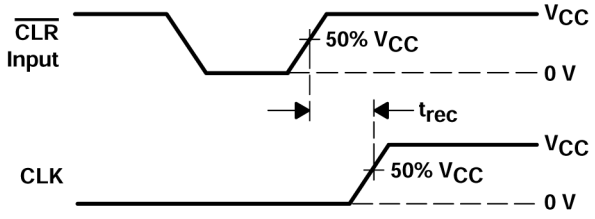


† When V_{CC} = 1.5 V, R1 = R2 = 1 kΩ

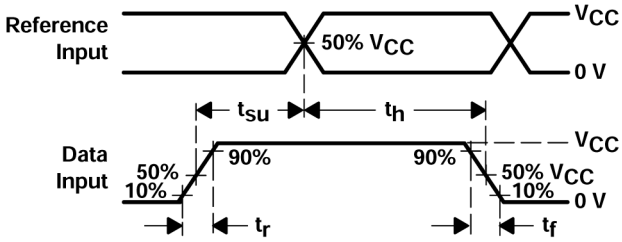
LOAD CIRCUIT



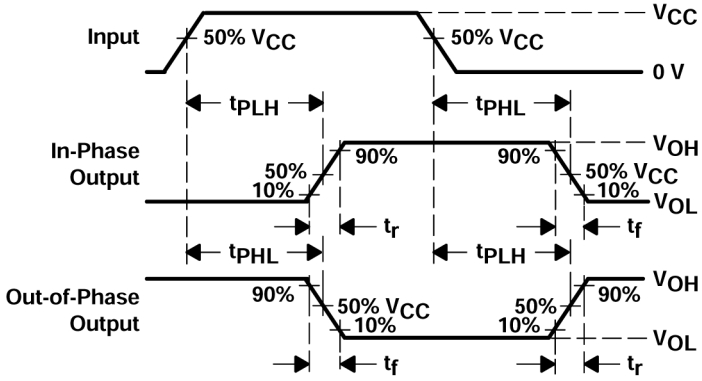
VOLTAGE WAVEFORMS
PULSE DURATION



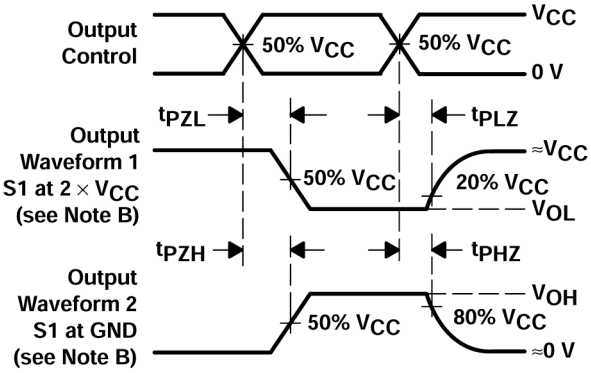
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

图 5-1. Load Circuit and Voltage Waveforms

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

6 Detailed Description

6.1 Overview

The ’AC74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

6.2 Functional Block Diagram

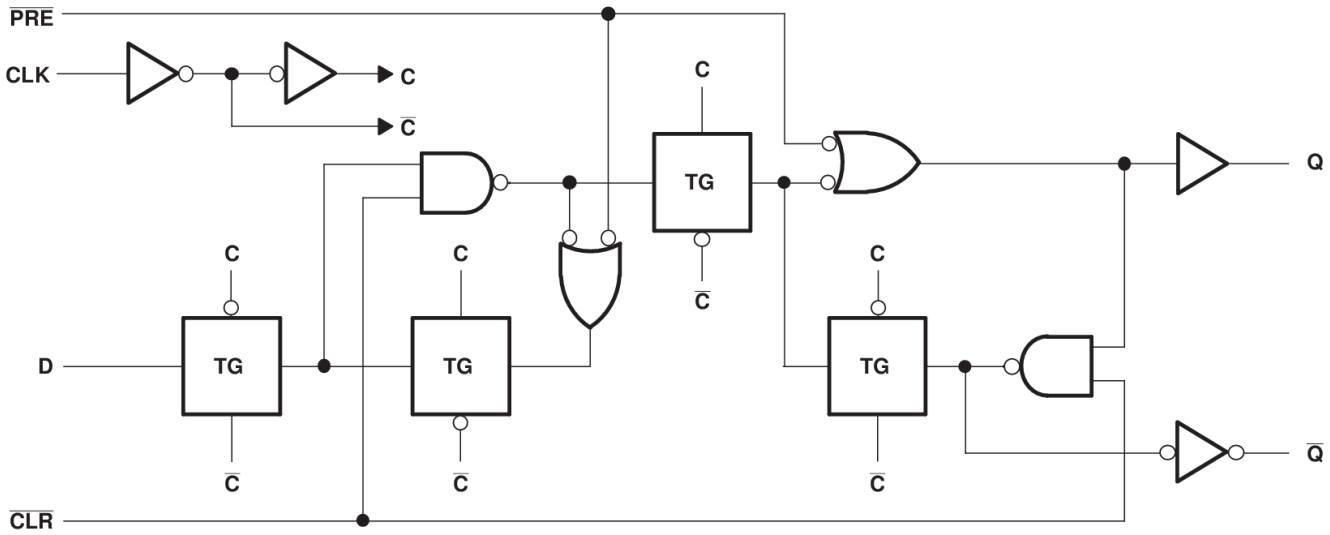


图 6-1.

6.3 Device Functional Modes

表 6-1. Function Table (Each Flip-flop)

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in *节 4.3* .

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

7.1 Layout

7.1.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Example for the CD74AC74 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

7.1.2 Layout Example

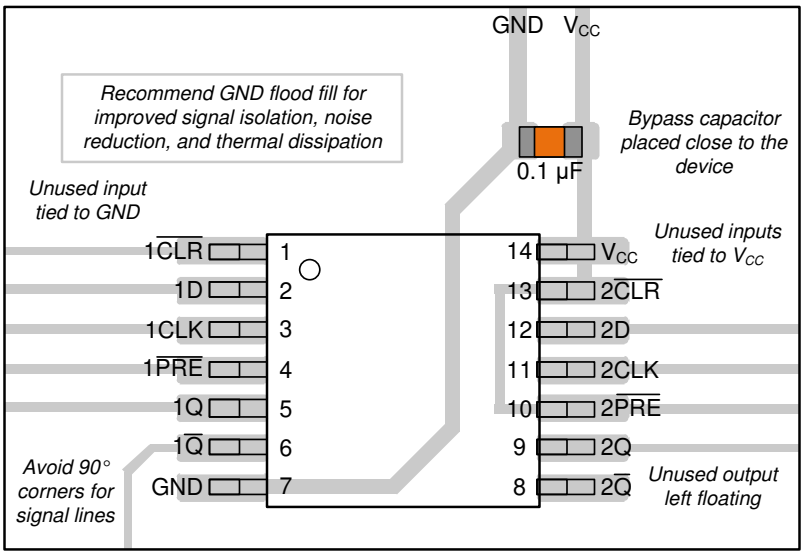


图 7-1. Example layout for the CD74AC74

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC74	Click here	Click here	Click here	Click here	Click here
CD74AC74	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2002) to Revision E (August 2024)	Page
• 添加了*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、*应用和实施* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Updated R θ JA values: D = 86 to 119.9, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC74F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC74F3A
CD74AC74E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC74E
CD74AC74M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	AC74M
CD74AC74M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC74M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC74, CD74AC74 :

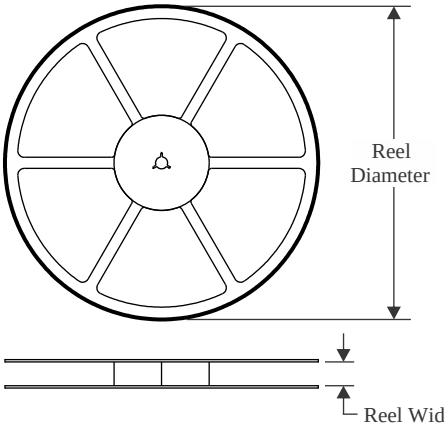
- Catalog : CD74AC74
- Military : CD54AC74

NOTE: Qualified Version Definitions:

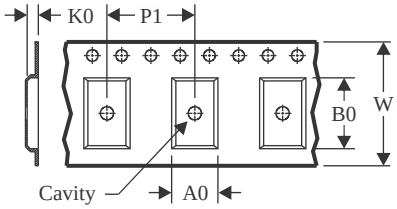
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

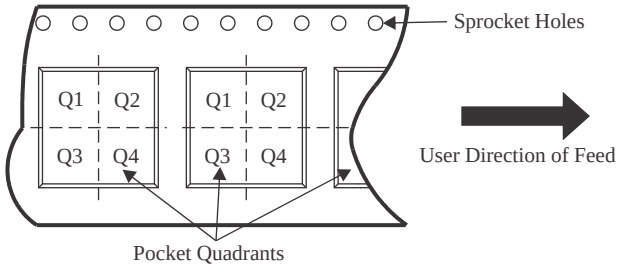


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

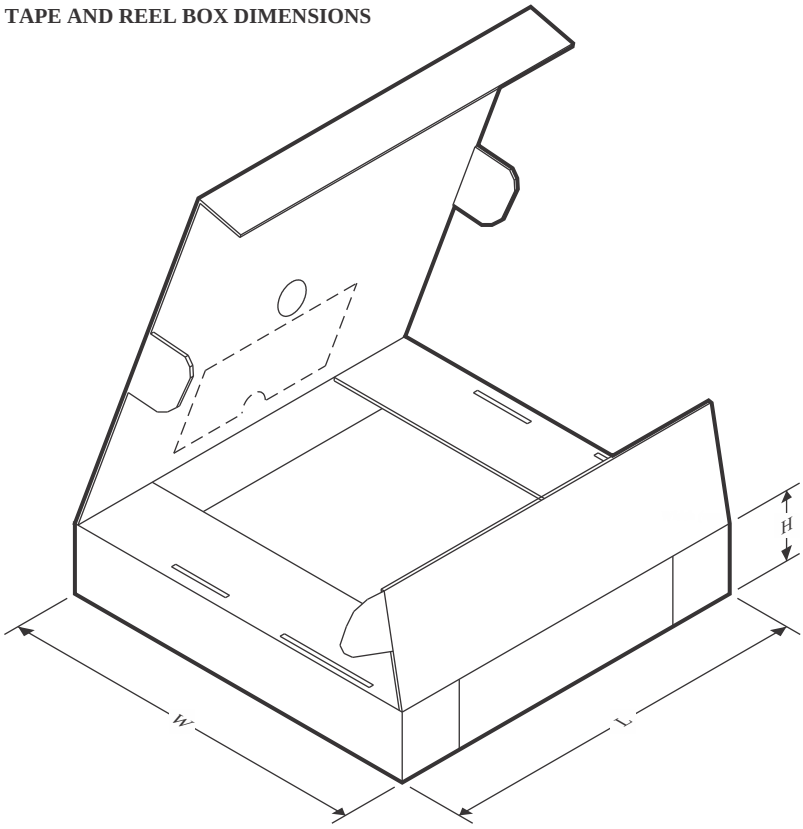
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74AC74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

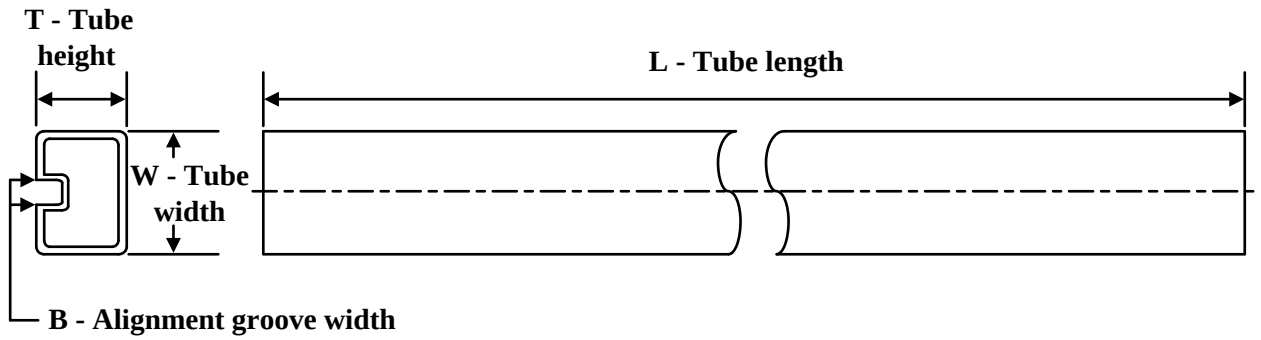
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC74M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74AC74M96	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



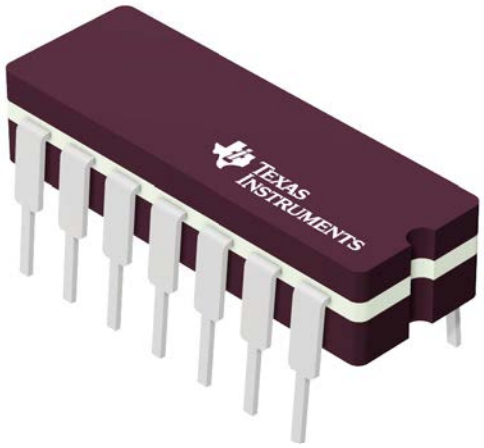
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC74E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC74E	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

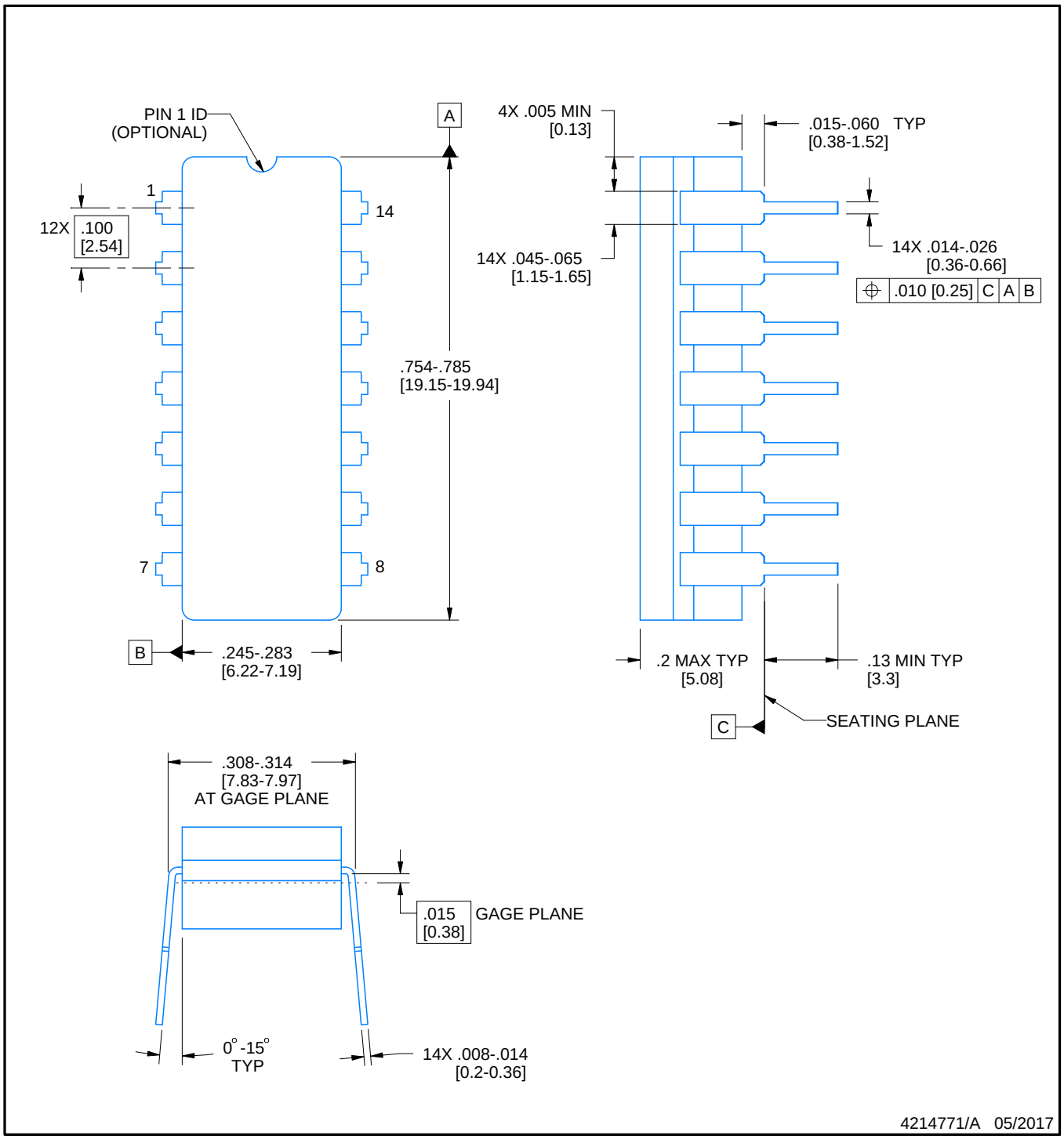
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

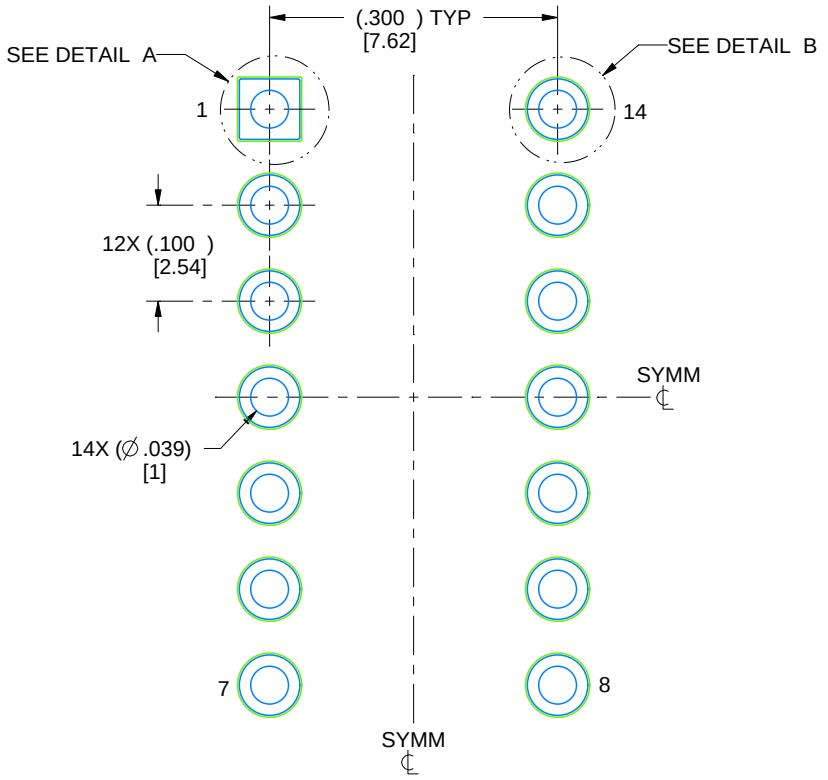
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

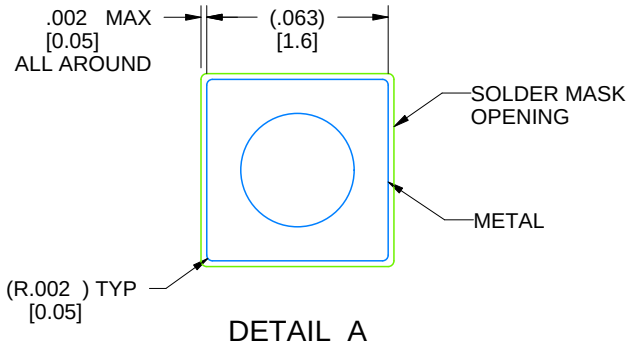
J0014A

CDIP - 5.08 mm max height

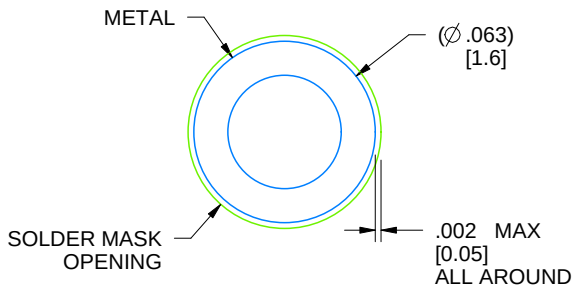
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



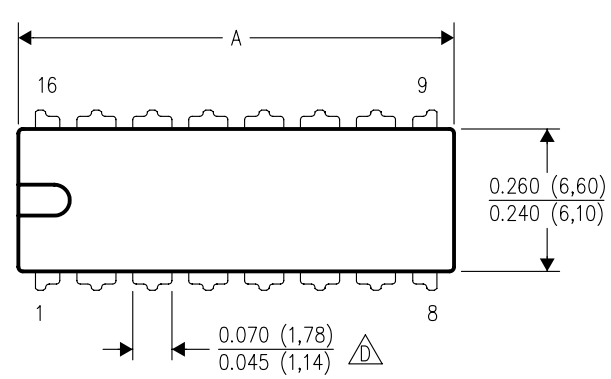
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

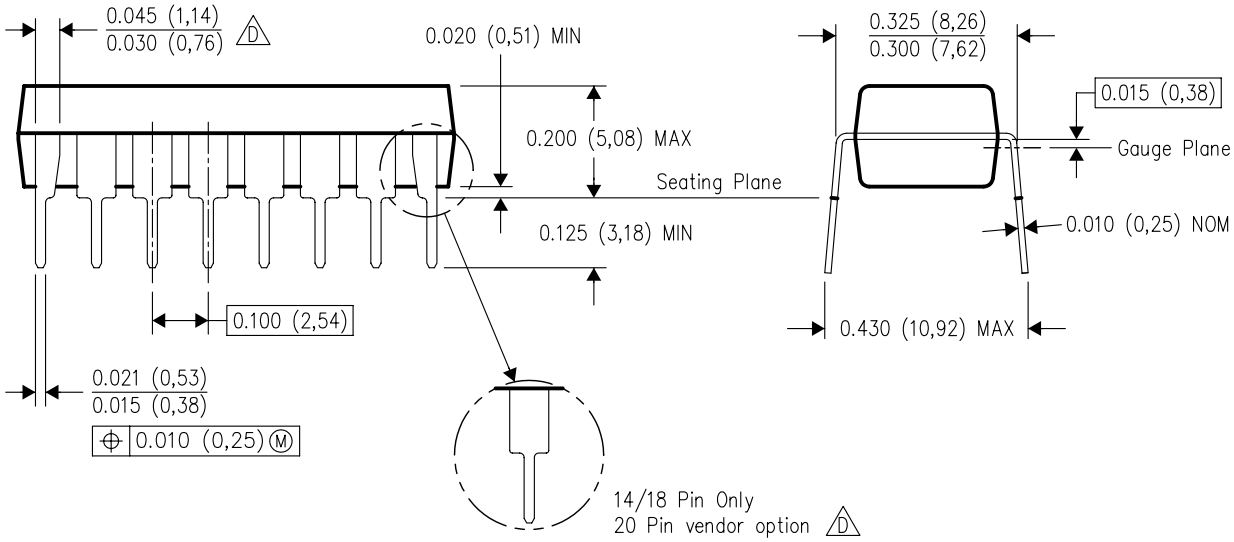
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

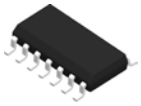


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

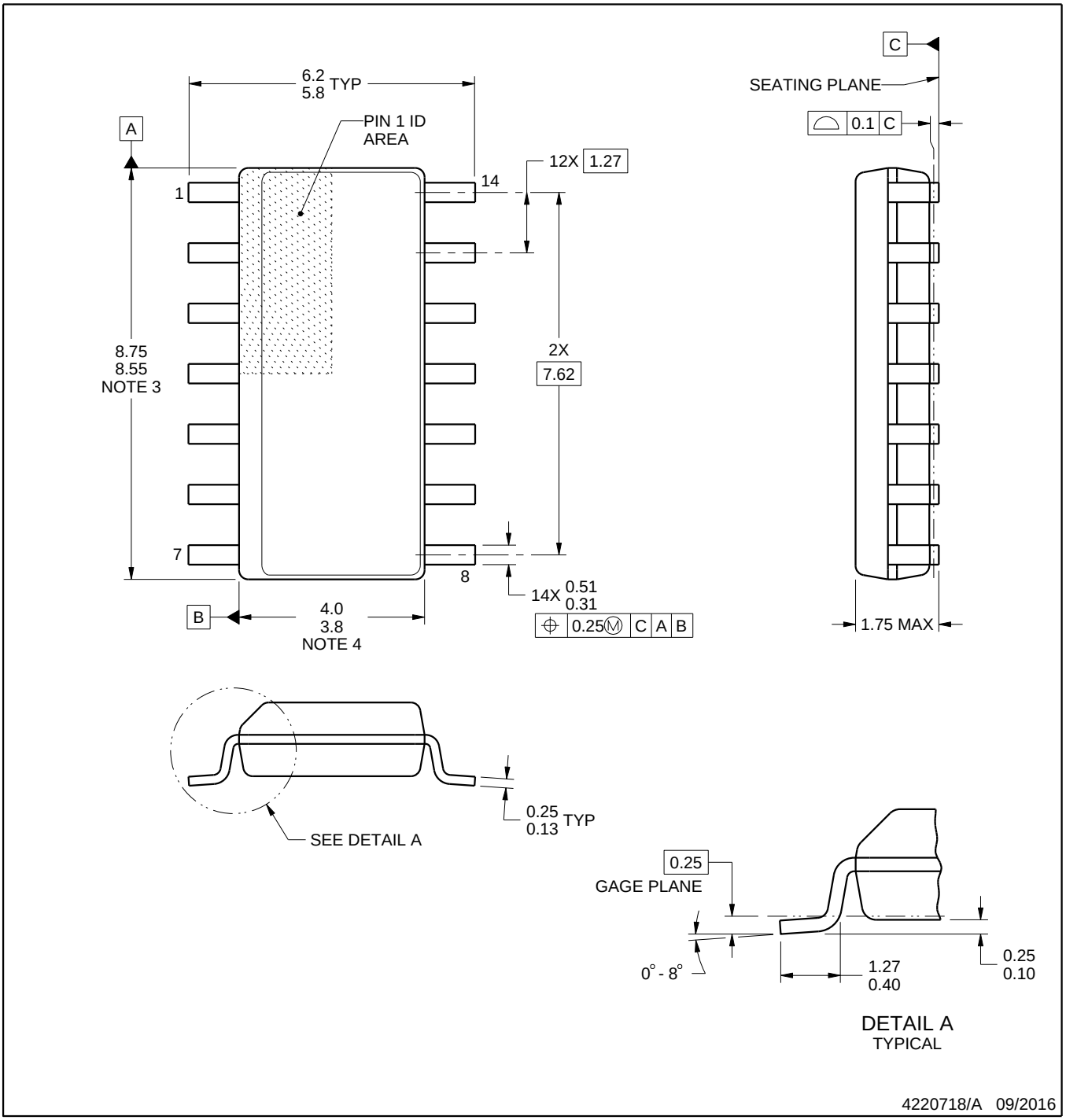


PACKAGE OUTLINE

D0014A

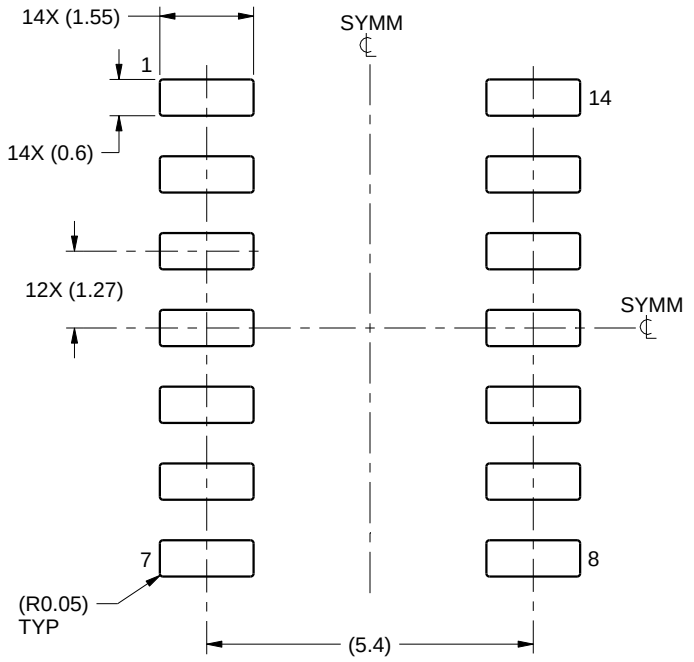
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

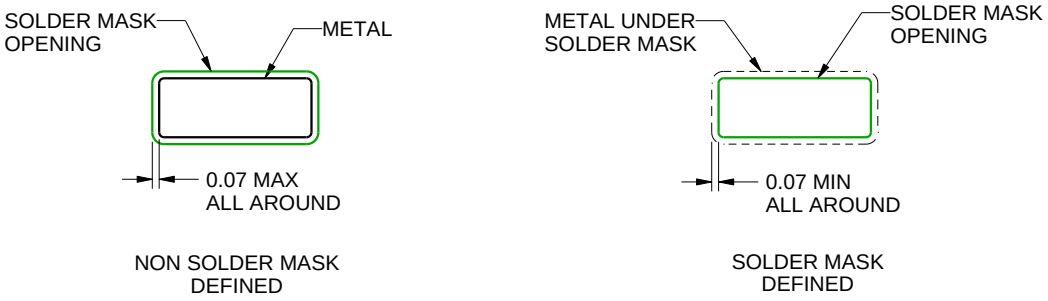


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

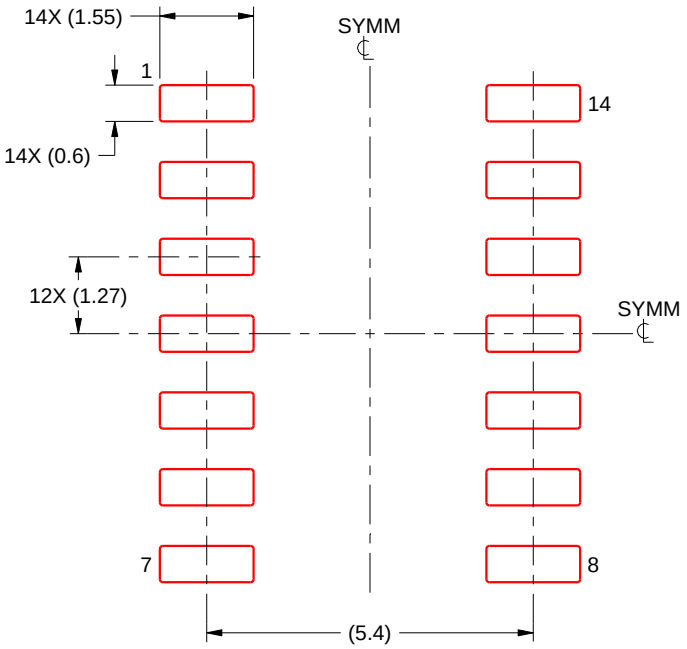
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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