

CMOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

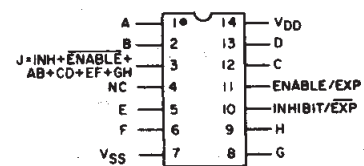
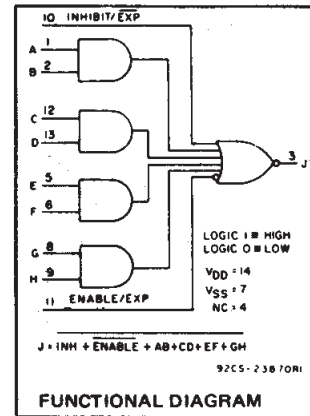
High-Voltage Types (20-Volt Rating)

■ CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/EXP input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/EXP is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig.10 and its associated explanation for applications where a capability greater than 4-wide is required.

The CD4086B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Medium-speed operation – t_{pHL} = 90 ns; t_{pLH} = 140 ns (typ.) at 10 V
- INHIBIT and ENABLE inputs
- Buffered outputs
- 100% tested for quiescent current at 20 V
- Maximum input leakage current of 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at V_{DD} = 5 V
 - 2 V at V_{DD} = 10 V
 - 2.5 V at V_{DD} = 15 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



92CS-23869R1
Top View
TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	-0.5V to +20V
Voltages referenced to V _{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 Inch (1.59 ± 0.79mm) from case for 10s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)	3	18	V

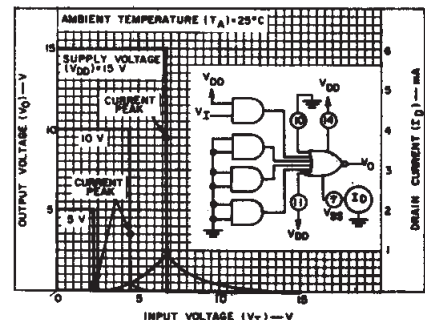


Fig. 1 – Typical voltage and current transfer characteristics.

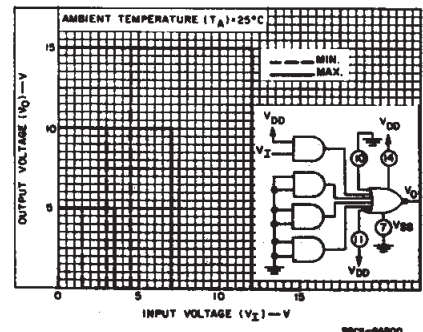


Fig. 2 – Minimum and maximum voltage transfer characteristics.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4086B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	—	0.5	5	1	1	30	30	—	0.02	1	μA
	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05			—			0	V
	—	0.10	10	0.05			—			0	
	—	0.15	15	0.05			—			0	
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95			4.95			5	V
	—	0.10	10	9.95			9.95			10	
	—	0.15	15	14.95			14.95			15	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5			—			1.5	V
	1.9	—	10	3			—			3	
	1.5, 13.5	—	15	4			—			4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5			3.5			—	V
	1.9	—	10	7			7			—	
	1.5, 13.5	—	15	11			11			—	
Input Current, I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

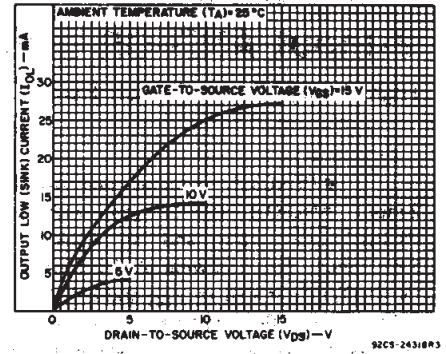


Fig. 3 - Typical output low (sink) current characteristics.

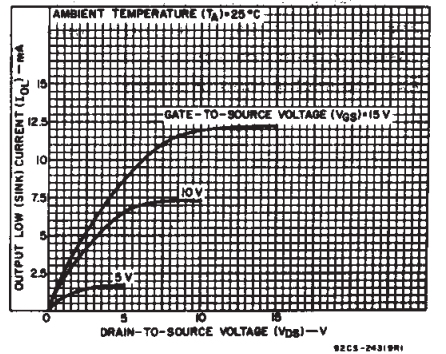


Fig. 4 - Minimum output low (sink) current characteristics.

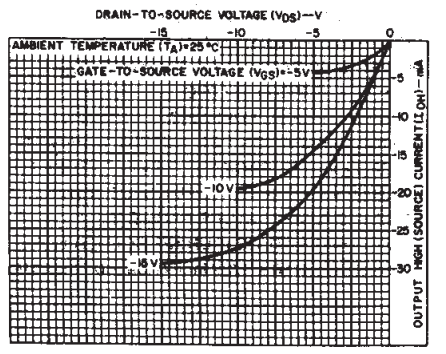


Fig. 5 - Typical output high (source) current characteristics.

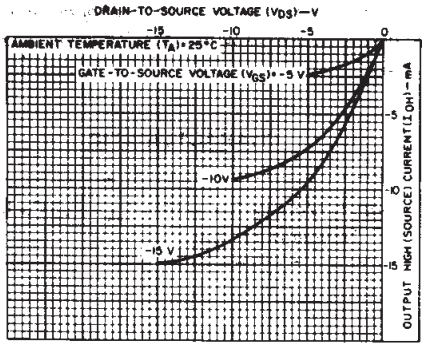


Fig. 8 - Minimum output high (source) current characteristics.

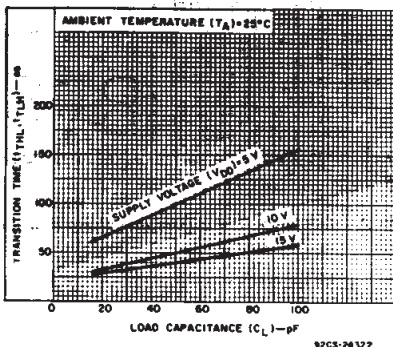


Fig. 6 - Typical transition time vs. load capacitance.

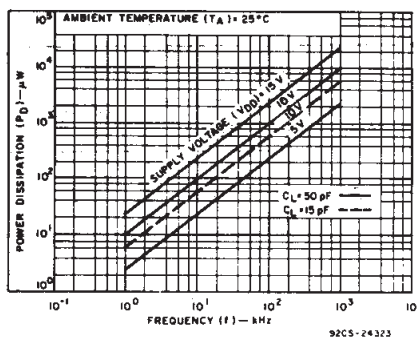


Fig. 7 - Typical power dissipation vs. frequency.

CD4086B Types

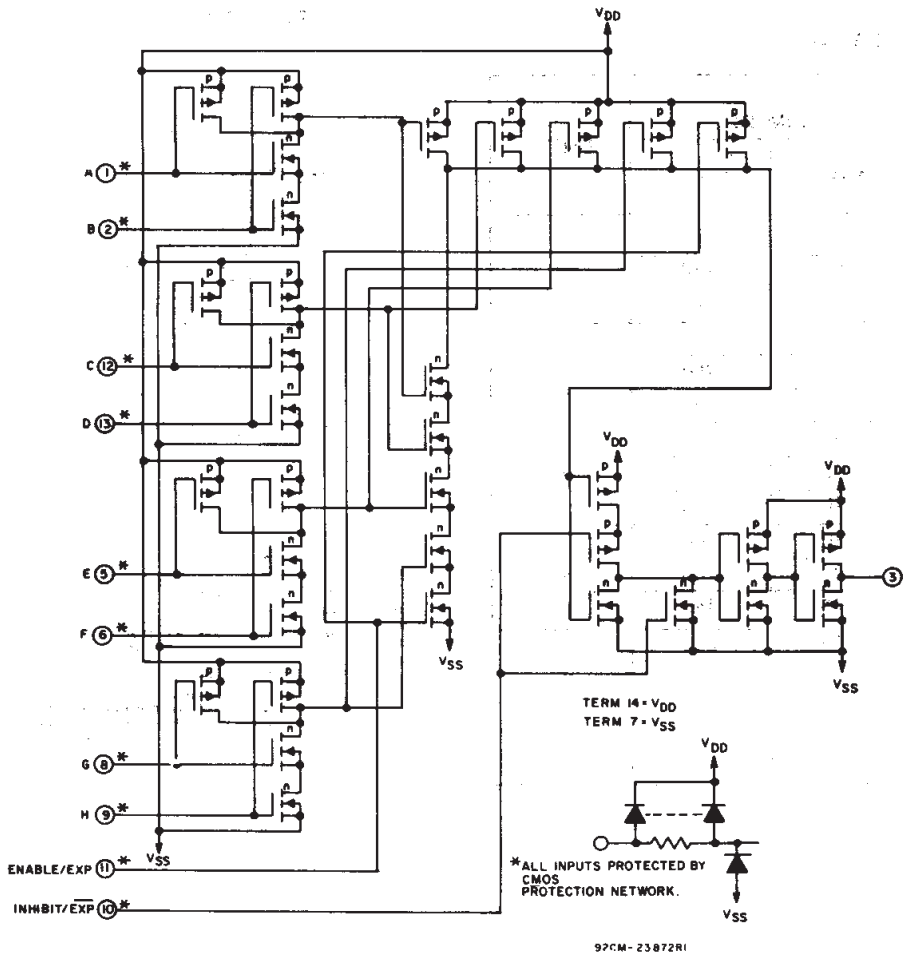


Fig. 9 - CD4086B schematic diagram.

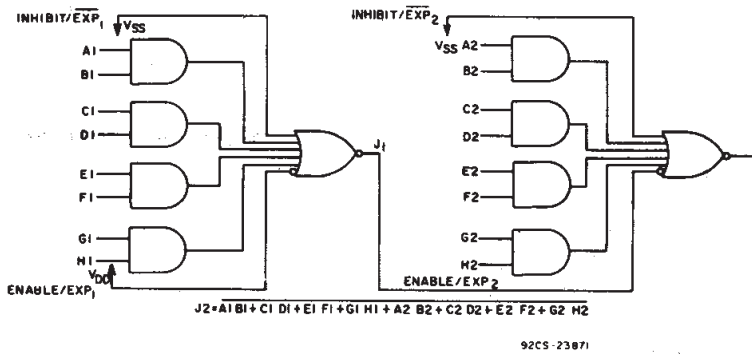


Fig. 10 - Two CD4086's connected as an 8-wide 2-input A-O-I gate.

Fig. 10 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any

NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/EXP input with the same result.

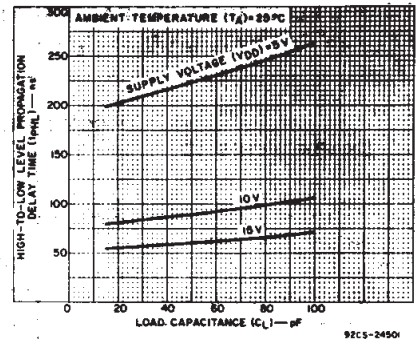


Fig. 11 - Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

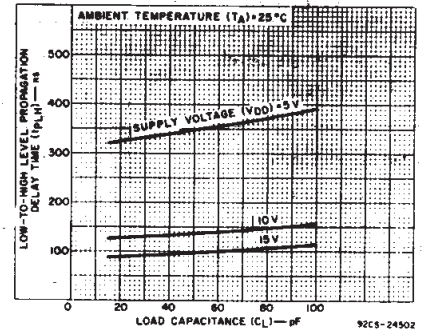


Fig. 12 - Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

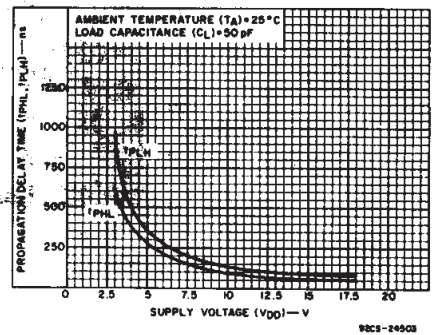


Fig. 13 - Typical DATA or ENABLE propagation delay time vs. supply voltage.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4086B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS	
		V_{DD} (V)	TYP.		MAX.
Propagation Delay Time (Data): High-to-Low Level, t_{pHL}		5	225	450	ns
		10	90	180	
		15	60	120	
Low-to-High Level, t_{pLH}		5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{pHL(INH)}$		5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level, $t_{pLH(INH)}$		5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance C_{iN}	Any Input		5	7.5	pF

TEST CIRCUITS

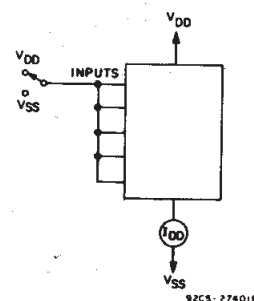


Fig. 14 - Quiescent device current.

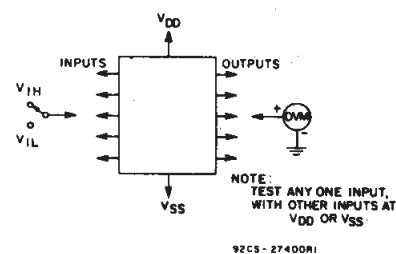
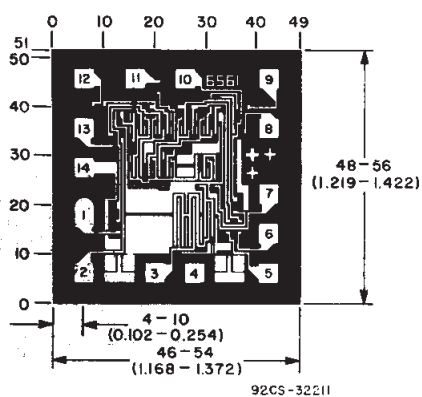


Fig. 15 - Input voltage.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and Pad Layout for the CD4086BH

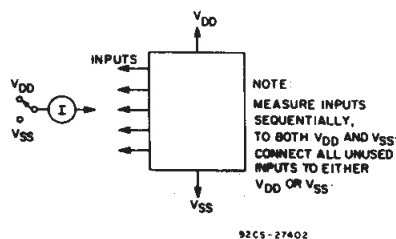


Fig. 16 - Input leakage current.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4086BE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4086BE
CD4086BF3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4086BF3A
CD4086BM	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4086BM
CD4086BMT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4086BM

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4086B, CD4086B-MIL :

- Catalog : [CD4086B](#)
- Military : [CD4086B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4086BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4086BMT	SOIC	D	14	250	210.0	185.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4086BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4086BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4086BM	D	SOIC	14	50	506.6	8	3940	4.32

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated