

## CD405xB 具有逻辑电平转换功能的 CMOS 单路 8 通道 模拟多路复用器或多路信号分离器

### 1 特性

- 各种数字和模拟信号电平：
  - 数字：3V 至 20V
  - 模拟： $\leq 20V_{P-P}$
- 单电源范围：3V 至 20V ( $V_{DD} < 3V$  时，性能会下降)
- 双电源范围： $\pm 3V$  至  $\pm 10V$
- 在  $V_{DD} = 15V$  时，输入范围内的低导通电阻为  $125\Omega$  (典型值)
- 在  $V_{DD} = 15V$  时，低通道漏电流为  $\pm 10pA$  (典型值)
- 低静态功耗： $0.2\mu W$  (典型值)
- 先断后合开关消除了通道重叠
- 双向信号路径
- ESD 保护 HBM：3000V，CDM：2000V
- 与业界通用 4051 多路复用器兼容的引脚

### 2 应用

- 模拟和数字多路复用和多路信号分离
- 模数和数模转换
- 信号门控
- 工厂自动化
- 电视
- 电器
- 消费类音频
- 可编程逻辑电路
- 传感器

### 3 说明

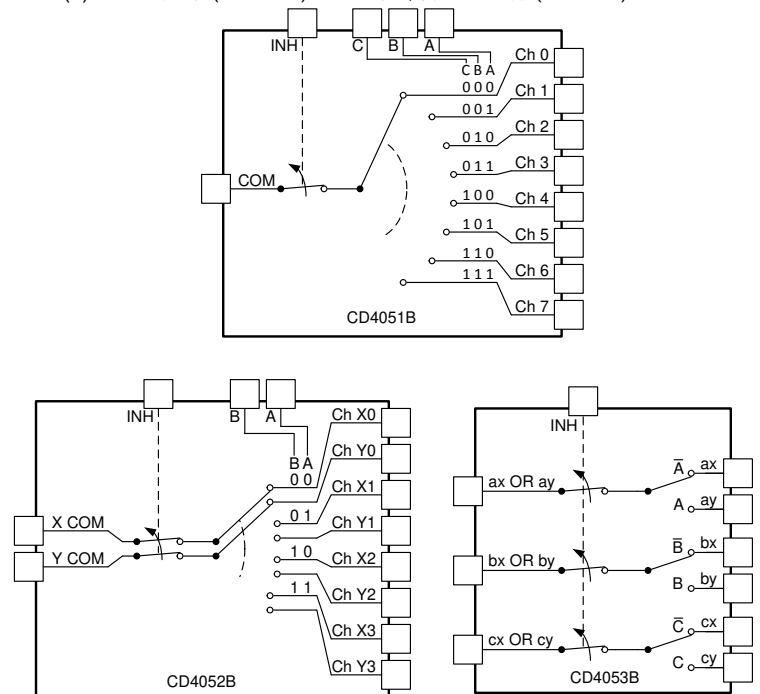
CD405xB 模拟多路复用器和多路信号分离器是数字控制的模拟开关，具有低接通阻抗和极低的关断漏电流。这些多路复用器电路在整个  $V_{DD} - V_{SS}$  和  $V_{DD} - V_{EE}$  电源电压范围内，消耗的静态功率极低，而不受控制信号的逻辑状态影响。

#### 封装信息

器件型号	封装 (1)	封装尺寸 (2)
CD405xB	J (CDIP, 16)	19.50mm × 6.92mm
	N (PDIP, 16)	19.3mm × 9.4mm
	D (SOIC, 16)	9.9mm × mm
	NS (SOP, 16)	10.2mm × 7.8mm
	PW (TSSOP, 16)	5mm × 6.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



CD4051B 的功能图



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## 4 Pin Configuration and Functions

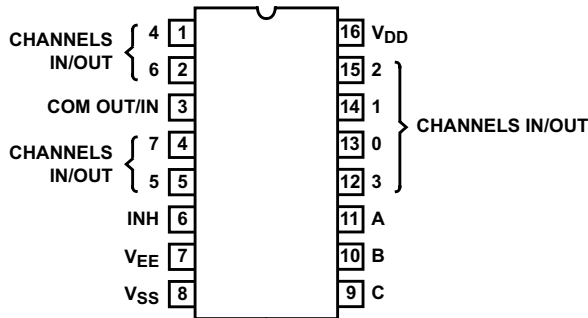


图 4-1. CD4051B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

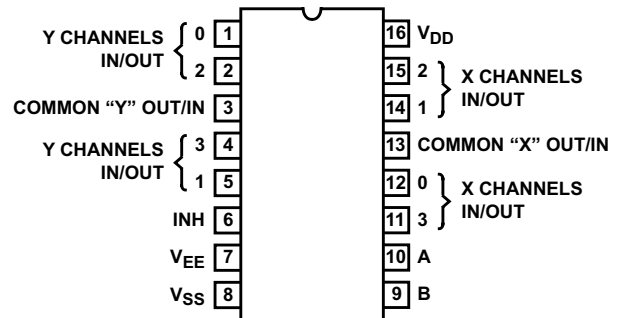


图 4-2. CD4052B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

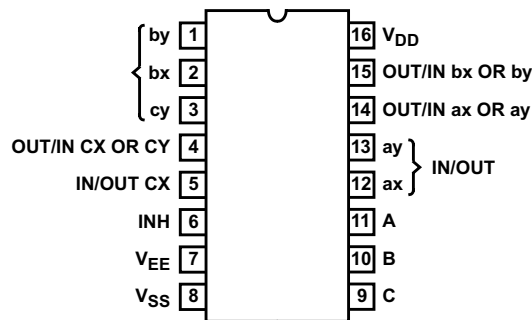


图 4-3. CD4053B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOP, and TSSOP (Top View)

表 4-1. Pin Functions CD4051B

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V <sub>EE</sub>	—	Negative power input
8	V <sub>SS</sub>	—	Ground
9	C	I	Channel select C. See 表 7-1.
10	B	I	Channel select B. See 表 7-1.
11	A	I	Channel select A. See 表 7-1.
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V <sub>DD</sub>	—	Positive power input

(1) I = input, O = output

表 4-2. Pin Functions CD4052B

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V <sub>EE</sub>	—	Negative power input
8	V <sub>SS</sub>	—	Ground
9	B	I	Channel select B. See 表 7-1.
10	A	I	Channel select A. See 表 7-1.
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V <sub>DD</sub>	—	Positive power input

(1) I = input, O = output

表 4-3. Pin Functions CD4053B

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See 表 7-1.
7	V <sub>EE</sub>	—	Negative power input
8	V <sub>SS</sub>	—	Ground
9	C	I	Channel select C. See 表 7-1.
10	B	I	Channel select B. See 表 7-1.
11	A	I	Channel select A. See 表 7-1.
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V <sub>DD</sub>	—	Positive power input

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

			MIN	MAX	UNIT
	Supply Voltage	V+ to V-, Voltages Referenced to V <sub>SS</sub> Terminal	- 0.5	20	V
	DC Input Voltage		- 0.5	V <sub>DD</sub> +0.5	V
	DC Input Current	Any One Input	- 10	10	mA
T <sub>JMAX1</sub>	Maximum junction temperature, ceramic package			175	°C
T <sub>JMAX2</sub>	Maximum junction temperature, plastic package			150	°C
T <sub>stg</sub>	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±2000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Temperature Range	- 55		125	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD405x				UNIT
		E (PDIP)	M (SOIC)	NS (SOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	67	73	64	116.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Electrical Characteristics

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100 \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT				
<b>SIGNAL INPUTS (<math>V_{IS}</math>) AND OUTPUTS (<math>V_{OS}</math>)</b>													
	$V_{IS}$ (V)	$V_{EE}$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)	TEMP								
Quiescent Device Current, $I_{DD}$ Max	0V	0V	0V	5V	- 55°C			60	$\mu A$				
					- 40°C			60					
					25°C		17	60					
					85°C			150					
					125°C			150					
					0V	0V	0V	10V		- 55°C			60
										- 40°C			60
										25°C		18	60
										85°C			300
										125°C			300
	0V	0V	0V	15V	- 55°C			60					
					- 40°C			60					
					25°C		18	60					
					85°C			600					
					125°C			600					
	0V	0V	0V	20V	- 55°C			100					
					- 40°C			100					
					25°C		18	100					
					85°C			3000					
					125°C			3000					
Drain to Source ON Resistance $r_{ON}$ Max $0 \leq V_{IS} \leq V_{DD}$	0V	0V	0V	5V	- 55°C			800	$\Omega$				
					- 40°C			850					
					25°C		470	1050					
					85°C			1200					
					125°C			1300					
	0V	0V	0V	10V	- 55°C			310					
					- 40°C			300					
					25°C		180	400					
					85°C			520					
					125°C			550					
	0V	0	0	15V	- 55°C			200					
					- 40°C			210					
					25°C		125	240					
					85°C			300					
					125°C			300					
Change in ON Resistance (Between Any Two Channels), $\Delta R_{ON}$	0V	0V	5V	25°C			15	$\Omega$					
			10V			10							
			15V			5							

## 5.5 Electrical Characteristics (续)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)		0V	0V	18V	- 55°C		± 100	nA	
					- 40°C		± 100		
					25°C	± 0.3	± 100 <sup>(2)</sup>		
					85°C		± 1000 <sup>(2)</sup>		
					125°C		± 1000 <sup>(2)</sup>		
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)		5 or 0	- 5V	0V	10.5V	85°C	± 300	nA	
		5	0V	0V	18V	85°C	± 300		
Capacitance	Input, $C_{IS}$	0V	0V	10V	25°C	5		pF	
	Output, $C_{OS}$					CD4051	30		
	Output, $C_{OS}$					CD4052	18		
	Output, $C_{OS}$					CD4053	9		
	Feed through, $C_{IOS}$						0.2		
Prop Delay		$V_{DD}$	$R_L = 200k\ \Omega$		5V	25°C	30	60	ns
			$C_L = 50pF$		10V		15	30	
			$t_r, t_f = 20ns$		15V		10	20	

### 5.5 Electrical Characteristics (续)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100\ \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
<b>CONTROL (ADDRESS OR INHIBIT), <math>V_C</math></b>									
Input Low Voltage, $V_{IL}$ , Max					5V	- 55°C	0.8	V	
						- 40°C	0.8		
						25°C	0.8		
						85°C	0.8		
						125°C	0.8		
						10V	- 55°C		0.8
							- 40°C		0.8
							25°C		0.8
							85°C		0.8
							125°C		0.8
						15V	- 55°C		0.8
							- 40°C		0.8
							25°C		0.8
							85°C		0.8
							125°C		0.8
Input High Voltage, $V_{IH}$ , Min					5V	- 55°C	3.5	V	
						- 40°C	3.5		
						25°C	3.5		
						85°C	3.5		
						125°C	3.5		
						10V	- 55°C		7
							- 40°C		7
							25°C		7
							85°C		7
							125°C		7
						15V	- 55°C		11
							- 40°C		11
							25°C		11
							85°C		11
							125°C		11
Input current, $I_{IN}$ (Max)					18V	- 55°C	$\pm 1$	$\mu A$	
						- 40°C	$\pm 1$		
						25°C	$\pm 0.6$		
						85°C	$\pm 1$		
						125°C	$\pm 1$		
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15)	$t_r, t_f = 20ns$ , $C_L = 50pF$ , $R_L = 10k\ \Omega$	0V	0V	5V	450	720	ns	
			0V	0V	10V	160	320		
			0V	0V	15V	120	240		
			- 5V	0V	5V	225	450		



## 5.5 Electrical Characteristics (续)

Over operating free-air temperature range,  $V_{SUPPLY} = \pm 5V$ , and  $R_L = 100 \Omega$ , (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11)	$t_r, t_f = 20ns,$ $C_L = 50pF,$ $R_L = 1k \Omega$	0V	0V	5V		400	720	ns
			0V	0V	10V		160	320	
			0V	0V	15V		120	240	
			- 10V	0V	5V		200	400	
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17)	$t_r, t_f = 20ns,$ $C_L = 50pF,$ $R_L = 10k \Omega$	0V	0V	5V		200	450	ns
			0V	0V	10V		90	210	
			0V	0V	15V		70	160	
			- 10V	0V	5V		130	300	
Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input)			- 5V	0V	5V	25°C	5	7.5	pF

- (1) Peak-to-Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$ .  
 (2) Determined by minimum feasible leakage measurement for automatic testing.

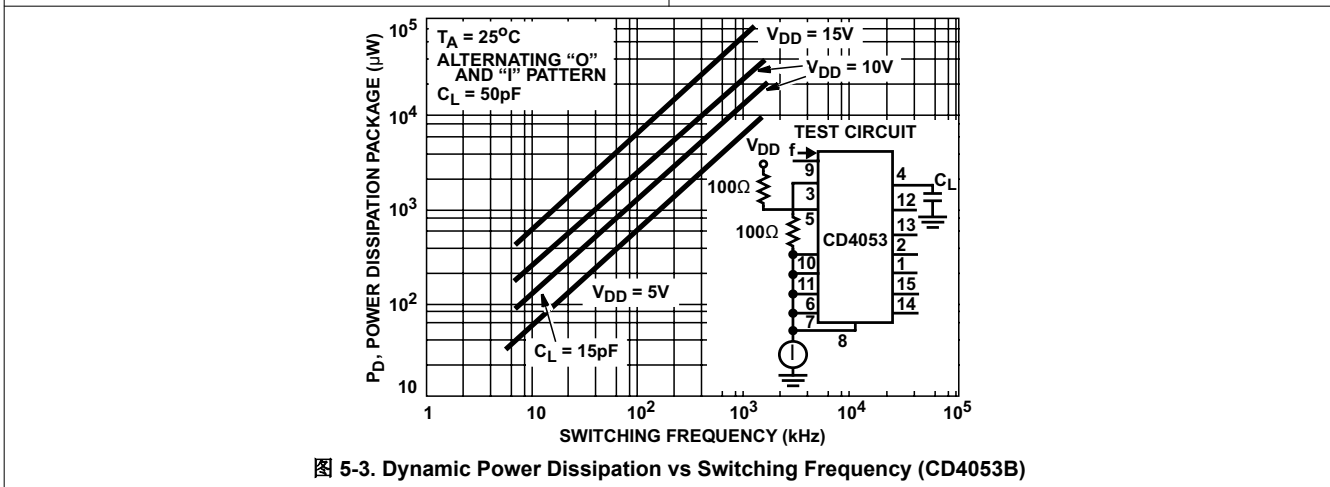
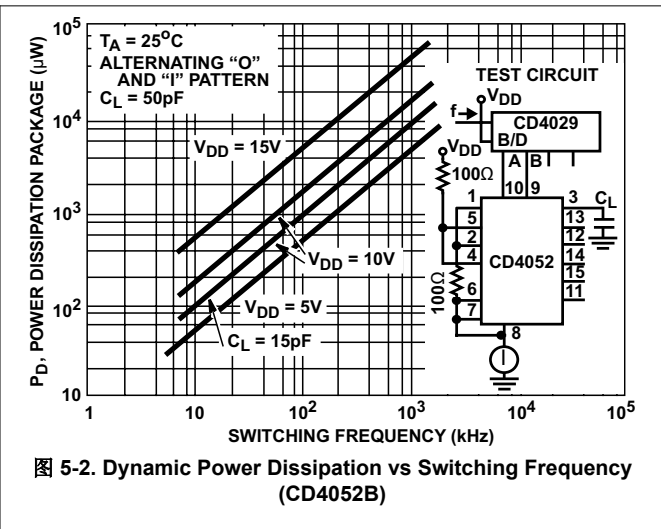
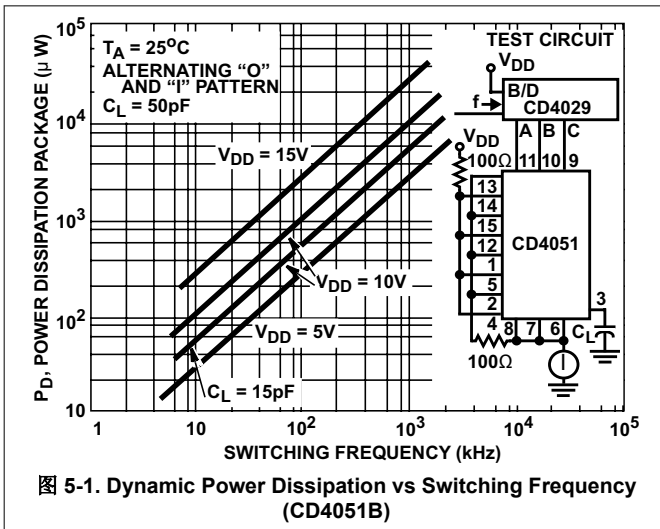
### 5.6 AC Performance Characteristics

$V_{DD} = +15V, V_{SS} = V_{EE} = 0V, T_A = 25^\circ C$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP	UNIT					
	$V_{IS}$ (V)	$V_{DD}$ (V)	$R_L$ (k $\Omega$ )							
Cutoff ( - 3dB) Frequency Channel ON (Sine Wave Input)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4053	30	MHz			
		10	1		CD4052	25				
		10	1		CD4051	20				
	$V_{EE} = V_{SS}, 20\text{Log}(V_{OS}/V_{IS}) = -3\text{dB}$			$V_{OS}$ at Any Channel		60				
Total Harmonic Distortion, THD	2 <sup>(1)</sup>	5	10			0.3%	%			
	3 <sup>(1)</sup>	10	10			0.2%				
	5 <sup>(1)</sup>	15	10			0.12%				
	$V_{EE} = V_{SS}, f_{IS} = 1\text{kHz Sine Wave}$									
- 40dB Feedthrough Frequency (All Channels OFF)	5 <sup>(1)</sup>	10	1	$V_{OS}$ at Common OUT/IN	CD4053	8	MHz			
					CD4052	10				
					CD4051	12				
	$V_{EE} = V_{SS}, 20\text{Log}(V_{OS}/V_{IS}) = -40\text{dB}$			$V_{OS}$ at Any Channel		8				
- 40dB Signal Crosstalk Frequency	5 <sup>(1)</sup>	10	1			3	MHz			
						$V_{EE} = V_{SS}, 20\text{Log}(V_{OS}/V_{IS}) = -3\text{dB}$		Between Sections, CD4052 Only	Measured on Common	6
									Measured on Any Channel	10
						$V_{EE} = V_{SS}, 20\text{Log}(V_{OS}/V_{IS}) = -3\text{dB}$		Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5
									In Pin 15, Out Pin 14	6
Address-or-Inhibit-to- Signal Crosstalk		10	10 <sup>(2)</sup>			65	mV <sub>PEAK</sub>			
						$V_{EE} = 0, V_{SS} = 0, t_r, t_f = 20\text{ns}, \text{mVPEAK}$ $V_{CC} = V_{DD} - V_{SS}$ (Square Wave)	65	mV <sub>PEAK</sub>		

- (1) Peak-to-Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$ .
- (2) Both ends of channel.

### 5.7 Typical Characteristics



### 6 Parameter Measurement Information

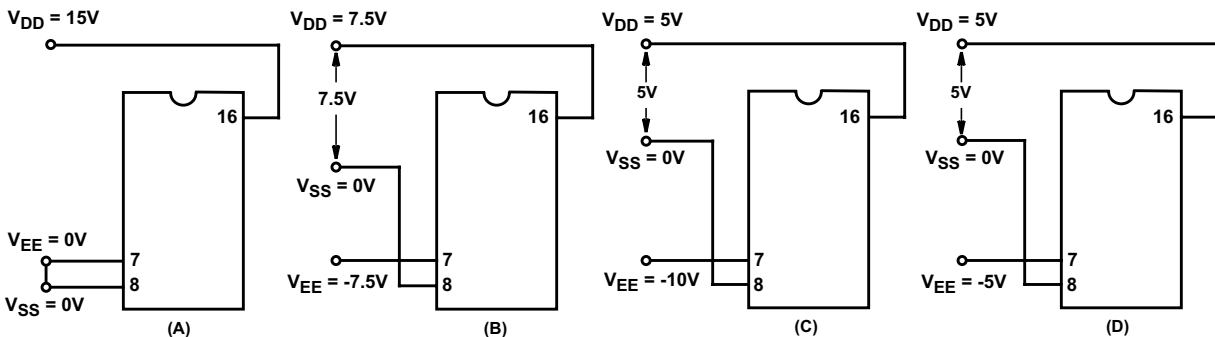


图 6-1. Typical Bias Voltages

备注

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V<sub>SS</sub> and 1 = V<sub>DD</sub>. The analog signal (through the TG) may swing from V<sub>EE</sub> to V<sub>DD</sub>.

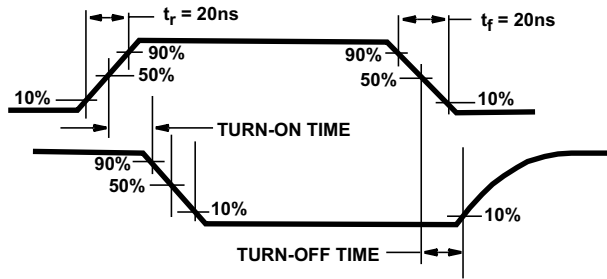


图 6-2. Waveforms, Channel Being Turned ON ( $R_L = 1k\Omega$ )

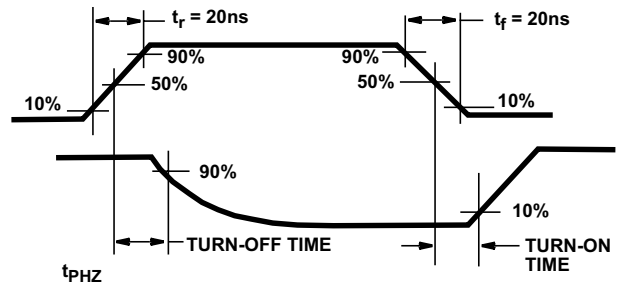


图 6-3. Waveforms, Channel Being Turned OFF ( $R_L = 1k\Omega$ )

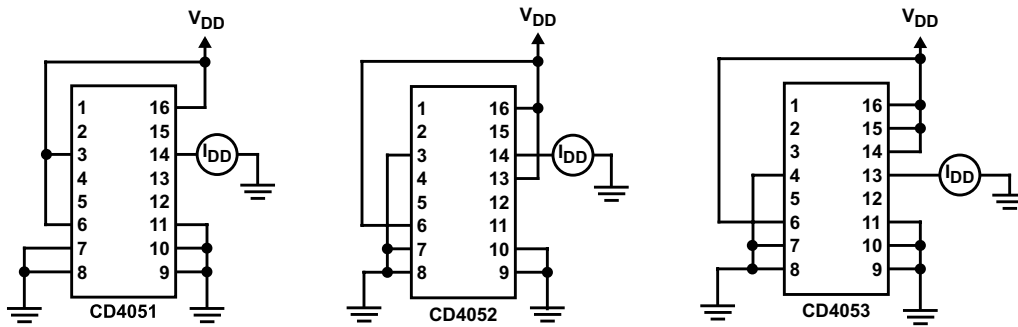
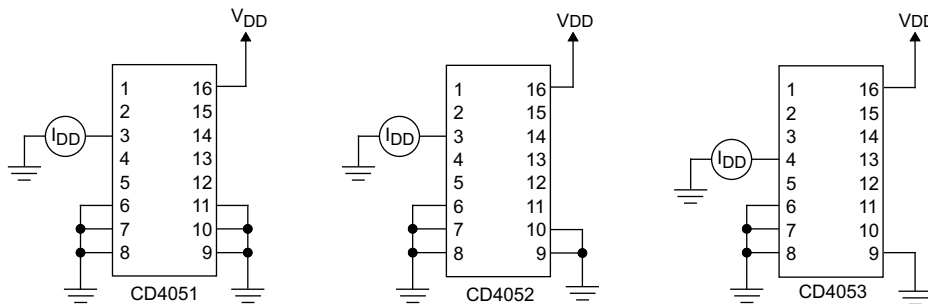


图 6-4. OFF Channel Leakage Current - Any Channel OFF



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图 6-5. On Channel Leakage Current - Any Channel On

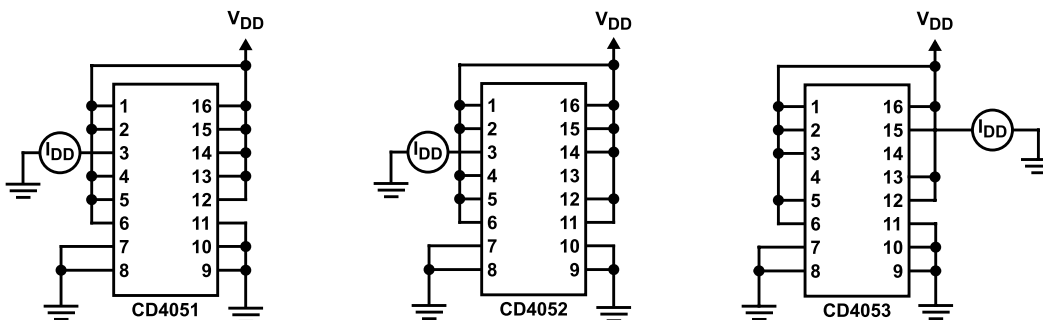


图 6-6. OFF Channel Leakage Current - All Channels OFF

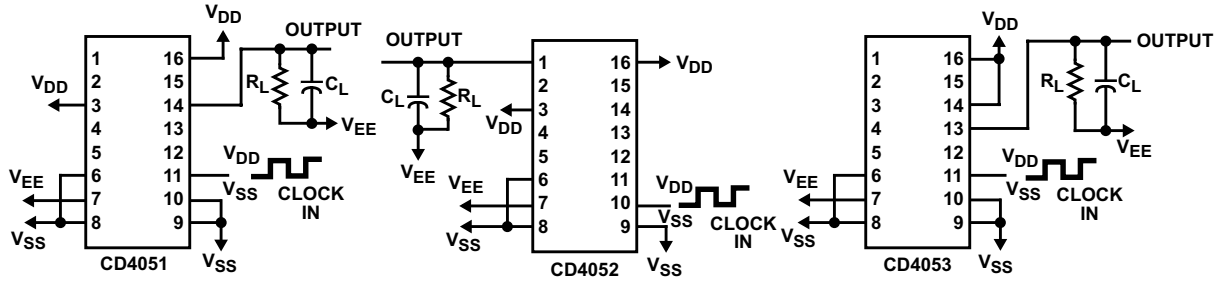


图 6-7. Propagation Delay - Address Input to Signal Output

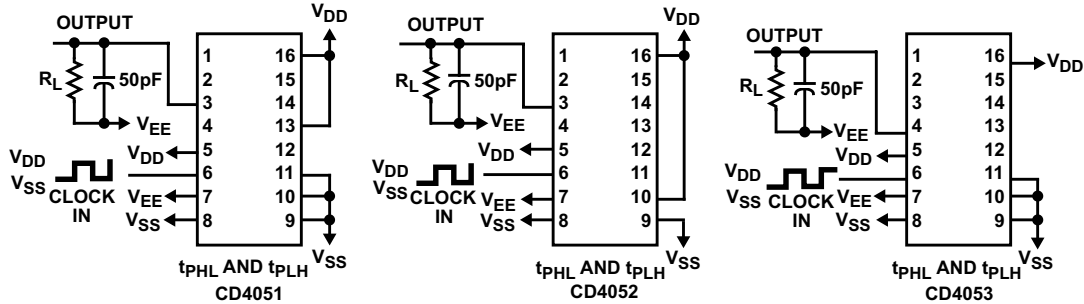


图 6-8. Propagation Delay - Inhibit Input to Signal Output

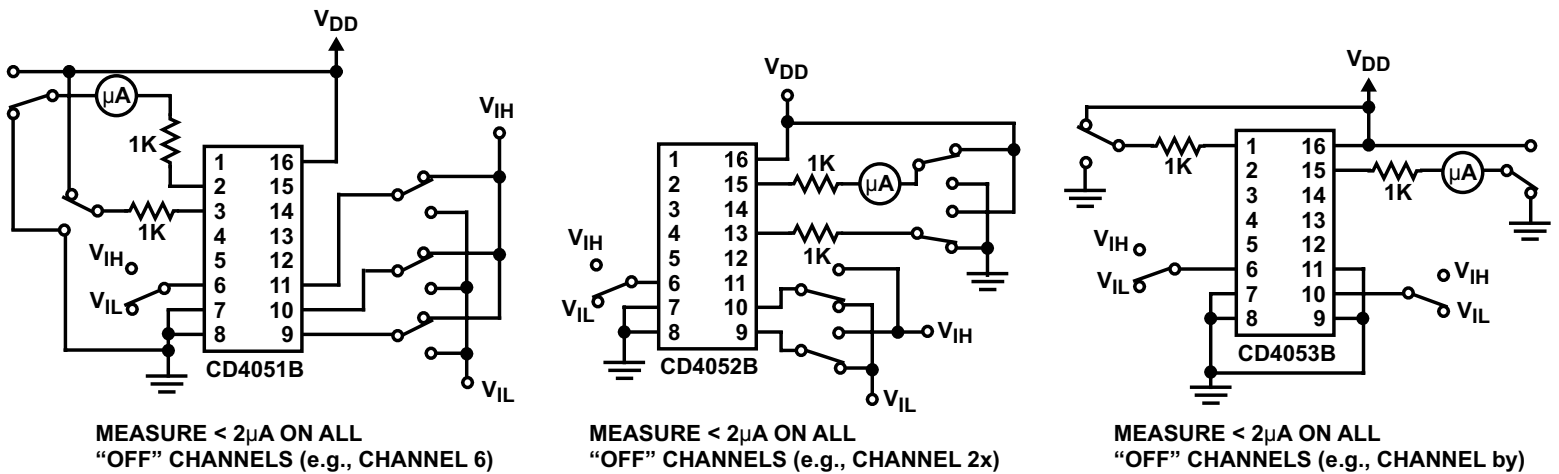


图 6-9. Input Voltage Test Circuits (Noise Immunity)

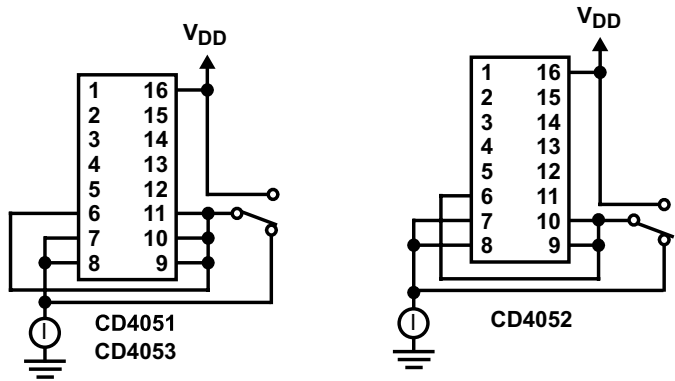


图 6-10. Quiescent Device Current

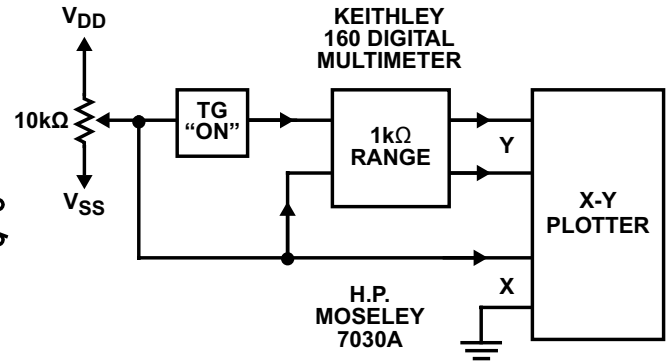


图 6-11. Channel ON Resistance Measurement Circuit

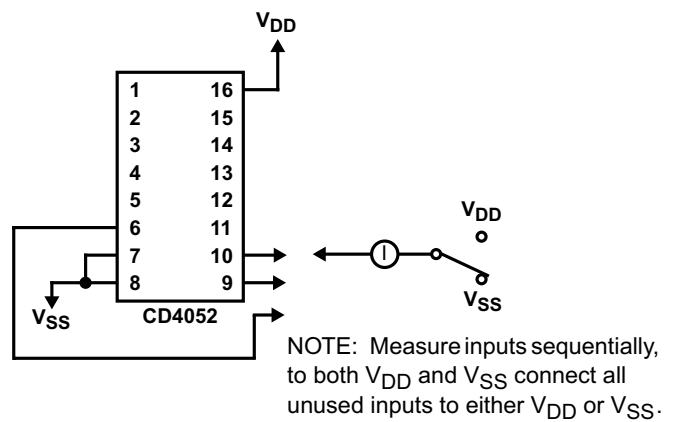
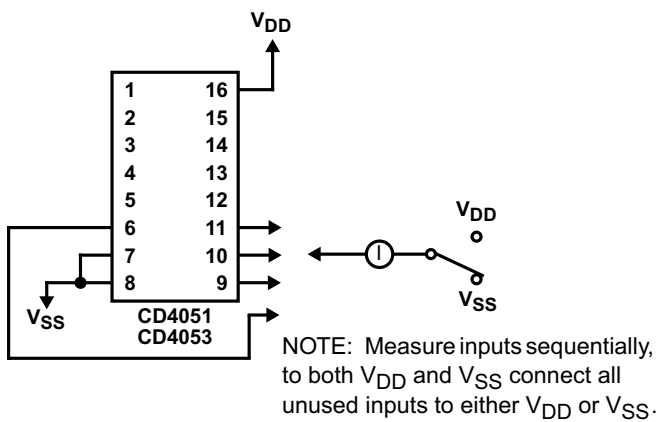


图 6-12. Input Current

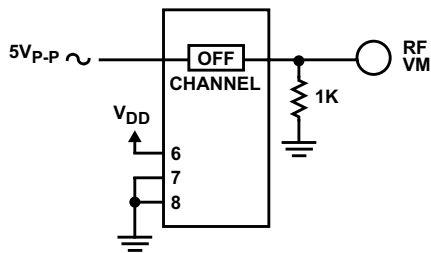


图 6-13. Feed-Through (All Types)

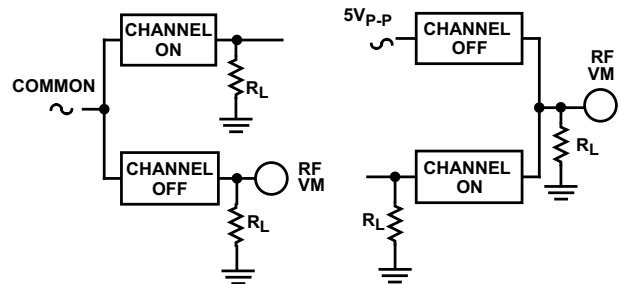
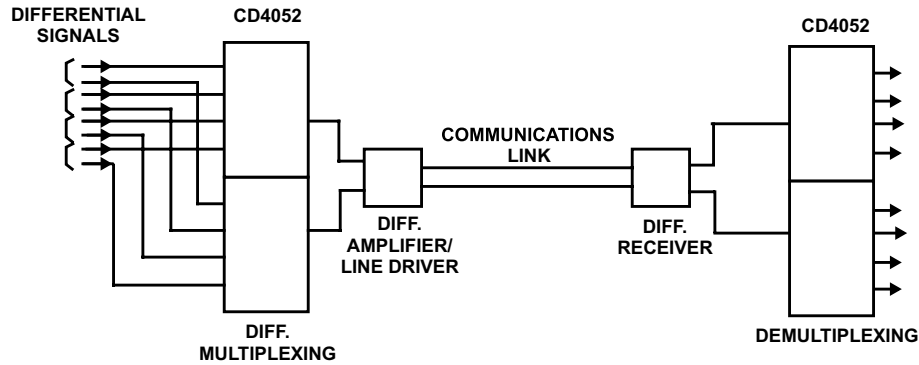


图 6-14. Crosstalk Between Any Two Channels (All Types)



图 6-15. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)



**Special Considerations:** In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

图 6-16. Typical Time-Division Application of the CD4052B

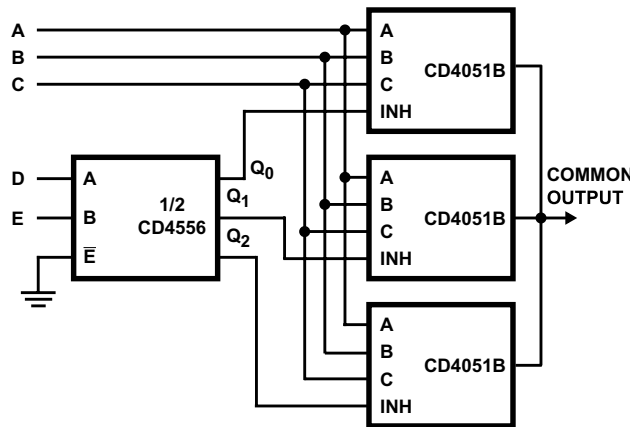


图 6-17. 24-to-1MUX Addressing

## 7 Detailed Description

### 7.1 Overview

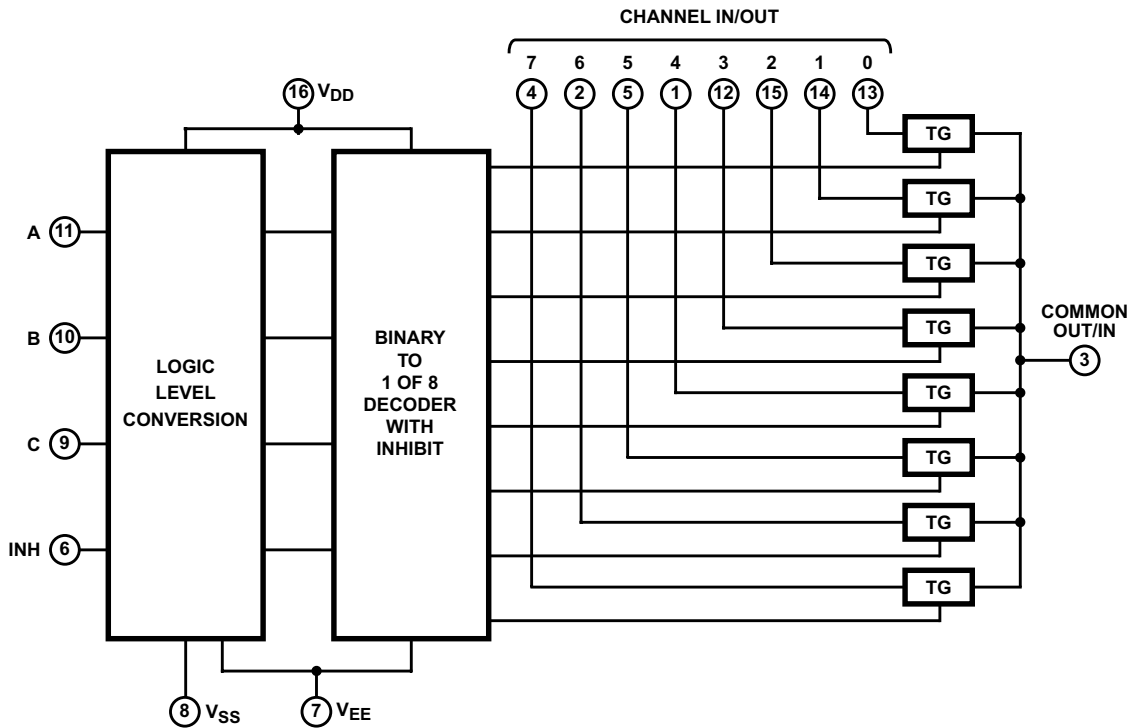
The CD4051B device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B device is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

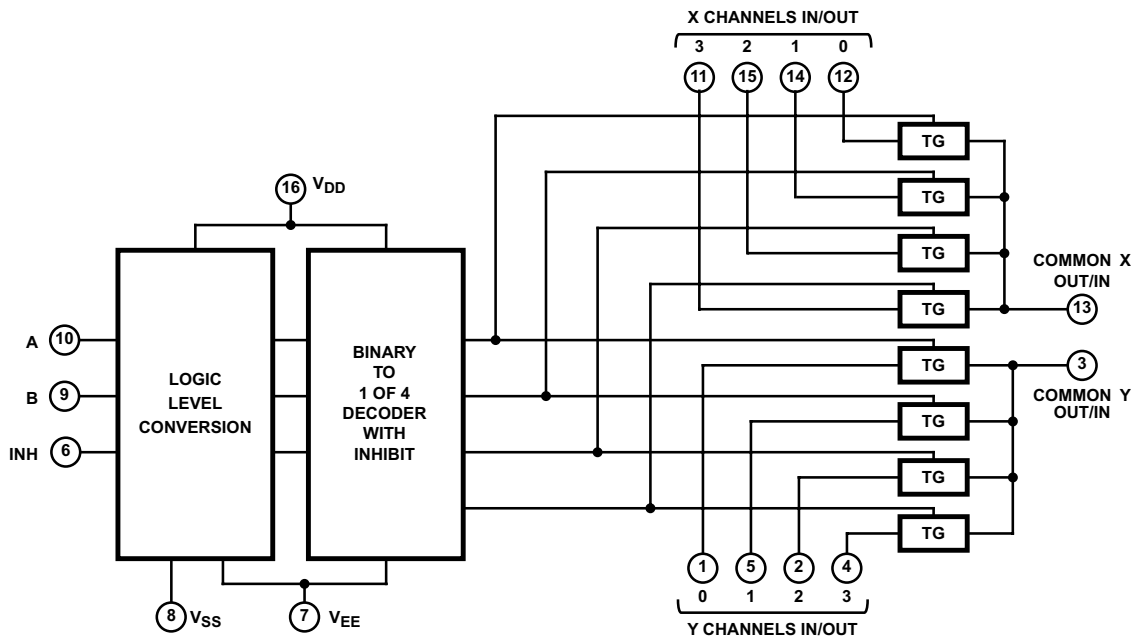
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

## 7.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

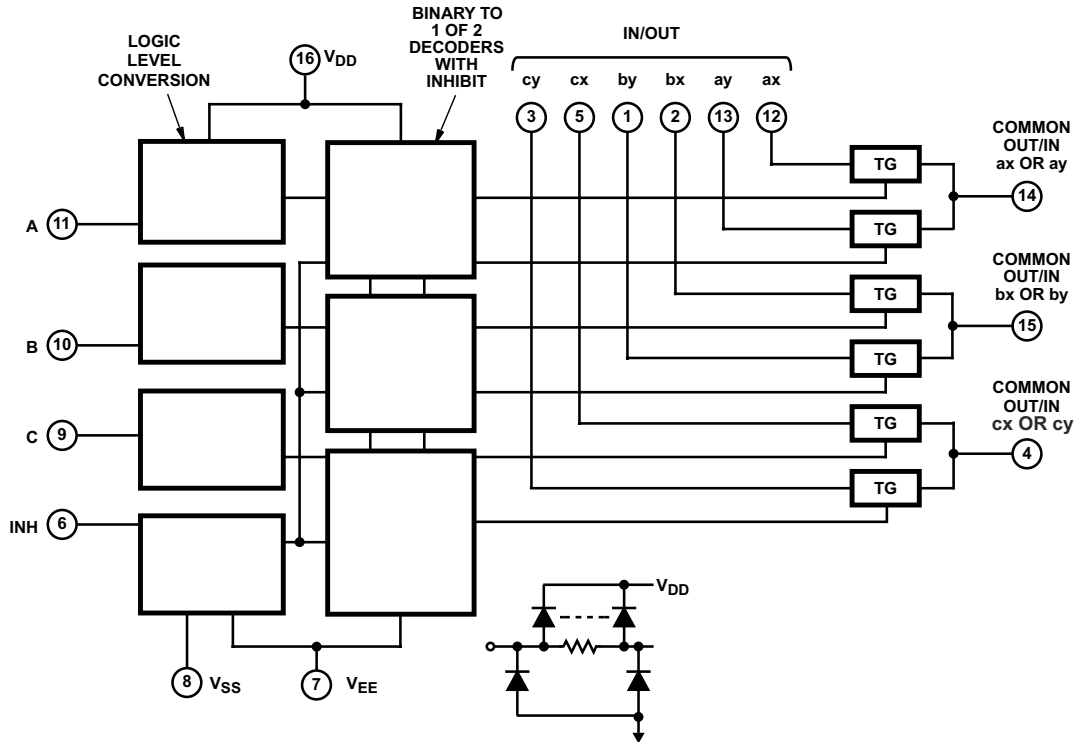
图 7-1. Functional Block Diagram, CD4051B



All inputs are protected by standard CMOS protection network.

图 7-2. Functional Block Diagram, CD4052B





All inputs are protected by standard CMOS protection network.

图 7-3. Functional Block Diagram, CD4053B

### 7.3 Feature Description

The CD405xB line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3V to 20V, and analog signals are accepted at levels  $\leq 20V$ . The devices have low ON resistance, typically  $125\Omega$  over  $15V_{P-P}$  signal input range for  $V_{DD} - V_{EE} = 18V$ . This feature allows for very little signal loss through the switch.

The CD405xB devices also have high OFF resistance, which keeps from the devices from wasting power when the switch is in the OFF position, with typical channel leakage of  $\pm 100pA$  at  $V_{DD} - V_{EE} = 18V$ .

Binary address decoding on the chip makes channel selection simple. When channels are changed, a break-before-make system eliminates channel overlap.

## 7.4 Device Functional Modes

表 7-1. Truth Table <sup>(1)</sup>

INPUT STATES				ON CHANNEL(S)
INHIBIT	C	B	A	
<b>CD4051B</b>				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
<b>CD4052B</b>				
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
<b>CD4053B</b>				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1) X = Do not care

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The CD405xB multiplexers and demultiplexers can be used for a wide variety of applications.

### 8.2 Typical Application

One application of the CD4051B is to use it in conjunction with a microcontroller to poll a keypad. 图 8-1 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

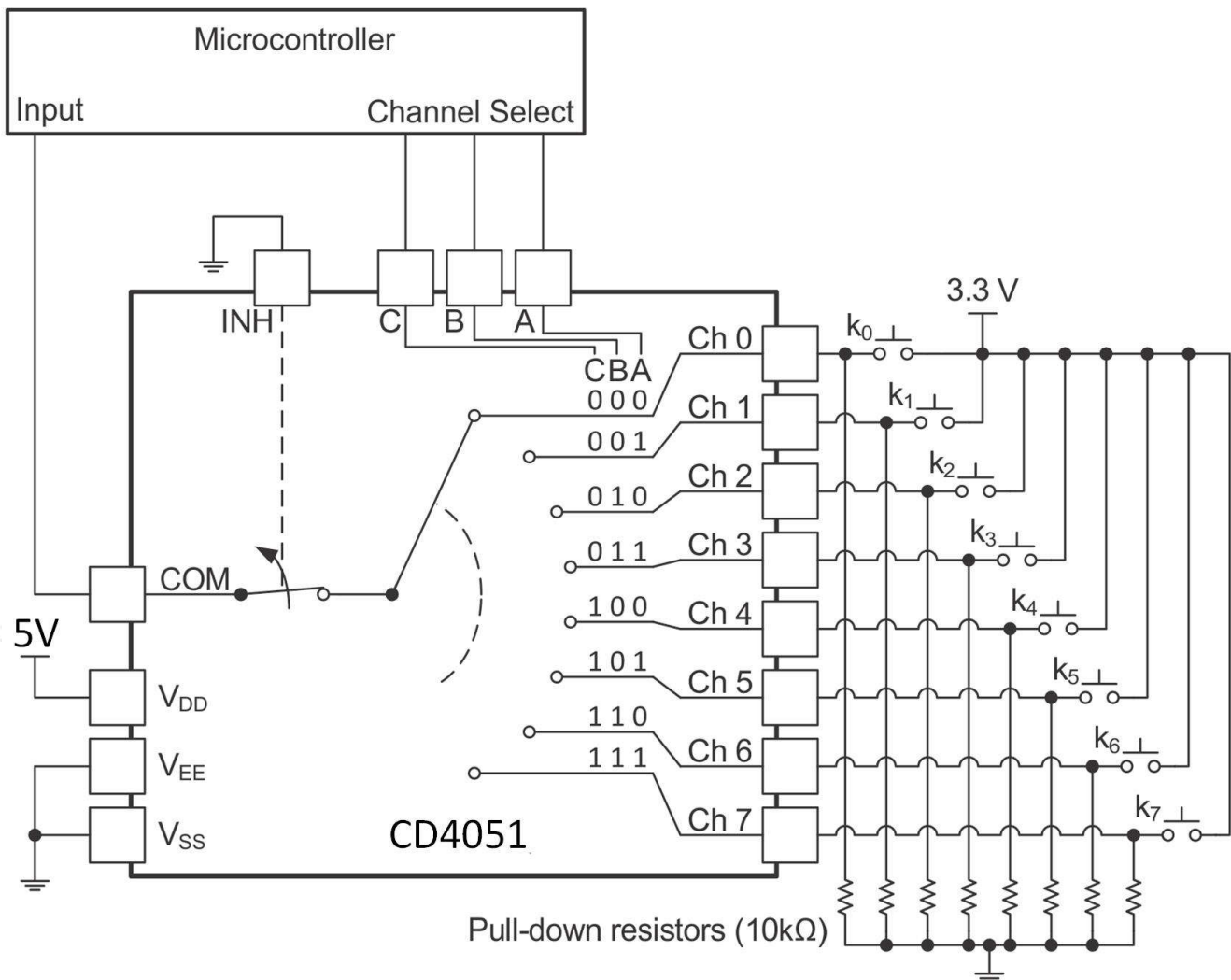


图 8-1. The CD4051B Being Used to Help Read Button Presses on a Keypad

### 8.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
  - For switch time specifications, see propagation delay times in [Electrical Characteristics](#).
  - Inputs should not be pushed more than 0.5V above  $V_{DD}$  or below  $V_{EE}$ .
  - For input voltage level specifications for control inputs, see  $V_{IH}$  and  $V_{IL}$  in [Electrical Characteristics](#).
- Recommended Output Conditions:
  - Outputs should not be pulled above  $V_{DD}$  or below  $V_{EE}$ .
- Input or output current consideration:
  - The CD405xB series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

### 8.2.3 Application Curve

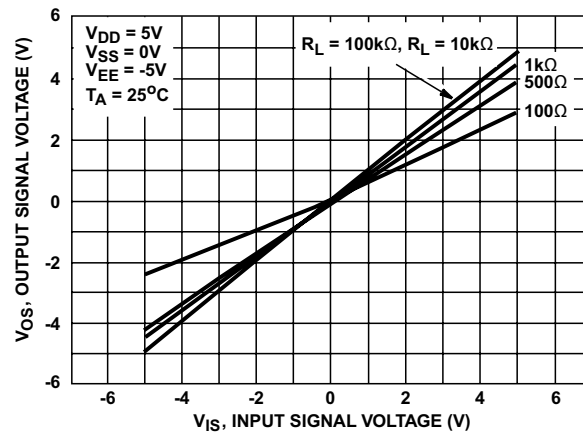


图 8-2. ON Characteristics for 1 of 8 Channels (CD4051B)

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Electrical Characteristics](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a  $0.1 \mu F$  bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a  $0.01 \mu F$  or  $0.022 \mu F$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a  $0.1 \mu F$  bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise.  $0.1 \mu F$  and  $1 \mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 图 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 8.4.2 Layout Example

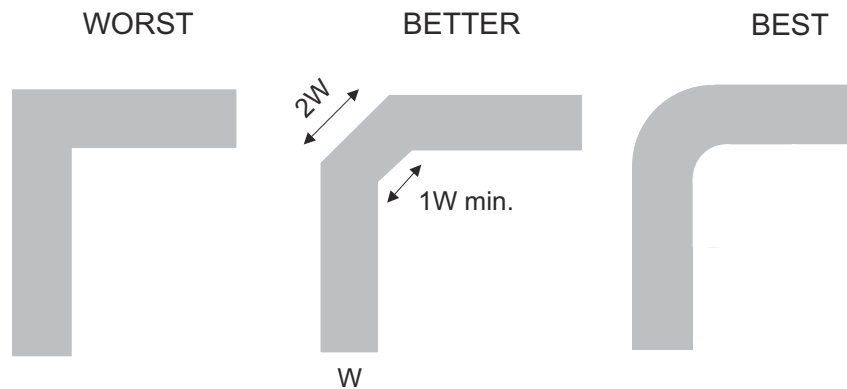


图 8-3. Trace Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

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### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

#### TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision M (November 2024) to Revision N (February 2025)</b>	<b>Page</b>
• 更新了 <a href="#">节 1</a> .....	<a href="#">1</a>
• Removed Figure 5-4 and Figure 5-5.....	<a href="#">11</a>
• Updated <a href="#">节 7.1</a> .....	<a href="#">15</a>
• Updated <a href="#">节 7.3</a> .....	<a href="#">17</a>
• Updated Figure 8-1 to 5V VDD.....	<a href="#">19</a>

<b>Changes from Revision L (September 2023) to Revision M (November 2024)</b>	<b>Page</b>
• Updated the <i>Typical Characteristics</i> section.....	<a href="#">11</a>
• Added Figure 5-4 and Figure 5-5.....	<a href="#">11</a>

<b>Changes from Revision K (March 2023) to Revision L (September 2023)</b>	<b>Page</b>
• 更改了 <i>封装信息</i> 表的格式以包含封装引线尺寸.....	<a href="#">1</a>
• Changed the format of the <i>ESD Ratings</i> , <i>Electrical Characteristics</i> , and <i>AC Performance</i> to consolidate package specifications.....	<a href="#">5</a>

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7901502EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	<a href="#">Samples</a>
8101801EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	<a href="#">Samples</a>
CD4051BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4051BE	<a href="#">Samples</a>
CD4051BEE4	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-55 to 125	CD4051BE	
CD4051BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF	<a href="#">Samples</a>
CD4051BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4051BF3A	<a href="#">Samples</a>
CD4051BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051BM	<a href="#">Samples</a>
CD4051BM96G3	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4051BM	
CD4051BM96G4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4051BM	
CD4051BMT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4051BM	
CD4051BNSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4051B	<a href="#">Samples</a>
CD4051BPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM051B	
CD4051BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM051B	<a href="#">Samples</a>
CD4051BPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM051B	
CD4052BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	<a href="#">Samples</a>
CD4052BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4052BE	<a href="#">Samples</a>
CD4052BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4052BF	<a href="#">Samples</a>
CD4052BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7901502EA CD4052BF3A	<a href="#">Samples</a>
CD4052BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4052BM	
CD4052BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052BM	<a href="#">Samples</a>
CD4052BM96G3	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4052BM	



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4052BM96G4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4052BM	
CD4052BMT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4052BM	
CD4052BNSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4052B	Samples
CD4052BPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM052B	
CD4052BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM052B	Samples
CD4052BPWRG3	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM052B	
CD4052BPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM052B	
CD4053BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4053BE	Samples
CD4053BF	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4053BF	Samples
CD4053BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8101801EA CD4053BF3A	Samples
CD4053BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4053M	
CD4053BM96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053M	Samples
CD4053BM96G3	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4053M	
CD4053BM96G4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4053M	
CD4053BMT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	CD4053M	
CD4053BNSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4053B	Samples
CD4053BPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM053B	
CD4053BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM053B	Samples
CD4053BPWRG3	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM053B	
CD4053BPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	CM053B	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4051B, CD4051B-MIL, CD4052B, CD4052B-MIL, CD4053B, CD4053B-MIL :**

● Catalog : [CD4051B](#), [CD4052B](#), [CD4053B](#)

● Automotive : [CD4051B-Q1](#), [CD4051B-Q1](#), [CD4053B-Q1](#), [CD4053B-Q1](#)

● Military : [CD4051B-MIL](#), [CD4052B-MIL](#), [CD4053B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4051BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4051BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4051BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4051BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4052BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4052BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4052BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4052BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4053BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4053BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4053BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4053BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4051BM96	SOIC	D	16	2500	356.0	356.0	35.0
CD4051BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD4051BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4051BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4052BM96	SOIC	D	16	2500	356.0	356.0	35.0
CD4052BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD4052BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4052BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4053BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4053BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4053BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD4053BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4051BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4052BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4053BEE4	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

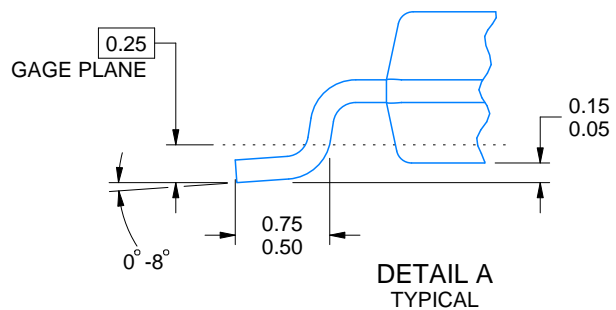
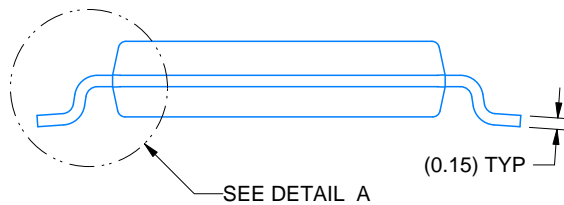
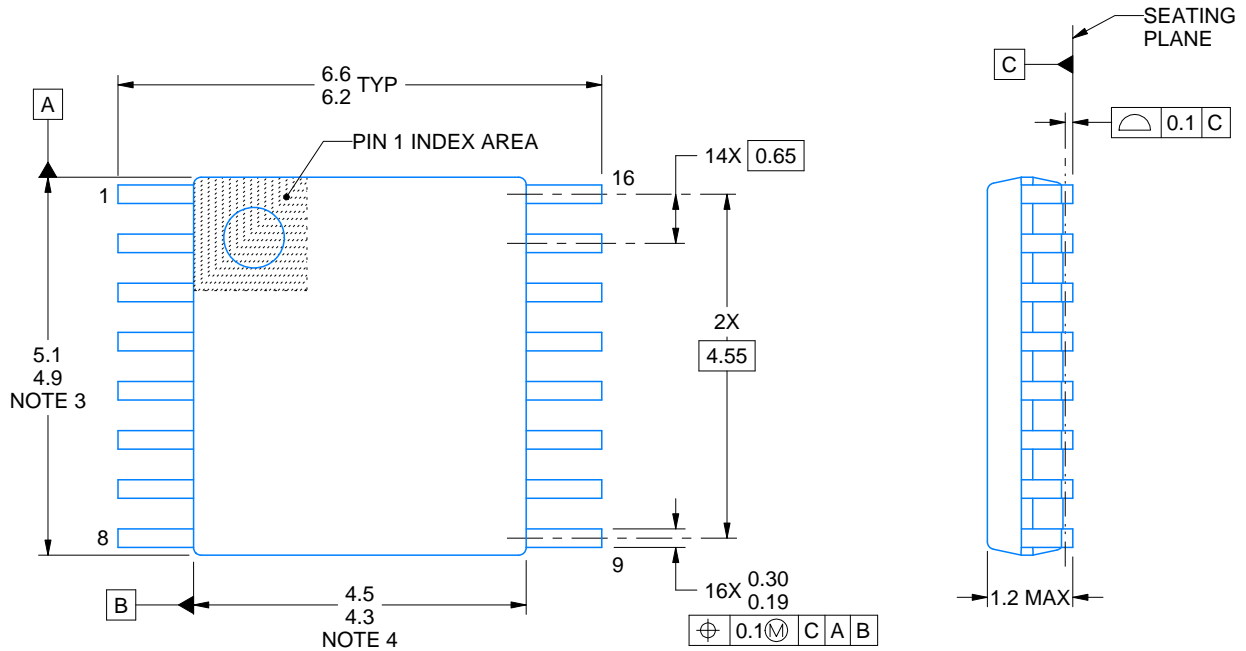
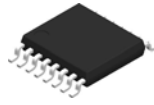
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



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