CC2340R5 SimpleLink™ 低功耗 *Bluetooth*® 5.3 无线 MCU

1 特性

无线微控制器

- 经过优化的 48MHz Arm® Cortex®-M0+ 处理器
- 512KB 系统内可编程闪存
- 12KB ROM 用于引导加载程序和驱动程序
- 36KB 超低泄漏 SRAM。待机模式下完全 RAM 保持
- 与低功耗 Bluetooth® 5.3 兼容的 2.4GHz 射频收发器
- 集成平衡-非平衡变压器
- 支持无线升级 (OTA)
- 串行线调试 (SWD)

低功耗

- MCU 功耗：
  - 2.6mA 有源模式，CoreMark®
  - 53 µA/MHz（运行 CoreMark® 时）
  - < 710nA 待机模式，RTC，36KB RAM
  - 150nA 关断模式，引脚唤醒
- 无线电功耗：
  - RX：5.3mA
  - TX：5.1mA（在 0dBm 条件下）
  - TX：< 11.0mA（在 +8dBm 条件下）

无线协议支持

- 低功耗 *Bluetooth*® 5.3
- ZigBee® [1]
- SimpleLink™ TI 15.4-stack [1]
- 专有系统

高性能无线电

- -102dBm（在 125kbps 低功耗 Bluetooth® 下）
- -96.5dBm（在 1Mbps 低功耗 Bluetooth® 下）
- 高达 +8dBm 的输出功率，具有温度补偿

法规遵从性

- 适用于符合以下标准的系统：
  - EN 300 328（欧洲）
  - FCC CFR47 第 15 部分
  - ARIB STD-T66（日本）

MCU 外设

- 多达 26 个 I/O 板
  - 2 个 IO 焊盘 SWD，与 GPIO 进行多路复用
  - 2 个 IO 焊盘 LFXT，与 GPIO 进行多路复用
  - 多达 22 个 DIO（模拟或数字 IO）
- 3×16 位和 1×24 位通用计时器，支持正交解码模式
- 12 位 ADC，使用外部基准时 1.2MSPS，使用内部基准时 267ksps、高达 12 个外部 ADC 输入
- 1× 低功耗比较器
- 1 个异步收发器 (UART)
- 1× SPI
- 1× I^2C
- 实时时钟 (RTC)
- 集成温度和电池监控器
- 看门狗计时器

安全驱动工具

- AES 128 位加密加速计
- 来自片上模拟噪声的随机数生成器

开发工具和软件

- LP-EM-CC2340R5 LaunchPad 开发套件
- SimpleLink™ CC23xx 软件开发套件 (SDK)
- 用于简单无线电配置的 SmartRF™ Studio
- SysConfig 系统配置工具

工作温度范围

- 片上降压直流/直流转换器
- 1.71V 至 3.8V 单电源电压
- T_j：-40 至 +125°C

符合 RoHS 标准的封装

- 5mm × 5mm RKP QFN40 (26 个 GPIO)
- 4mm × 4mm RGE QFN24（12 个 GPIO）

[1] 在未来的 SDK 中提供

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

2 应用

- 医疗
  - 居家医疗保健 – 血糖监测仪、血压监测仪、CPAP 呼吸机、电子温度计
  - 患者监护和诊断 – 医疗传感器贴片
  - 个人护理和健身 – 电动牙刷、可穿戴健身和活动监测仪
- 楼宇自动化
  - 楼宇安防系统 – 运动检测器、电子智能锁、门窗传感器、车库门系统、网关
  - HVAC – 恒温器、无线环境传感器
  - 防火安全系统 – 烟雾和热量探测器
  - 视频监控 – IP 网络摄像头
- 照明
  - LED 灯具
  - 照明控制 – 日光传感器、照明传感器、无线控制
- 工厂自动化和控制
- 零售自动化和支付 – 电子销售终端
  - 电子货架标签
- 通信设备
  - 有线网络
  - 无线 LAN 或 Wi-Fi 接入点，边缘路由器
- 个人电子产品
  - 联网外设 – 消费类无线模块、指点设备、键盘
  - 游戏 – 电子玩具和机器人玩具
  - 可穿戴设备（非医用）– 智能追踪器、智能服装

3 说明

SimpleLink™ CC2340R5 器件是面向低功耗 *Bluetooth*® 5.3 和专有 2.4GHz 应用的 2.4GHz 无线微控制器 (MCU)。该器件针对低功耗无线通信进行了优化，并支持片上双映像无线下载 (OAD) 功能，[2] 适用于楼宇自动化（无线传感器、照明控制、信标）、资产跟踪、医疗、零售 EPOS（电子销售终端）、ESL（电子货架标签）和个人电子产品（玩具、HID、触控笔）市场。 的突出特性包括：

- 支持 *Bluetooth* ® 5 特性：高速模式 (2Mbps PHY)、远距离（LE 编码 125kbps 和 500kbps PHY）、Privacy 1.2.1 和通道选择算法 2，以及对 *Bluetooth* ® 4.2 和早期低功耗规范的向后兼容性和支持。
- 完全合格的 *Bluetooth* ® 5.3 软件协议栈（SimpleLink™ CC23xx 软件开发套件 (SDK) 随附）。
- SimpleLink™ CC23xx 软件开发套件 (SDK) 支持 Zigbee® 协议栈 [2]
- 超低待机电流不到 0.71 µA 并具有 RTC 操作和完全 RAM 保持，可显著延长电池寿命，尤其是对于睡眠间隔较长的应用。
- 集成平衡-非平衡变压器，可减少物料清单 (BOM) 电路板布局布线
- 出色的无线电敏感度和稳健性（选择性与阻断）性能，适用于低功耗 *Bluetooth* ®（125kbps LE 编码 PHY 且集成平衡-非平衡变压器时为 -102dBm）。

CC2340R5 器件是 SimpleLink™ MCU 平台的一部分，该平台包括 Wi-Fi®、低功耗*蓝牙*、Thread、Zigbee、Sub-1GHz MCU 和主机 MCU，它们共用一个通用、易于使用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。借助一次性集成的 SimpleLink™ 平台，可以将产品组合中的任何器件组合添加至您的设计中，从而在设计要求变更时实现 100% 的代码重用。如需更多信息，请访问 SimpleLink™ MCU 平台。

[2] 在未来的 SDK 中提供

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器件信息

器件型号(1)	封装	封装尺寸（标称值）
CC2340R52E0RGER	QFN24	4.00mm × 4.00mm
CC2340R52E0RKPR	QFN40	5.00mm × 5.00mm

(1) 如需所有可用器件的最新器件、封装和订购信息，请参阅节 12 中的“封装选项附录”或访问 TI 网站。

4 功能方框图

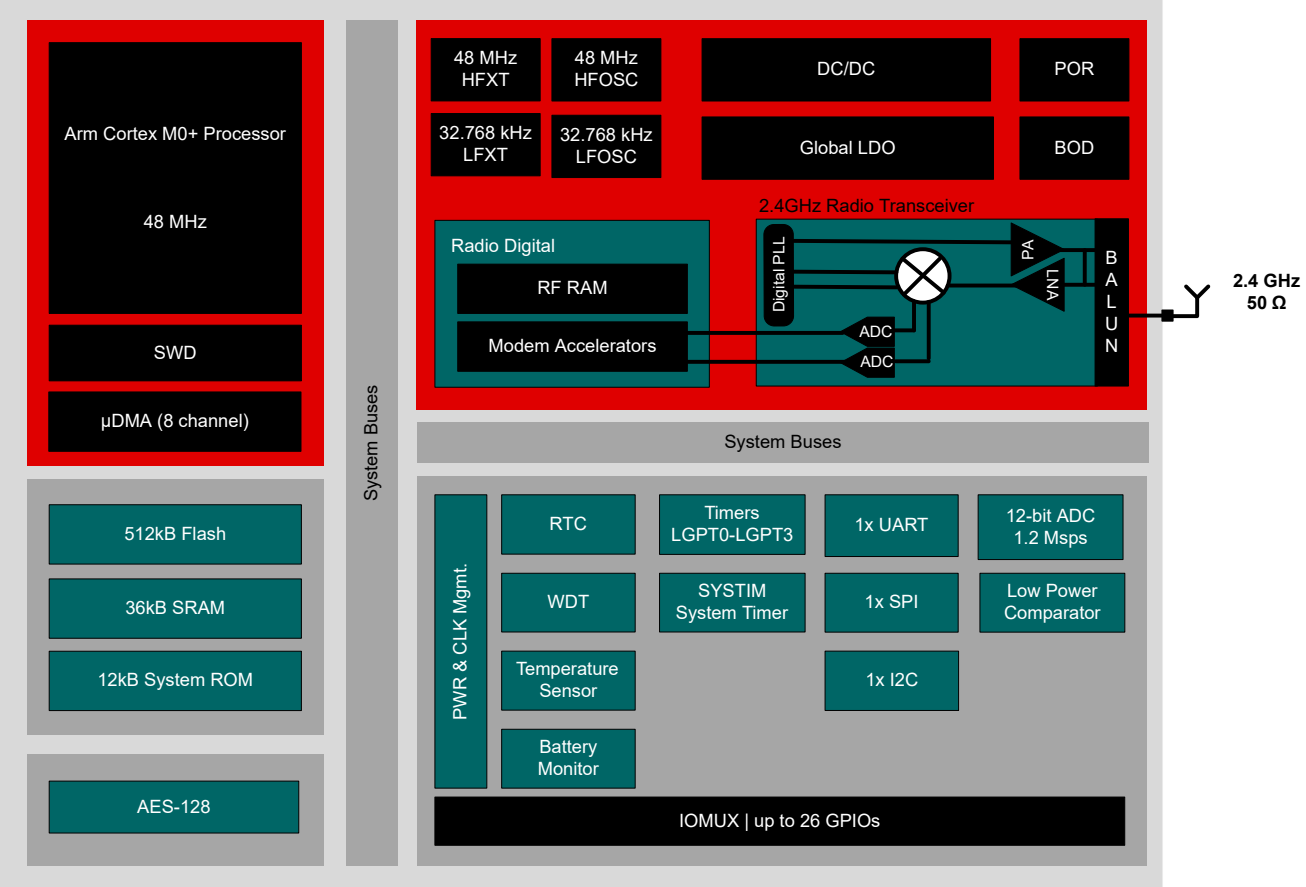

图 4-1. CC2340R5 方框图

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5 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from April 31, 2023 to June 30, 2023 (from Revision B (April 2023) to Revision C (June 2023)) **Page**

- 删除了 4mm × 4mm RGE QFN24 封装的预发布状态 1
- 更正了应用的链接 2
- Corrected pin pitch in pin diagram title 6
- Corrected pin pitch in pin diagram title 9
- Corrected signal name column for DIO19 11
- Changed CDM ESD value to +/- 500 V in ESD Ratings 21
- Clarified that HFOSC tracks HFXT in Table 9-2 and is off in Standby 47
- Corrected temperature calculation example 50

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6 Device Comparison

Device	RADIO SUPPORT										FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE				
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	Wi-SUN®	Sidewalk	*Bluetooth*® LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 X 4 mm VQFN (24)	4 X 4 mm VQFN (32)	5 X 5 mm VQFN (32)	5 X 5 mm VQFN (40)	7 X 7 mm VQFN (48)
CC1310	X		X								32-128	16-20 + 8	10-30		X	X		X
CC1311R3	X		X								352	32 + 8	22-30				X	X
CC1311P3	X		X							X	352	32 + 8	26					X
CC1312R	X		X	X							352	80 + 8	30					X
CC1312R7	X		X	X	X				X		704	144 + 8	30					X
CC1352R	X	X	X	X		X	X	X	X		352	80 + 8	28					X
CC1352P	X	X	X	X		X	X	X	X	X	352	80 + 8	26					X
CC1352P7	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26	X				X
CC2340R5[(1)]		X				X	X	X			512	36	12-26	X			X	
CC2640R2F						X					128	20 + 8	10-31		X	X		X
CC2642R						X					352	80 + 8	31					X
CC2642R-Q1						X					352	80 + 8	31					X
CC2651R3		X				X	X				352	32 + 8	23-31				X	X
CC2651P3		X				X	X			X	352	32 + 8	22-26				X	X
CC2652R		X				X	X	X	X		352	80 + 8	31					X
CC2652RB		X				X	X	X	X		352	80 + 8	31					X
CC2652R7		X				X	X	X	X		704	144 + 8	31					X
CC2652P		X				X	X	X	X	X	352	80 + 8	26					X
CC2652P7		X				X	X	X	X	X	704	144 + 8	26					X
CC2662R-Q1		X									352	80 + 8	31					X

(1) ZigBee and Thread support enabled by future software update

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7 Pin Configuration and Functions

7.1 Pin Diagram – RKP Package (Top View)

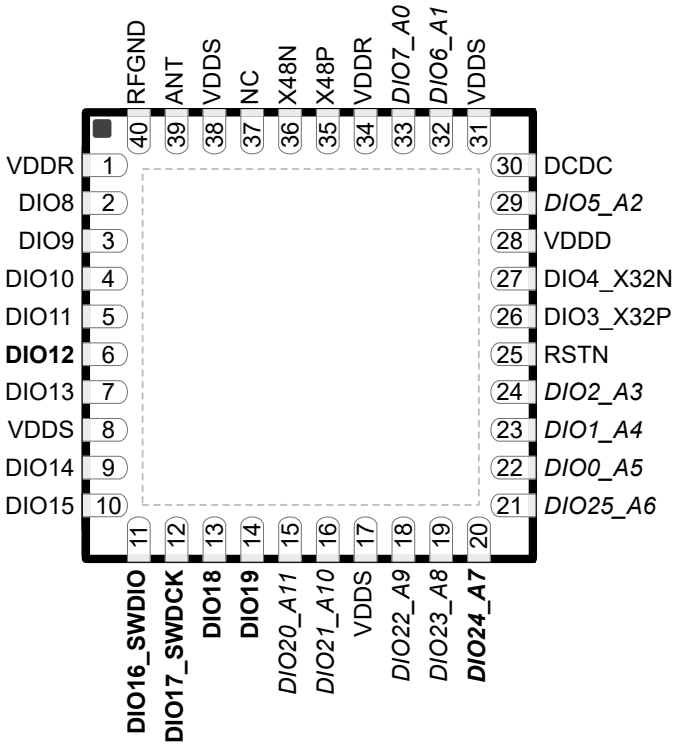

图 7-1. RKP (5-mm × 5-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in 图 7-1 in **bold** have high-drive capabilities:

- Pin 6, DIO12
- Pin 11, DIO16_SWDIO
- Pin 12, DIO17_SWDCK
- Pin 13, DIO18
- Pin 14, DIO19
- Pin 20, DIO24_A7

The following I/O pins marked in 图 7-1 in *italics* have analog capabilities:

- Pin 15, DIO20_A11
- Pin 16, DIO21_A10
- Pin 18, DIO22_A9
- Pin 19, DIO23_A8
- Pin 20, DIO24_A7
- Pin 21, DIO25_A6
- Pin 22, DIO0_A5
- Pin 23, DIO1_A4
- Pin 24, DIO2_A3
- Pin 29, DIO5_A2
- Pin 32, DIO6, A1
- Pin 33, DIO7_A0

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7.2 Signal Descriptions – RKP Package

表 7-1. Signal Descriptions – RKP Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
EGP	—	—	GND	Ground – exposed ground pad(1)
VDDR	1	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (3) (4)
DIO8	2	I/O	Digital	GPIO
DIO9	3	I/O	Digital	GPIO
DIO10	4	I/O	Digital	GPIO
DIO11	5	I/O	Digital	GPIO
DIO12	6	I/O	Digital	GPIO, high-drive capability
DIO13	7	I/O	Digital	GPIO
VDDS	8	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO14	9	I/O	Digital	GPIO
DIO15	10	I/O	Digital	GPIO
DIO16_SWDIO	11	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO17_SWDCK	12	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO18	13	I/O	Digital	GPIO, high-drive capability
DIO19	14	I/O	Digital	GPIO, high-drive capability
DIO20_A11	15	I/O	Digital or Analog	GPIO, analog capability
DIO21_A10	16	I/O	Digital or Analog	GPIO, analog capability
VDDS	17	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO22_A9	18	I/O	Digital or Analog	GPIO, analog capability
DIO23_A8	19	I/O	Digital or Analog	GPIO, analog capability
DIO24_A7	20	I/O	Digital or Analog	GPIO, Analog capability, high-drive capability
DIO25_A6	21	I/O	Digital or Analog	GPIO, analog capability
DIO0_A5	22	I/O	Digital or Analog	GPIO, analog capability
DIO1_A4	23	I/O	Digital or Analog	GPIO, analog capability
DIO2_A3	24	I/O	Digital or Analog	GPIO, analog capability
RSTN	25	I	Digital	Reset, active low. No internal pullup resistor
DIO3_X32P	26	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 1, Optional TCXO input
DIO4_X32N	27	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 2
VDDD	28	—	Power	For decoupling of internal 1.28-V regulated core-supply. Connect an external 1 µF decoupling capacitor.(2)
DIO5_A2	29	I/O	Digital or Analog	GPIO, analog capability
DCDC	30	—	Power	Switching node of internal DC/DC converter(5)
VDDS	31	—	Power	1.71-V to 3.8-V analog supply(5)
DIO6_A1	32	I/O	Digital or Analog	GPIO, analog capability
DIO7_A0	33	I/O	Digital or Analog	GPIO, analog capability
VDDR	34	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(2) (3) (4)
X48P	35	—	Analog	48-MHz crystal oscillator pin 1
X48N	36	—	Analog	48-MHz crystal oscillator pin 2
NC	37	—	—	No Connect
VDDS	38	—	Power	1.71-V to 3.8-V analog supply(5)

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表 7-1. Signal Descriptions – RKP Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
ANT	39	I/O	RF	2.4 GHz TX, RX
RFGND	40	—	RFGND	RF Ground

(1) EGP is the only non-RF ground connection for the device. Good electrical connection to PCB ground plane is required for proper device operation.
(2) Do not supply external circuitry from this pin.
(3) VDDR pins 1 and 34 must be tied together on the PCB.
(4) Output from internal DC/DC and LDO is trimmed to 1.5 V.
(5) For more details, see the technical reference manual listed in 节 11.3.

7.3 Connections for Unused Pins and Modules – RKP Package

表 7-2. Connections for Unused Pins – RKP Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	2 – 7 9 – 10 13 – 14	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	11	NC, GND, or VDDS	GND or VDDS
	DIO17_SWDCK	12	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	15 – 16 18 – 24 29 32 – 33	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	26	NC or GND	NC
	DIO4_X32N	27		
DC/DC converter(2)	DCDC	30	NC	NC
	VDDS	8, 17, 31, 38	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF DCDC capacitor must be kept on the VDDR net.

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7.4 Pin Diagram – RGE Package (Top View)

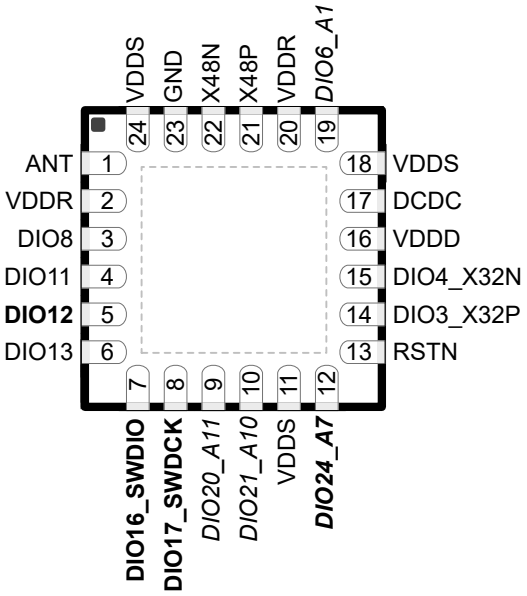

图 7-2. RGE (4-mm × 4-mm) Pinout, 0.5-mm Pitch(Top View)

The following I/O pins marked in 图 7-2 in **bold** have high-drive capabilities:

- Pin 5, DIO12
- Pin 7, DIO16_SWDIO
- Pin 8, DIO17_SWDCK
- Pin 12, DIO24_A7

The following I/O pins marked in 图 7-2 in *italics* have analog capabilities:

- Pin 9, DIO20_A11
- Pin 10, DIO21_A10
- Pin 12, DIO24_A7
- Pin 19, DIO6_A1

7.5 Signal Descriptions – RGE Package

表 7-3. Signal Descriptions – RGE Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
EGP	—	—	GND	Ground – exposed ground pad(1)
ANT	1	I/O	RF	2.4 GHz TX, RX
VDDR	2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (3) (4)
DIO8	3	I/O	Digital	GPIO
DIO11	4	I/O	Digital	GPIO
DIO12	5	I/O	Digital	GPIO, high-drive capability
DIO13	6	I/O	Digital	GPIO
DIO16_SWDIO	7	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO17_SWDCK	8	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO20_A11	9	I/O	Digital or Analog	GPIO, analog capability
DIO21_A10	10	I/O	Digital or Analog	GPIO, analog capability

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表 7-3. Signal Descriptions – RGE Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDS	11	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO24_A7	12	I/O	Digital or Analog	GPIO, Analog capability, high-drive capability
RSTN	13	I	Digital	Reset, active low. No internal pullup resistor
DIO3_X32P	14	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 1, Optional TCXO input
DIO4_X32N	15	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 2
VDDD	16	—	Power	For decoupling of internal 1.28-V regulated core-supply. Connect an external 1 µF decoupling capacitor.(2)
DCDC	17	—	Power	Switching node of internal DC/DC converter(5)
VDDS	18	—	Power	1.71-V to 3.8-V analog supply(5)
DIO6_A1	19	I/O	Digital or Analog	GPIO, analog capability
VDDR	20	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(2) (3) (4)
X48P	21	—	Analog	48-MHz crystal oscillator pin 1
X48N	22	—	Analog	48-MHz crystal oscillator pin 2
GND	23	—	GND	Ground
VDDS	24	—	Power	1.71-V to 3.8-V analog supply(5)

(1) EGP is the only non-RF ground connection for the device. Good electrical connection to PCB ground plane is required for proper device operation.
(2) Do not supply external circuitry from this pin.
(3) VDDR pins 2 and 20 must be tied together on the PCB.
(4) Output from internal DC/DC and LDO is trimmed to 1.5 V.
(5) For more details, see technical reference manual listed in 节 11.3.

7.6 Connections for Unused Pins and Modules – RGE Package

表 7-4. Connections for Unused Pins – RGE Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	3 – 6	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	7	NC, GND, or VDDS	GND or VDDS
	DIO17_SWDCK	8	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	9 – 10 12 19	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	14	NC or GND	NC
	DIO4_X32N	15		
DC/DC converter(2)	DCDC	17	NC	NC
	VDDS	11, 18, 24	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF DCDC capacitor must be kept on the VDDR net.

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7.7 RKP and RGE Peripheral Pin Mapping

表 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
2	1	VDDR	VDDR	—	N/A	N/A
3	2	DIO8	GPIO8	I/O	0	I/O
			SPI0SCLK		1	I/O
			UART0RTS		2	O
			T1C0N		3	O
			I2C0SDA		4	I/O
			T0C0N		5	O
			DTB3		7	O
—	3	DIO9	GPIO9	I/O	0	I/O
			T3C0		1	O
			LRFD3		3	O
—	4	DIO10	GPIO10	I/O	0	I/O
			LPCO		1	O
			T2PE		2	O
			T3C0N		3	O
4	5	DIO11	GPIO11	I/O	0	I/O
			SPI0CSN		1	I/O
			T1C2N		2	O
			T0C0		3	O
			LRFD0		4	O
			SPI0POCI		5	I/O
			DTB9		7	O
5	6	DIO12	GPIO12	I/O	0	I/O
			SPI0POCI		1	I/O
			SPI0PICO		2	I/O
			UART0RXD		3	I
			T1C1		4	O
			I2C0SDA		5	I/O
			DTB13		7	O
6	7	DIO13	GPIO13	I/O	0	I/O
			SPI0POCI		1	I/O
			SPI0PICO		2	I/O
			UART0TXD		3	O
			T0C0N		4	O
			T1F		5	O
			DTB4		7	O
—	8	VDDS	VDDS	—	N/A	N/A
—	9	DIO14	GPIO14	I/O	0	I/O
			T3C2		1	O
			T1C2N		2	O
			LRFD5		3	O
			T1F		4	O

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表 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
—	10	DIO15	GPIO15	I/O	0	I/O
			UART0RXD		1	I
			T2C0N		2	O
			CKMIN		3	I
7	11	DIO16_SWDIO	GPIO16	I/O	0	I/O
			SPI0PICO		1	I/O
			UART0RXD		2	I
			I2C0SDA		3	I/O
			T1C2		4	O
			T1C0N		5	O
			DTB10		7	O
8	12	DIO17_SWDCK	GPIO17	I/O	0	I/O
			SPI0SCLK		1	I/O
			UART0TXD		2	O
			I2C0SCL		3	I/O
			T1C1N		4	O
			T0C2		5	O
			DTB11		7	O
—	13	DIO18	GPIO18	I/O	0	I/O
			T3C0		1	O
			LPCO		2	O
			UART0TXD		3	O
			SPI0SCLK		4	I/O
			DTB12		7	O
—	14	DIO19	GPIO19	I/O	0	I/O
			T3C1		1	O
			T2PE		2	O
			SPI0PICO		4	I/O
			DTB0		7	O
9	15	DIO20_A11	GPIO20	I/O	0	I/O
			LPCO		1	O
			UART0TXD		2	O
			UART0RXD		3	I
			T1C0		4	O
			SPI0POCI		5	I/O
			ADC11		6	I
			DTB14		7	O

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表 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
10	16	DIO21_A10	GPIO21	I/O	0	I/O
			UART0CTS		1	I
			T1C1N		2	O
			T0C1		3	O
			SPI0POCI		4	I/O
			LRFD1		5	O
			ADC10/LPC+		6	I
			DTB15		7	O
11	17	VDDS	VDDS	—	N/A	N/A
—	18	DIO22_A9	GPIO22	I/O	0	I/O
			T2C0		1	O
			UART0RXD		2	I
			T3C1N		3	O
			ADC9		6	I
			DTB1		7	O
—	19	DIO23_A8	GPIO23	I/O	0	I/O
			T2C1		1	O
			T3C2N		3	O
			ADC8/LPC+/LPC-		6	I
12	20	DIO24_A7	GPIO24	I/O	0	I/O
			SPI0SCLK		1	I/O
			T1C0		2	O
			T3C0		3	O
			T0PE		4	O
			I2C0SCL		5	I/O
			ADC7/LPC+/LPC-		6	I
			DTB5		7	O
—	21	DIO25_A6	GPIO25	I/O	0	I/O
			SPI0POCI		1	I/O
			I2C0SCL		2	I/O
			T2C2N		3	O
			ADC6		6	I
—	22	DIO0_A5	GPIO0	I/O	0	I/O
			SPI0CSN		1	I/O
			I2C0SDA		2	I/O
			T3C2		3	O
			ADC5		6	I
—	23	DIO1_A4	GPIO1	I/O	0	I/O
			T3C1		1	O
			LRFD7		2	O
			T1F		3	O
			UART0RTS		4	O
			ADC4		5	I
			DTB2		6	O

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表 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
—	24	DIO2_A3	GPIO2	I/O	0	I/O
			T0PE		1	O
			T2C1N		2	O
			UART0CTS		3	I
			ADC3		6	I
13	25	RTSN	RSTN	—	N/A	N/A
14	26	DIO3_X32P	GPIO3	I/O	0	I/O
			LFCI		1	I
			T0C1N		2	O
			LRFD0		3	O
			T3C1		4	O
			T1C2		5	O
			LFXT_P		6	I
			DTB7		7	O
15	27	DIO4_X32N	GPIO4		0	I/O
			T0C2N		1	O
			UART0TXD		2	O
			LRFD1		3	O
			SPI0PICO		4	I/O
			T0C2		5	O
			LFXT_N		6	I
			DTB8		7	O
16	28	VDDD	VDDD	—	N/A	N/A
—	29	DIO5_A2	GPIO5	I/O	0	I/O
			T2C2		1	O
			LRFD6		3	O
			ADC2		6	I
17	30	DCDC	DCDC	—	N/A	N/A
18	31	VDDS	VDDS	—	N/A	N/A
19	32	DIO6_A1	GPIO6	I/O	0	I/O
			SPI0CSN		1	I/O
			I2C0SCL		2	I/O
			T1C2		3	O
			LRFD2		4	O
			UART0TXD		5	O
			ADC1/AREF+		6	I
			DTB6		7	O
—	33	DIO7_A0	GPIO7	I/O	0	I/O
			T3C1		1	O
			LRFD4		3	O
			ADC0/AREF-		6	I
20	34	VDDR	VDDR	—	N/A	N/A
21	35	X48P	X48P	—	N/A	N/A
22	36	X48N	X48N	—	N/A	N/A

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表 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE(1)	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
—	37	NC	NC	—	N/A	N/A
24	38	VDDS	VDDS	—	N/A	N/A
1	39	ANT	ANT	—	N/A	N/A
—	40	RFGND	RFGND	—	N/A	N/A
	GND_TAB			—	N/A	N/A

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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7.8 RKP and RGE Peripheral Signal Descriptions

表 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descriptions

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
ADC	ADC11	9	15	I/O	I	HP ADC channel 11 input
	ADC10	10	16			HP ADC channel 10 input
	ADC9	—	18			HP ADC channel 9 input
	ADC8	—	19			HP ADC channel 8 input
	ADC7	12	20			HP ADC channel 7 input
	ADC6	—	21			ADC channel 6 input
	ADC5	—	22			ADC channel 5 input
	ADC4	—	23			ADC channel 4 input
	ADC3	—	24			ADC channel 3 input
	ADC2	—	29			ADC channel 2 input
	ADC1	19	32			HP ADC channel 1 input
	ADC0	—	33			HP ADC channel 0 input
ADC Reference	AREF+	19	32	I/O	I	ADC external voltage reference, positive terminal
	AREF-	—	33			ADC external voltage reference, negative terminal
Clock	X32P	14	26	I/O	I	32-kHz crystal oscillator pin 1, Optional TCXO input
	X32N	15	27	I/O	I	32-kHz crystal oscillator pin 2
	X48P	21	35	—	I	48-MHz crystal oscillator pin 1
	X48N	22	36	—	I	48-MHz crystal oscillator pin 2
	CKMIN	—	10	I/O	I	TDC or HFOSC tracking loop reference clock input
	LFCI	14	26	I/O	I	Low frequency clock input (LFXT bypass clock from pin)
Comparator	LPCO	—	4	I/O	O	Low power comparator output
		—	13			
		9	15			
Comparator Input	LPC+	10	16	I/O	I	Low power comparator positive input terminal
		—	19			
		12	20			
	LPC-	—	19			Lower power comparator negative input terminal
		12	20			

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表 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
Digital Test Bus	DTB3	3	2	I/O	O	Digital test bus output 3
	DTB9	4	5			Digital test bus output 9
	DTB0	—	14			Digital test bus output 0
	DTB4	6	7			Digital test bus output 4
	DTB10	7	11			Digital test bus output 10
	DTB11	8	12			Digital test bus output 11
	DTB12	—	13			Digital test bus output 12
	DTB13	5	6			Digital test bus output 13
	DTB1	—	18			Digital test bus output 1
	DTB2	—	23			Digital test bus output 2
	DTB14	9	15			Digital test bus output 14
	DTB5	12	20			Digital test bus output 5
	DTB15	10	16			Digitial test bus output 15
	DTB7	14	26			Digital test bus output 7
	DTB8	15	27			Digital test bus output 8
	DTB6	19	32			Digital test bus output 6
GPIO	GPIO8	3	2	I/O	I/O	General-purpose input or output
	GPIO9	—	3			
	GPIO10	—	4			
	GPIO11	4	5			
	GPIO12	5	6			
	GPIO13	6	7			
	GPIO14	—	9			
	GPIO15	—	10			
	GPIO16	7	11			
	GPIO17	8	12			
	GPIO18	—	13			
	GPIO19	—	14			
	GPIO20	9	15			
	GPIO21	10	16			
	GPIO22	—	18			
	GPIO23	—	19			
	GPIO24	12	20			
	GPIO25	—	21			
	GPIO0	—	22			
	GPIO1	—	23			
	GPIO2	—	24			
	GPIO3	14	26			
	GPIO4	15	27			
	GPIO5	—	29			
	GPIO6	19	32			
	GPIO7	—	33			

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表 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
I2C	I2C0SCL	8	12	I/O	I/O	I2C clock data
		12	20			
		—	21			
		19	32			
	I2C0SDA	3	2	I/O	I/O	I2C data
		5	6			
		7	11			
		—	22			
LRF Digital Output	LRFD3	—	3	I/O	O	LRF digital ouptut 3
	LRFD0	4	5			LRF digital output 0
		14	26			
	LRFD5	—	9			LRF digital output 5
	LRFD1	10	16			LRF digital output 1
		15	27			
	LRFD7	—	23			LRF digital output 7
	LRFD6	—	29			LRF digital output 6
	LRFD2	19	32			LRF digital output 2
	LRFD4	—	33			LRF digital output 4
Power	VDDR	2	1	—	—	Internal supply
		20	34			
	VDDS	—	8	—	—	1.71-V to 3.8V DIO supply
		11	17			
		18	31			
		24	38			
	VDDD	16	28	—	—	For decoupling of internal 1.28-V regulated core-supply.
	DCDC	17	30	—	—	Switching node of internal DC/DC converter
Reset	RSTN	13	25	—	—	Global main device reset (active low)
RF	ANT	1	39			50 ohm RF port
RF Ground	RFGND	—	40	—	—	RF Ground reference

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表 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
SPI	SPI0SCLK	3	2	I/O	I/O	SPI clock
		8	12			
		—	13			
		12	20			
	SPI0POCI	4	5	I/O	I/O	SPI POCI
		5	6			
		6	7			
		9	15			
		10	16			
		—	21			
	SPI0CSN	4	5	I/O	I/O	SPI chip select
		—	22			
		19	32			
	SPI0PICO	5	6	I/O	I/O	SPI PICO
		6	7			
		7	11			
		—	14			
		15	27			
SWD	SWDIO	7	11	I/O	I/O	JTAG/SWD TCK. Reset default pinout.
	SWDCK	8	12	I/O	I	JTAG/SWD TMS. Reset default pinout.
Timers - Capture/ Compare	T0C0	4	5	I/O	I/O	Capture/compare Output-0 from Timer-0
	T0C1	10	16			Capture/compare Output-1 from Timer-0
	T0C2	8	12			Capture/compare Output-2 from Timer-0
		15	27			
	T1C0	9	15	I/O	I/O	Capture/compare Output-0 from Timer-1
		12	20			
	T1C1	5	6			Capture/compare Output-1 from Timer-1
	T1C2	7	11			Capture/compare Output-2 from Timer-1
		14	26			
		19	32			
	T2C0	—	18	I/O	I/O	Capture/compare Output-0 from Timer-2
	T2C1	—	19			Capture/compare Output-1 from Timer-2
	T2C2	—	29			Capture/compare Output-2 from Timer-2
	T3C0	—	3	I/O	I/O	Capture/compare Output-0 from Timer-3
		—	13			
		12	20			
	T3C1	—	14			Capture/compare Output-1 from Timer-3
		—	23			
		14	26			
		—	33			
	T3C2	—	9			Capture/compare Output-2 from Timer-3
		—	22			

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表 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
Timers - Complementary Capture/ Compare	T0C0N	3	2	I/O	O	Complementary compare/PWM Output-0 from Timer-0
		6	7			
	T0C1N	14	26			Complementary compare/PWM Output-1 from Timer-0
	T0C2N	15	27			Complementary compare/PWM Output-2 from Timer-0
	T1C0N	3	2	I/O	O	Complementary compare/PWM Output-0 from Timer-1
		7	11			
	T1C1N	8	12			Complementary compare/PWM Output-1 from Timer-1
		10	16			
	T1C2N	4	5			Complementary compare/PWM Output-2 from Timer-1
		—	9			
	T2C0N	—	10	I/O	O	Complementary compare/PWM Output-0 from Timer-2
	T2C1N	—	24			Complementary compare/PWM Output-1 from Timer-2
	T2C2N	—	21			Complementary compare/PWM Output-2 from Timer-2
	T3C0N	—	4	I/O	O	Complementary compare/PWM Output-0 from Timer-3
	T3C1N	—	18			Complementary compare/PWM Output-1 from Timer-3
	T3C2N	—	19			Complementary compare/PWM Output-2 from Timer-3
Timers - Fault input	T1F	6	7	I/O	I	Fault input for Timer-1
		—	9			
		—	23			
Timers - Prescaler Event	T2PE	—	4	I/O	O	Prescaler event ouput from Timer-2
		—	14			
	T0PE	12	20	I/O	O	Prescaler eveny ouput from Timer-0
		—	24			
UART	UART0TXD	6	7	I/O	O	UART0 TX data
		8	12			
		—	13			
		9	15			
		15	27			
		19	32			
	UART0RXD	5	6	I/O	I	UART0 RX data
		—	10			
		7	11			
		9	15			
		—	18			
	UART0CTS	10	16	I/O	I	UART0 clear-to-send input (active low)
		—	24			
	UART0RTS	3	2	I/O	O	UART0 request-to-send (active low)
		—	23			

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VDDS	Supply voltage	–0.3	4.1	V
	Voltage on any digital pin(3)	–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins X48P and X48N	–0.3	1.24	V
V_{in_adc}	Voltage on ADC input	0	VDDS	V
	Input level, RF pins		5	dBm
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIOs.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (2)	–40	125	°C
Operating junction temperature(1) (2)	–40	125	°C
Operating supply voltage (VDDS)	1.71	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(3)	0	1	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
(2) For thermal resistance details, refer to *Thermal Resistance Characteristics* table in this document.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10-µF VDDS input capacitor must be used to ensure compliance with this slew rate.

8.4 DCDC

When measured on the CC2340R5 reference design with T_c = 25 °C and DCDC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for DCDC operation (1) (2)		2.2	3.0	3.8	V

(1) When the supply voltage drops below the DCDC operation min voltage, the device automatically transitions to use GLDO regulator on-chip.
(2) A 10uH and 10uF load capacitor are required on the VDDR voltage rail. They should be placed close to the DCDC output pin.

8.5 Global LDO (GLDO)

When measured on the CC2340R5 reference design with T_c = 25 °C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for GLDO operation (1)		1.71	3.0	3.8	V

(1) A 10 µF capacitor is recommended at VDDR pin.

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8.6 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS_BOD					
Untrimmed brownout rising threshold	Before initial boot (1)		1.67		V
Trimmed brownout rising threshold (1)			1.68		V
Trimmed brownout falling threshold (1)			1.67		V
POR					
power-on reset power-up level			1.5		V
power-on reset power-down level			1.45		V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RSTN pin.

8.7 Battery Monitor

Measured on the CC2340R5 reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			22		mV
Range		1.7		3.8	V
Accuracy	VDDS = 3.0 V		30		mV

8.8 Temperature Sensor

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy	-40 °C to 85 °C		±10 (1)		°C

(1) Raw output from register.

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8.9 Power Consumption - Power Modes

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption with DCDC				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	2.6	mA
I_{core}	Active	MCU running CoreMark from Flash at 48MHz	53	µA / MHz
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	780	µA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	810	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	1100	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	1200	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFOSC, DCDC recharge current setting (ipeak = 1)	0.71	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT, DCDC recharge current setting (ipeak = 1)	0.74	µA
Core Current consumption with GLDO				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	4.1	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	1170	µA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	1230	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	1490	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	1665	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFOSC, default GLDO recharge current setting	1.1	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT default GLDO recharge current setting	1.15	µA
Reset, Shutdown Current Consumption				
I_{core}	Reset	Reset. RSTN pin asserted or VDDS below power-on-reset threshold	150	nA
I_{core}	Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled	150	nA
Peripheral Current Consumption				
I_{peri}	RF	Delta current, clock enabled, RF subsystem idle	40	µA
I_{peri}	Timers	Delta current with clock enabled, module is idle, one LGPT timer	2.4	µA
I_{peri}	I2C	Delta current with clock enabled, module is idle	10.6	µA
I_{peri}	SPI	Delta current with clock enabled, module is idle	3.4	µA
I_{peri}	UART	Delta current with clock enabled, module is idle	24.5	µA
I_{peri}	CRYPTO (AES)	Delta current with clock enabled, module is idle	3.8	µA

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8.10 Power Consumption - Radio Modes

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DCDC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, system bus off (1)	5.3	mA
I_{RX}	Radio receive current	2440 MHz, 1 Mbps, GFSK, DCDC OFF, system bus off (1)	9	mA
I_{TX}	Radio transmit current	-8 dBm output power setting 2440 MHz system bus off (1)	4.0	mA
I_{TX}	Radio transmit current	0 dBm output power setting 2440 MHz system bus off (1)	5.1	mA
I_{TX}	Radio transmit current	0 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	8.8	mA
I_{TX}	Radio transmit current	+4 dBm output power setting 2440 MHz system bus off (1)	7.7	mA
I_{TX}	Radio transmit current	+6 dBm output power setting 2440 MHz system bus off (1)	8.9	mA
I_{TX}	Radio transmit current	+8 dBm output power setting 2440 MHz system bus off (1)	10.7	mA
I_{TX}	Radio transmit current	+8 dBm output power setting 2440 MHz DCDC OFF, system bus off (1)	19	mA

(1) System bus off refers to device idle mode, DMA disabled, flash disabled

8.11 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		KB
Supported flash erase cycles before failure, full bank(1) (2)		30			k Cycles
Supported flash erase cycles before failure, single sector(3)		60			k Cycles
Maximum number of write operations per row before sector erase(4)				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash retention	125 °C	10			Years
Flash sector erase current	Average delta current		1.2		mA
Flash sector erase time(5)	0 erase cycles		2.2		ms
Flash write current	Average delta current, full sector at a time		1.7		mA
Flash write time(5)	full sector at a time, 0 erase cycles		7.7		µs

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Aborting flash during erase or program modes is not a safe operation.
(3) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(5) This number is dependent on Flash aging and increases over time and erase cycles

8.12 Thermal Resistance Characteristics

THERMAL METRIC	THERMAL METRIC	PACKAGE		UNIT (1)
		RKP (VQFN)	RGE (VQFN)	
		40 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	40.1	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.1	30.5	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.7	17.2	℃/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	℃/W

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THERMAL METRIC	THERMAL METRIC	PACKAGE		UNIT (1)
		RKP (VQFN)	RGE (VQFN)	
		40 PINS	24 PINS	
ψ_{JB}	Junction-to-board characterization parameter	12.7	17.1	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	3.4	℃/W

(1) °C/W = degrees Celsius per watt.

8.13 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2510	MHz

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8.14 Bluetooth Low Energy - Receive (RX)

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–102		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–122/ 122) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 31 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		47 / 42 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		49 / 45 (3)		dB
Selectivity, ±6 MHz(2)	Wanted signal at –79 dBm, modulated interferer at ⩾ ±6 MHz, BER = 10^{-3}		52 / 48 (3)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ⩾ ±7 MHz, BER = 10^{-3}		54 / 49 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, Image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 42 (3)		dB
500 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–99		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–122 / 122) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90/ 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–4.5		dB
Selectivity, ±1 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		42 / 31 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		45 / 41 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		46 / 42 (3)		dB
Selectivity, ±6 MHz(2)	Wanted signal at –72 dBm, modulated interferer at ⩾ ±6 MHz, BER = 10^{-3}		50 / 45 (3)		dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ⩾ ±7 MHz, BER = 10^{-3}		51 / 46 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB

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When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, Image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at – 72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 41 (3)		dB
1 Mbps (LE 1M)					
Receiver sensitivity	BER = 10^{-3}		– 96.5		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (– 225 /225) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (– 750 / 750) (1)		ppm
Co-channel rejection(2)	Wanted signal at – 67 dBm, modulated interferer in channel, BER = 10^{-3}		– 6		dB
Selectivity, ±1 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 5 (3)		dB
Selectivity, ±2 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		39 / 28 (3)		dB
Selectivity, ±3 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		44 / 38 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		47 / 35 (3)		dB
Selectivity, ±5 MHz or more(2)	Wanted signal at – 67 dBm, modulated interferer at ⩾ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(2)	Wanted signal at – 67 dBm, modulated interferer at image frequency, BER = 10^{-3}		28		dB
Selectivity, image frequency ±1 MHz(2)	Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at – 67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		5 / 38 (3)		dB
Out-of-band blocking(4)	30 MHz to 2000 MHz		– 10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		– 10		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		– 10		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)		– 2		dBm
Intermodulation	Wanted signal at 2402 MHz, – 64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		– 37		dBm
Spurious emissions, 30 to 1000 MHz(5)	Measurement in a 50-Ω single-ended load.		< – 59		dBm
Spurious emissions, 1 to 12.75 GHz(5)	Measurement in a 50-Ω single-ended load.		< – 47		dBm
RSSI dynamic range (6)			70		dB
RSSI accuracy			±4		dB
RSSI resolution			1		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Measured at SMA connector, BER = 10^{-3}		– 92		dBm
Receiver saturation	Measured at SMA connector, BER = 10^{-3}		2		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (– 225 / 225) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (– 1050 / 1050) (1)		ppm
Co-channel rejection(2)	Wanted signal at – 67 dBm, modulated interferer in channel,BER = 10^{-3}		– 8		dB
Selectivity, ±2 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±2 MHz, Image frequency is at – 2 MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±4 MHz(2)	Wanted signal at – 67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		40 / 32 (3)		dB

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When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±6 MHz(2)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		46 / 40 (3)		dB
Selectivity, image frequency(2)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		5		dB
Selectivity, image frequency ±2 MHz(2)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–8 / 32 (3)		dB
Out-of-band blocking(4)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–10		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Exceeding Bluetooth specification
(2) Numbers given as I/C dB
(3) X / Y, where X is +N MHz and Y is –N MHz
(4) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(5) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
(6) The device will saturate at -30dB.

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8.15 Bluetooth Low Energy - Transmit (TX)

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Delivered to a single-ended 50-Ω load through integrated balun		8		dBm
Output power programmable range	Delivered to a single-ended 50-Ω load through integrated balun		28		dB

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8.16 Proprietary Radio Modes

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps GFSK (HID), 320 kHz deviation					
Receiver sensitivity	PER = 30.8%, Payload 37 bytes		-89		dBm

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8.17 2.4 GHz RX/TX CW

When measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Spurious emissions and harmonics						
Spurious emissions(1)	f < 1 GHz, outside restricted bands	+8 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics (1)	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.18 Timing and Switching Characteristics

8.18.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RSTN low duration	1			µs

8.18.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset/Shutdown to Active(1)	GLDO default charge current setting, VDDR capacitor fully charged (2)		350-450		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). DCDC ON, default recharge current configuration		33-43 (3)		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). GLDO ON, default recharge current configuration		33-50 (3)		µs
MCU, Idle to Active	Flash enabled in idle mode		3		µs
MCU, Idle to Active	Flash disabled in idle mode		14		µs

(1) Wakeup time includes device ROM bootcode execution time. The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
(2) This is the best case reset/shutdown to active time (including ROM bootcode operation), for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time
(3) Depending on VDDR capacitor voltage level.

8.18.3 Clock Specifications

8.18.3.1 48 MHz Crystal Oscillator (HFXT)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(4)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ⩽ 9 pF		20	60	Ω
ESR	Equivalent series resistance 5 pF < C_L ⩽ 6 pF			80	Ω
C_L	Crystal load capacitance(1)	3	7(2)	9	pF

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.[4]

	PARAMETER	MIN	TYP	MAX	UNIT
Start-up time [3]	Until clock is qualified		200		µs

(1) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations.
(2) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(3) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(4) Tai-Saw TZ3908AAAO43 has been validated for CC2340R5 design.

8.18.3.2 48 MHz RC Oscillator (HFOSC)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±3		%
Calibrated frequency accuracy [1]		±0.25		%

(1) Accuracy relative to the calibration source (HFXT)

8.18.3.3 32 kHz Crystal Oscillator (LFXT)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
Supported crystal load capacitance	6		12	pF
ESR		30	100	kΩ

8.18.3.4 32 kHz RC Oscillator (LFOSC)

Measured on the CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.768 [1]		kHz
Temperature coefficient.		±600		ppm/°C

(1) When using LFOSC as source for the low frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

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8.19 Peripheral Characteristics

8.19.1 UART

8.19.1.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

8.19.2 SPI

8.19.2.1 SPI Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fSCLK 1/tsclk	SPI clock frequency	Primary Mode 1.71 < VDDS < 3.8			12	MHz
		Secondary Mode 2.7 < VDDS < 3.8			8	
		Secondary Mode VDDS < 2.7			7	
DC_{SCK}	SCK Duty Cycle		45	50	55	%

8.19.2.2 SPI Controller Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK\_H/L}$	SCLK High or Low time		$(t_{SPI}/2)$ - 1	$t_{SPI}/2$	$(t_{SPI}/2)$ + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid,C_L = 20 pF			13	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

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8.19.2.3 SPI Timing Diagrams - Controller Mode

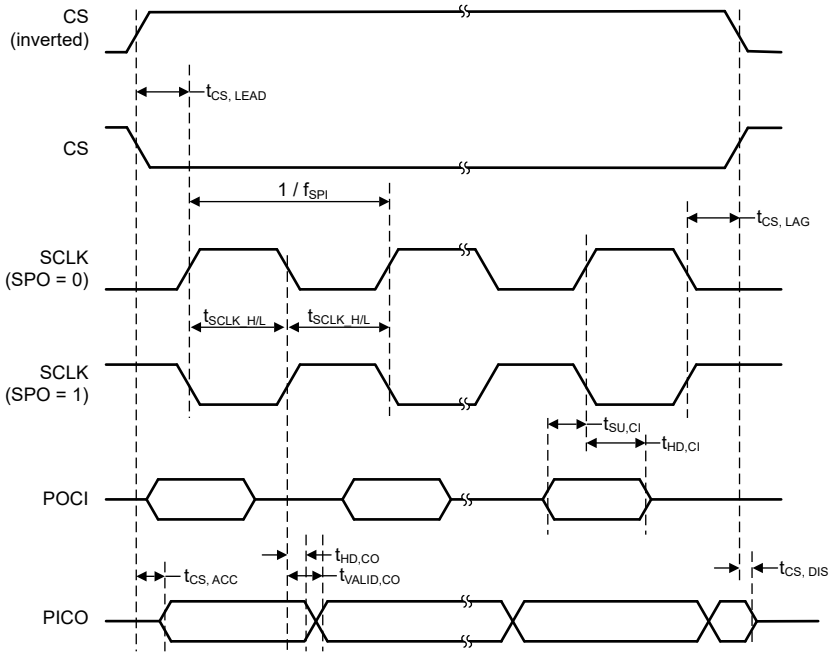

图 8-1. SPI Timing Diagram - Controller Mode, SPH = 0

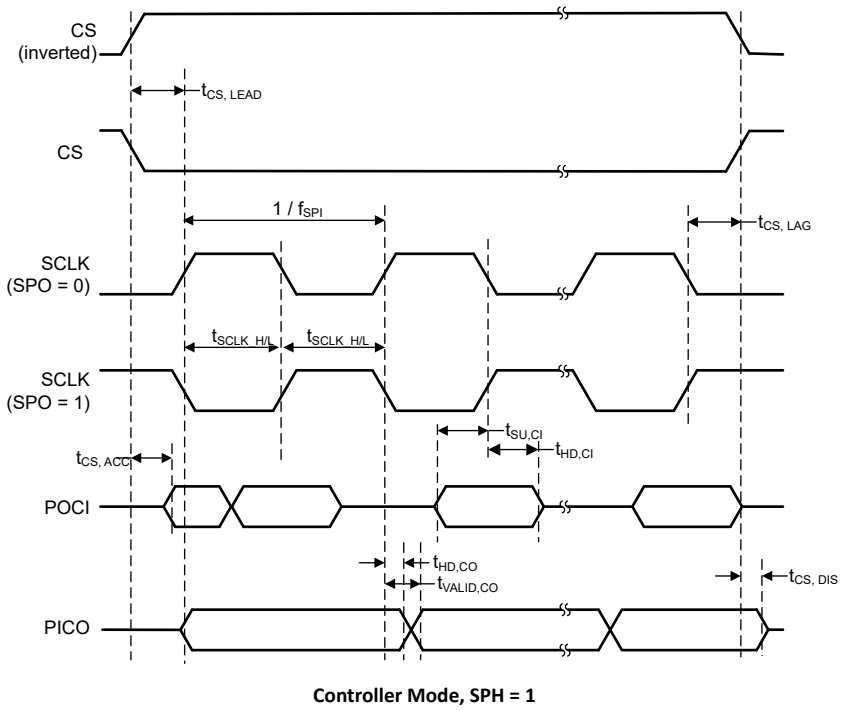

图 8-2. SPI Timing Diagram - Controller Mode, SPH = 1

8.19.2.4 SPI Peripheral Mode

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK

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Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 3.3V			56	ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 1.8V			70	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 3.3V			56	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 1.8V			70	ns
$t_{SU.PI}$	PICO input data setup time		30			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20 pF, 3.3V (4)			50	ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20 pF, 1.8V (4)			65	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20 pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

8.19.2.5 SPI Timing Diagrams - Peripheral Mode

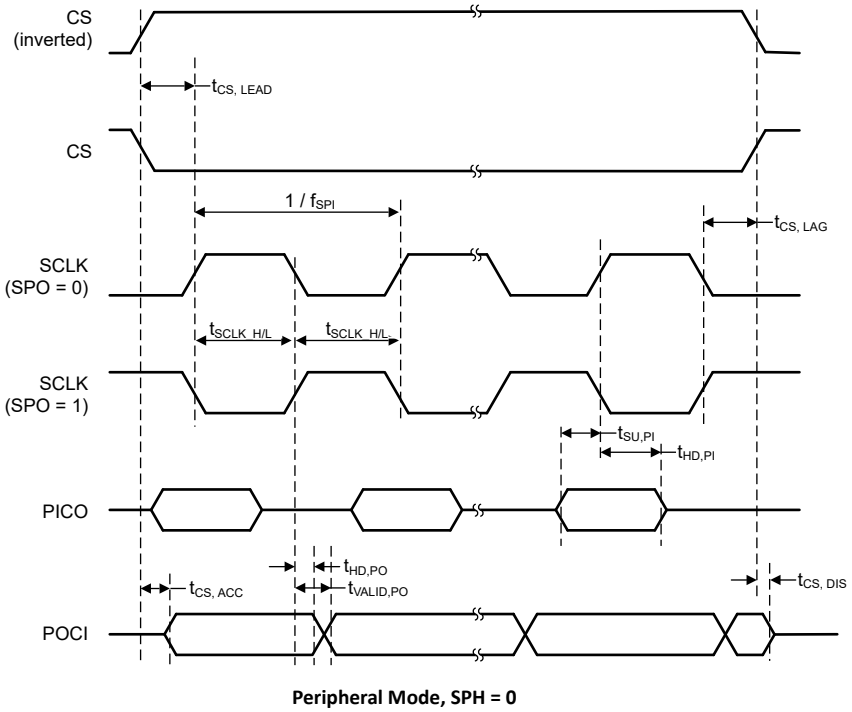

图 8-3. SPI Timing Diagram - Peripheral Mode, SPH = 0

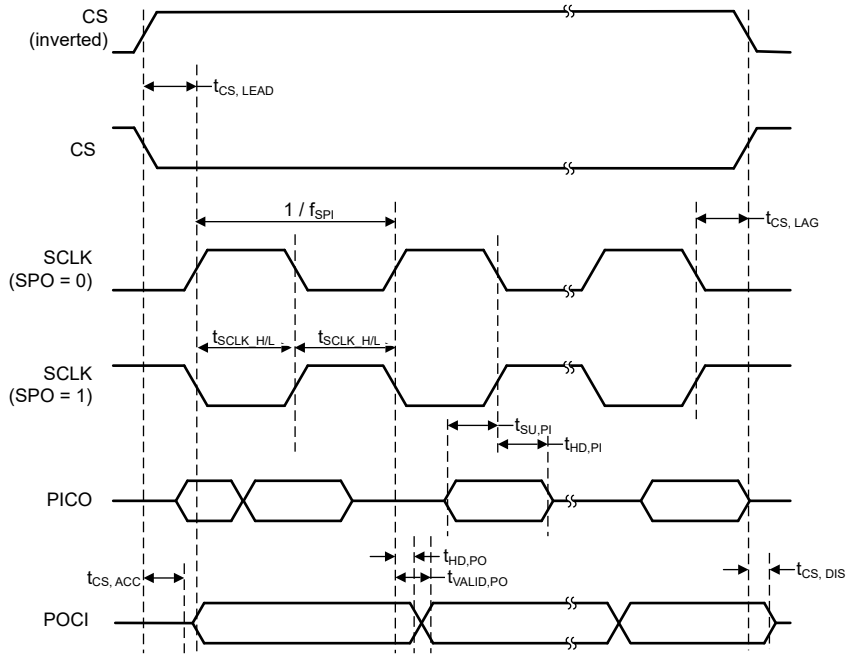

图 8-4. SPI Timing Diagram - Peripheral Mode, SPH = 1

8.19.3 I²C

8.19.3.1 I2C

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100kHz	4.0			µs
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} > 100kHz	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100kHz	4.7			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} > 100kHz	0.6			µs
$t_{HD,DAT}$	Data hold time		0			µs
$t_{SU,DAT}$	Data setup time		100			µs
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100kHz	4.0			µs
$t_{SU,STO}$	Setup time for STOP	f_{SCL} > 100kHz	0.6			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100kHz	4.7			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} > 100kHz	1.3			µs
t_{SP}	Pulse duration of spikes supressed by input deglitch filter		50			ns

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8.19.3.2 I²C Timing Diagram

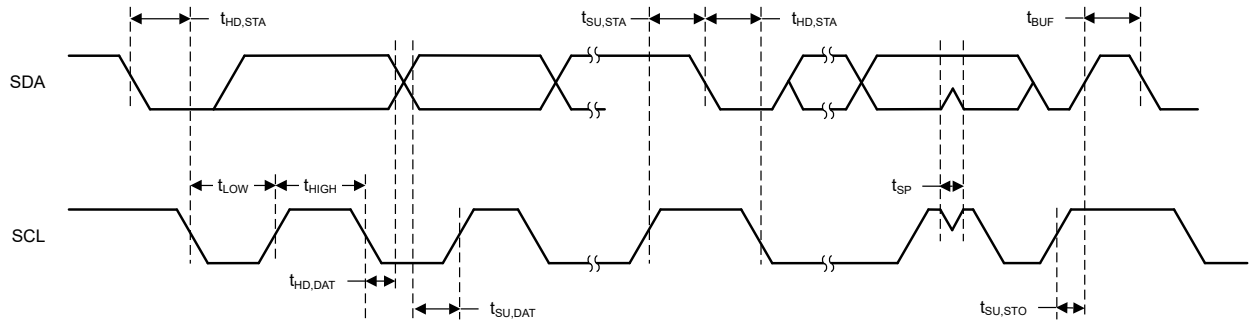

图 8-5. I²C Timing Diagram

8.19.4 GPIO

8.19.4.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	39.08	65.84	108.9	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	9.815	20.71	39.96	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	0.9145	1.105	1.277	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	0.5891	0.752	0.9146	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.2559	0.3534	0.4401	V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 10 mA load	high-drive GPIOs only, max drive setting	2.466			V
GPIO VOL at 10 mA load	high-drive GPIOs only, max drive setting			0.2527	V
GPIO VOH at 2 mA load	standard drive GPIOs	2.516			V
GPIO VOL at 2 mA load	standard drive GPIOs			0.1985	V
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	169.5	261.5	392.7	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	60.08	109.7	171.6	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	1.757	1.983	2.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	1.262	1.515	1.791	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.3961	0.4689	0.5405	V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

8.19.5 ADC

8.19.5.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(2)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins Ax	0		VDDS	V
$I_{(ADC)}$ single-ended mode	Operating supply current into VDDS terminal	RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADCREF_EN = 0), VeREF+ = VDDS		480		µA
		RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADCREF_EN = 0), ADCREF = 2.5V		365		
$C_{I\ GPIO}$	Input capacitance into a single terminal			5	7	pF
$R_{I\ GPIO}$	Input MUX ON-resistance			0.5	1	kΩ
ADC Switching Characteristics						
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			267 (1)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			308 (1)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			400 (1)	ksps

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T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(2)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			1.2 (1)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			1.33 (1)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			1.6 (1)	Msps
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x0 (12-bit)		14		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x1 (10-bit)		12		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x2 (8-bit)		9		cycles
t_{Sample}	Sampling time	RES = 0x0 (12-bit), R_S = 25 Ω, C_{pext} = 10 pF. +/- 0.5 LSB settling	250			ns
$t_{VSUPPLY/3(sample)}$	Sample time required when Vsupply/3 channel is selected		20			µs
ADC Linearity Parameters						
E_I	Integral linearity error (INL) for single-ended inputs	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 2		LSB
E_D	Differential linearity error (DNL)	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 1		LSB
E_O	Offset error	12-bit Mode, External reference, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		1.98		LSB
E_O	Offset error	12-bit Mode, Internal reference, V_{R+} = ADCREF = 2.5V		1.02		LSB
E_G	Gain error	External Reference, V_{R+} = VeREF+ = VDDS , VDD= 1.71-->3.8		+/- 2		LSB
E_G	Gain error	Internal reference, V_{R+} = ADCREF = 2.5V		+/- 40		LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x1 (10-bit)		9.9		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		11.2		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V} , RES = 0x1 (10-bit)		9.6		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		10.4		bit
ENOB	Effective number of bits	VDDS reference, RES = 0x0 (12-bit)		11.2		bit
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		69.18		dB
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		64.37		dB
SINAD	Signal-to-noise and distortion ratio	VDDS reference, RES = 0x0 (12-bit)		69.18		dB
ADC External Reference						
EXTREF	Positive external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF+)	1.4		VDDS	V
EXTREF	Negative external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF-)			0	V
ADC Temperature Diode, Supply Monitor						

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T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(2)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Internal Input: V_{SUPPLY} / 3 Accuracy	V_{supply} voltage divider accuracy for supply monitoring	ADC input channel: Vsupply monitor		+/- 1		%
ADC Internal Input: $I_{Vsupply / 3}$	V_{supply} voltage divider current consumption	ADC input channel Vsupply monitor. V_{supply}=VDDS=3.3V		10		µA
ADC Internal and VDDS Reference						
VDDSREF	Positive ADC reference voltage	ADC reference sourced from VDDS		VDDS		V
ADCREF	Internal ADC Reference Voltage	ADCREF_EN = 1, ADCREF_VSEL = 0, VDDS = 1.71V - VDDSmax		1.4		V
		ADCREF_EN = 1, ADCREF_VSEL = 1, VDDS = 2.7V - VDDSmax		2.5		V
I_{ADCREF}	Operating supply current into VDDA terminal with internal reference ON	ADCREF_EN = 1, VDDA = 1.7V to VDDAmax, ADCREF_VSEL = {0,1}		80		µA
t_{ON}	Internal ADC Reference Voltage power on-time	ADCREF_EN = 1		2		µs

(1) Measured with 48MHz HFOSC
(2) Using IEEE Std 1241-2010 for terminology and test methods

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8.19.6 Comparators

8.19.6.1 Ultra-low power comparator

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		KHz
Voltage Divider Accuracy	Input voltage range is between VDDS/4 and VDDS		98		%
Offset	Measured at V_{DDS} / 2 (Errors seen when using two external inputs)		+/- 27.3		mV
Decision time	Step from – 50 mV to 50 mV		1	3	Clock Cycle
Comparator enable time	COMP_LP disable → enable, VIN+, VIN- from pins,Overdrive ⩾ 20 mV		70		µs
Current consumption	Including using VDDS/2 as internal reference at VIN- comparator terminal		270		nA

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9 Detailed Description

9.1 Overview

节 4 shows the core modules of the CC2340R5 device.

9.2 System CPU

The CC2340R5 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M0+ system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The Cortex-M0+ processor offers multiple benefits to developers including:

- Ultra-low power, energy efficient operation
- Deterministic, high-performance interrupt handling for time-critical applications
- Upward compatibility with the Cortex-M processors family

The Cortex-M0+ processor provides the excellent performance expected of a modern 32- bit architecture core, with higher code density than other 8-bit and 16-bit microcontrollers. Its features include the following:

- ARMv6-M architecture optimized for small-footprint embedded applications
- Subset of Arm Thumb/Thumb-2 mixed 16- and 32-bit instructions delivers the high performance expected of a 32-bit Arm
- Single-cycle multiply instruction
- VTOR supporting offset of the vector table base address
- Serial Wire debug with HW break-point comparators
- Ultra-low-power consumption with integrated sleep modes
- SysTick timer
- 48 MHz operation
- 0.99 DMIPS/MHz

Additionally, the CC2340Rx devices are compatible with all ARM tools and software.

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9.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high performance and highly flexible RF sub system containing RF and baseband circuitry in addition to a software defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The software-defined modem is not programmable by customers but is instead loaded with pre-compiled images provided in the radio driver in the SimpleLink™ CC23xx software development kit (SDK). This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory, thus image loading from NV memory only occurs once after boot and also, no patching is required when exiting power modes.

9.3.1 Bluetooth 5.3 Low Energy

The RF Core offers full support for Bluetooth 5.3 Low Energy, including the high-speed 2 Mbps physical layer and the 500 kbps and 125 kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.3 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.3 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.3 enables fast, reliable firmware updates.

9.3.2 802.15.4 (Thread and Zigbee)

Through a dedicated IEEE radio API, the RF sub-system supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread and Zigbee protocols. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

9.4 Memory

The 512 KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. A special flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static 36 KB RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution during boot.

The ROM includes device bootcode firmware handling initial device trimming operations, security configurations and device lifecycle management. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

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9.5 Cryptography

The CC2340R5 device comes with AES-128 cryptography hardware accelerator, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerators supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AES GCM
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

The AES hardware accelerator can be fed with plaintext/ciphertext from either CPU or using DMA. Sustained throughput of one 16 byte ECB block per 23 cycles is possible corresponding to > 30 Mbps.

The CC2340R5 device supports Random Number Generation (RNG) using on-chip analog noise as the non-deterministic noise source for the purpose of generating a seed for a cryptographically secure counter deterministic random bit generator (CTR-DRBG) that in turn is used to generate random numbers for keys, initialization vectors (IVs), and other random number requirements. Hardware acceleration of AES CTR-DRBG is supported.

The CC2340R5 device includes a complete SHA 256 library in ROM, reducing the code footprint of the application. Uses cases may include generating digests for use in digital signature algorithms, data integrity checks, and password storage.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform.

9.6 Timers

A large selection of timers are available as part of the CC2340R5 device. These timers are:

- **Real-Time Clock (RTC)**

  The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. When the device enters the RESET or SHUTDOWN state the RTC is reset.

  The RTC accumulates time elapsed since reset on each LFCLK. The RTC counter is incremented by LFINC at a rate of 32.768 kHz. LFINC indicates the period of LFCLK in μs, with an additional granularity of 16 fractional bits.

  The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

  There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multi-channel and higher resolution SYSTIM remain in synchronization with the RTC’s time base.

  The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.
- **System Timer (SYSTIM)**

  The SYSTIM is a 34-bit, 5-channel wrap-around timer with a per-channel selectable 32b slice with either a 1 us resolution and 1h11m35s range or 250 ns resolution and 17m54s range. All channels support both capture and single-shot compare (posting an event) operation. One channel is reserved for system software, three channels are reserved for radio software and one channel is freely available to user applications.

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For software convenience a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base (albeit with different resolutions/spans). Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately trigger if the submitted event is in the immediate past (4.294s with 1 us resolution and 1.049s with 250 ns resolution).

- **General Purpose Timers (LGPT)**

  The CC2340R5 device provides four LGPTs with 3 × 16 bit timers and 1× 24 bit timer, all running on up to 48 MHz. The LGPTs support a wide range of features such as:

  - 3 capture/compare channels
  - One-shot or periodic counting
  - Pulse width modulation (PWM)
  - Time counting between edges and edge counting
  - Input filter implemented on each of the channels for all timers
  - IR generation feature available on Timer-0
  - Dead band feature available on Timer-1

  The timer capture/compare and PWM signals are connected to IOs via IO controller module (IOC) and the internal timer event connections to CPU, DMA and other peripherals are via the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. Two LGPTs (2× 16 bit timers) supports quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

表 9-1. Timer Comparison

Feature	Timer 0	Timer 1	Timer 2	Timer 3
Counter Width	16-bit counter width	24-bit counter width	24-bit counter width	24-bit counter width
Quadrature Decoder	Yes	No	Yes	No
Park Mode on Fault	No	Yes	No	No
Programmable Dead-Band Insertion	No	Yes	No	No

- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32 kHz clock rate and operates in device active, idle, and standby modes and cannot be stopped once enabled.

9.7 Serial Peripherals and I/O

The CC2340R5 device provides 1xUART, 1xSPI and 1xI2C serial peripherals

The SPI module supports both SPI controller and peripheral up to 12 MHz with configurable phase and polarity.

The UART module implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps and IRDA SIR mode of operation.

The I2C module is used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both controller and target.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open source. Some GPIOs have high-drive capabilities, which are marked in **bold** in 节 7.

For more information, see the CC23xx SimpleLink™ Wireless MCU Technical Reference Manual.

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9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2340R5 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 8 channels, with 6 channels having dedicated peripheral interface and 2 channels having ability to be triggered via configurable events.
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

On-chip debug is supported through the serial wire debug (SWD) interface, which is an ARM bi-directional 2-wire protocol that communicates with the JTAG Test Access Port (TAP) controller and allows for complete debug functionality. SWD is fully compatible with Texas Instruments' XDS family of debug probes.

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9.11 Power Management

To minimize power consumption, the CC2340R5 supports a number of power modes and power management features (see 表 9-2).

表 9-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES (1)				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
48 MHz high-speed clock (HFCLK)	HFOSC (tracks HFXT)	HFOSC (tracks HFXT)	Off	Off	Off
32 kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IOC, BATMON, RTC, LPCOMP	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	On	On
Watchdog timer (WDT)	Available	Available	Available	Off	Off

(1) “Available” indicates that the specific IP or feature can be enabled by user application in the corresponding device operating modes. “On” indicates that the specific IP or feature is turned on irrespective of the user application configuration of the device in the corresponding device operating mode. “Off” indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode

In the **Active** mode, both of MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU..

In **Idle** mode the CPU is in sleep but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on state of the DMA and debug subsystem.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only state retained in this mode are the latched I/O state, 3V register bank, and the flash memory contents.

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备注

The power, RF and clock management for the CC2340R5 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2340R5 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

9.12 Clock Systems

The CC2340R5 device has the following internal system clocks.

The 48 MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 48 MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48 MHz crystal (HFXT). Radio operation requires an external 48 MHz crystal.

The 32.768 kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer before or after Standby power mode. LFCLK can be driven by the internal 32.8 kHz RC Oscillator (LFOSC), a 32.768 kHz watch-type crystal, or clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32 kHz LFCLK signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC2340R5 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC - with the application and protocol stack running on the system CPU inside the device).

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

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10 Application, Implementation, and Layout

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2340R5 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

LP-EM-CC2340R5 Design Files	The CC2340R5 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2340R5 device.
Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

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10.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are two recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \quad (2)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

Example:

In this example, we assume a simple use case where the radio is transmitting continuously at 0 dBm output power. Let us assume we want to maintain a junction temperature equal or less than 85 °C and the supply voltage is 3 V. Using Equation 1, the temperature difference between the top of the case and junction temperature is calculated. To calculate P, look up the current consumption for Tx at 85 °C. At 85 °C the current consumption is approximately 5.5 mA. This means that P is 5.5 mA × 3 V = 16.5 mW.

The maximum case temperature to maintain and junction temperature of 85 °C is then calculated as:

$$T_{\mathrm{case}} < T_j - 0.4^{\circ C}/_{W} \times 23.4mW = 84.99^{\circ}C \quad (3)$$

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, and so on. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in the Measuring CC13xx and CC26xx Current Consumption application report.

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RHB*).

For orderable part numbers of devices in the RHB (5-mm x 5-mm) package type, see the *Package Option Addendum* of this document, the Device Information in 节 3, the TI website (www.ti.com), or contact your TI sales representative.

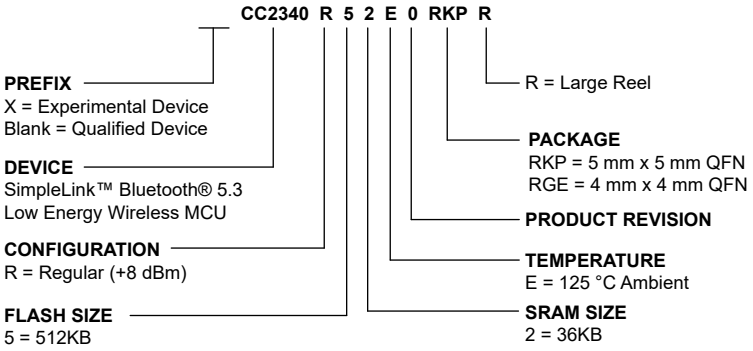

图 11-1. Device Nomenclature

11.2 Tools and Software

The CC2340R5 device is supported by a variety of software and hardware development tools.

Development Kit

CC2340R5 LaunchPad™ Development Kit

The CC2340R5 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2340R5 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and

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Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ CC23xx software development kit (SDK)

The SimpleLink CC23xx software development kit (SDK) provides a complete package for the development of wireless applications on the CC23xx family of devices. The SDK includes a comprehensive software package for the CC2340R5 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.3

The SimpleLink CC23xx SDK is part of TI’s SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

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Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

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11.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder (CC2340R5). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2340R5 Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2340R5 device are found on the device product folder (CC2340R5).

Technical Reference Manual (TRM)

CC23xx SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2340R52E0RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2340 R52	Samples
CC2340R52E0RKPR	ACTIVE	VQFN	RKP	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	CC2340 R52	Samples
CC2340R52N0RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2340 R52	Samples
CC2340R52N0RKPR	ACTIVE	VQFN	RKP	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2340 R52	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CC2340R5 :

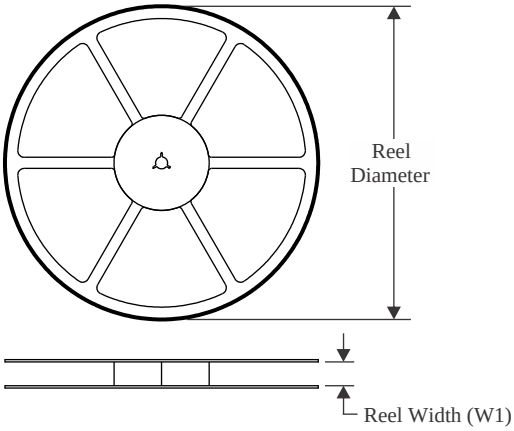
- Automotive : CC2340R5-Q1

NOTE: Qualified Version Definitions:

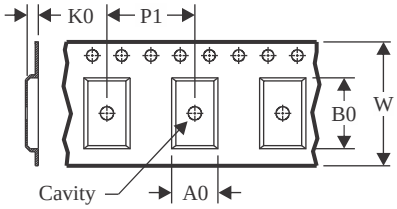
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

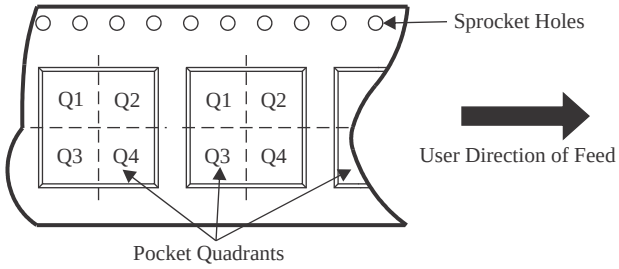


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

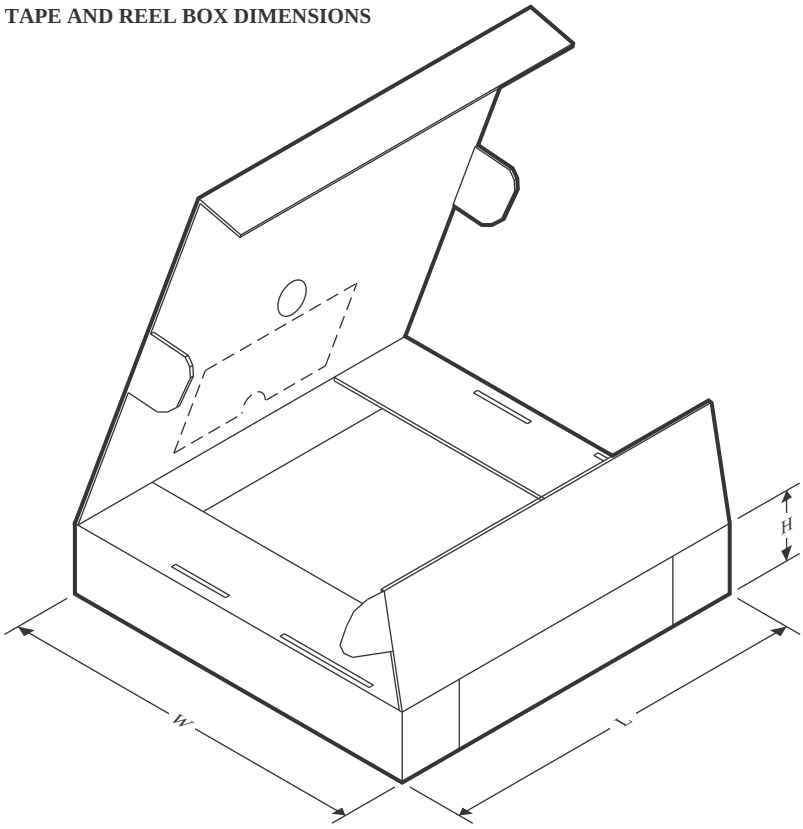
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2340R52E0RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2340R52E0RKPR	VQFN	RKP	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC2340R52N0RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2340R52N0RKPR	VQFN	RKP	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



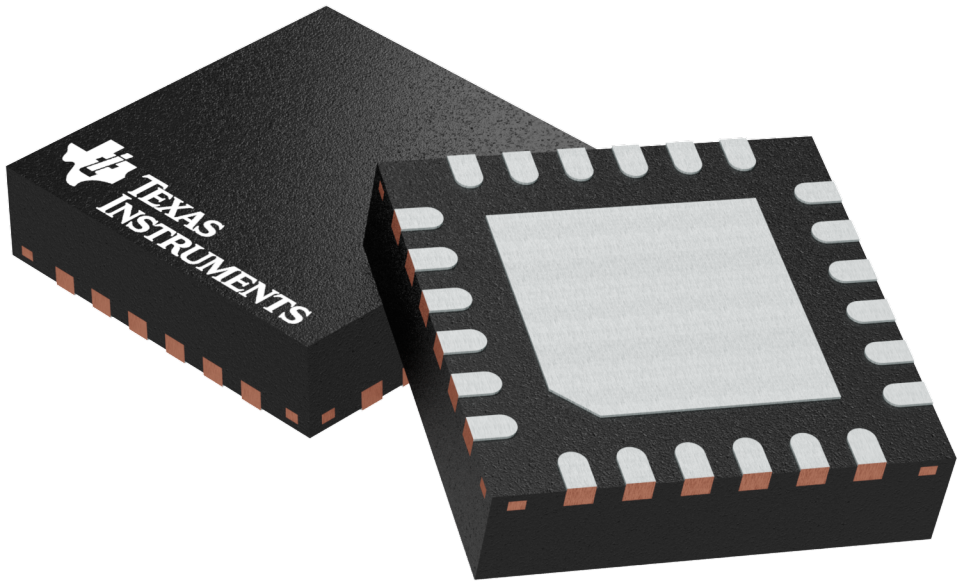
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2340R52E0RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
CC2340R52E0RKPR	VQFN	RKP	40	3000	367.0	367.0	35.0
CC2340R52N0RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
CC2340R52N0RKPR	VQFN	RKP	40	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

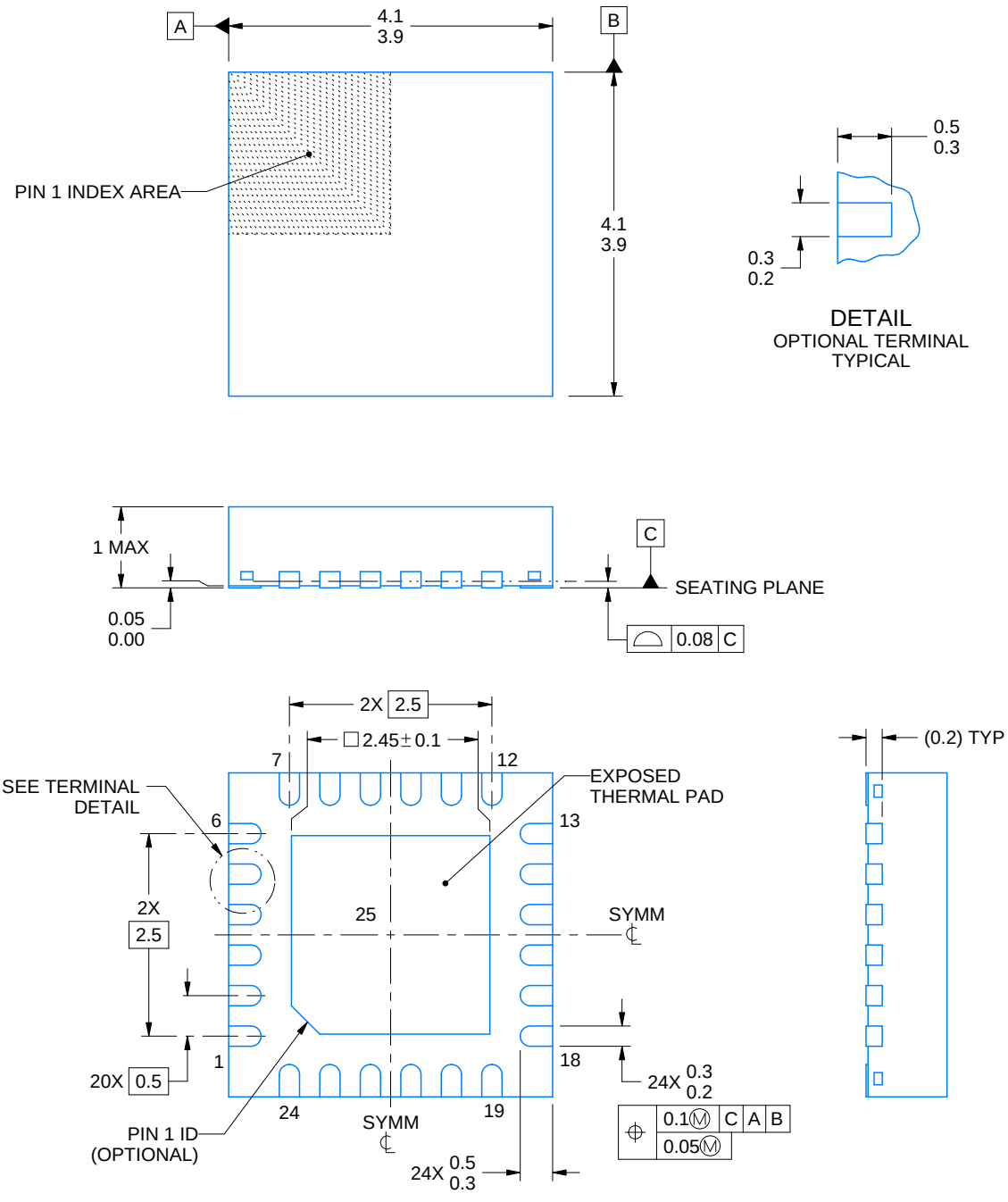
4204104/H

PACKAGE OUTLINE

RGE0024B

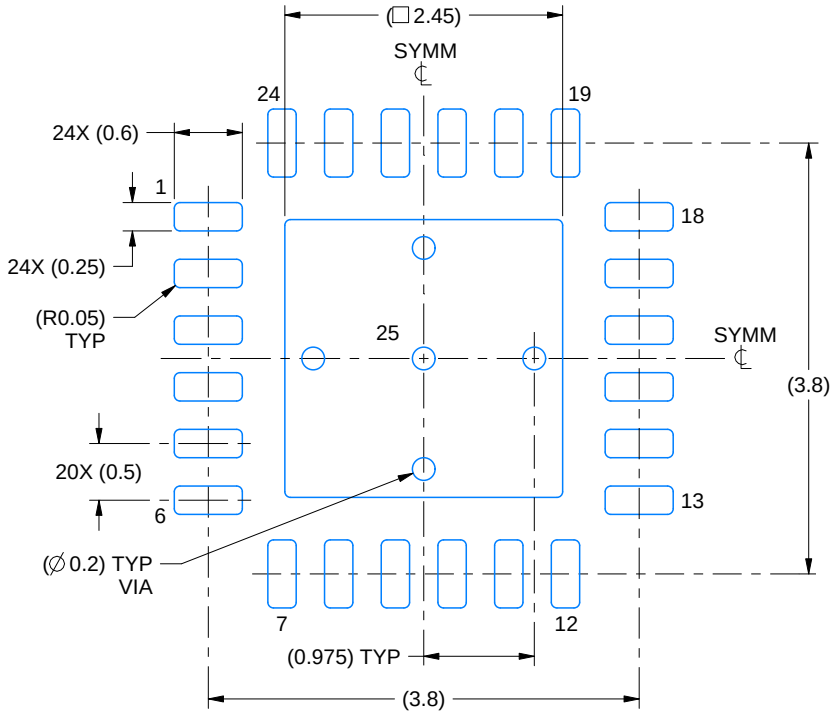
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

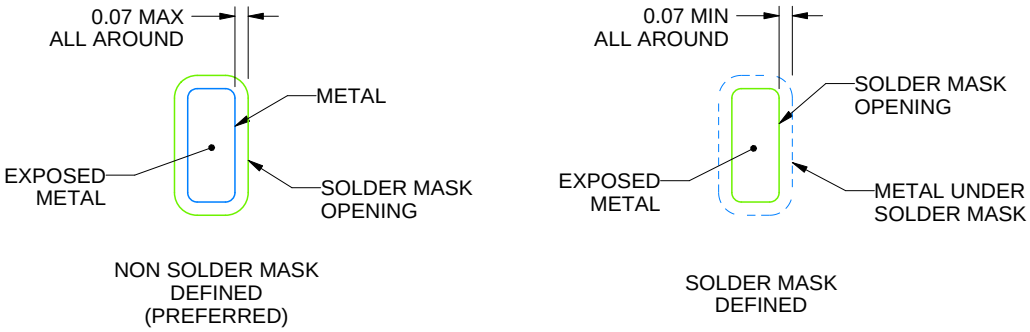


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

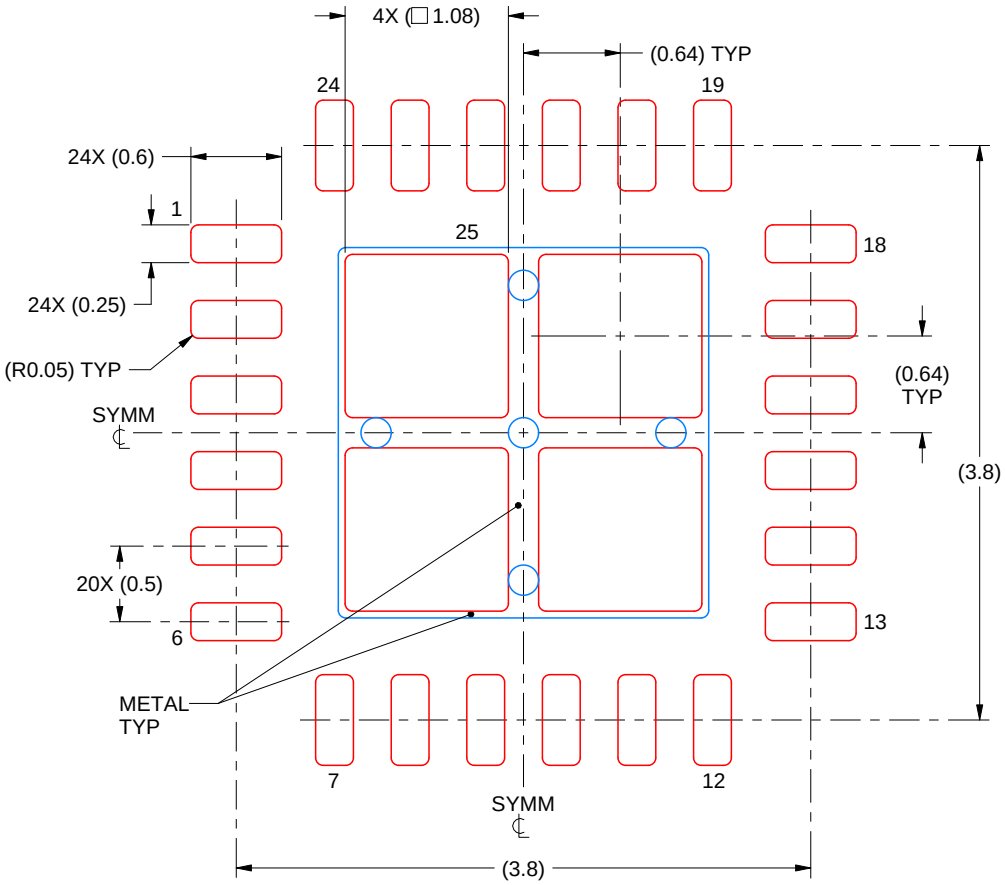


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

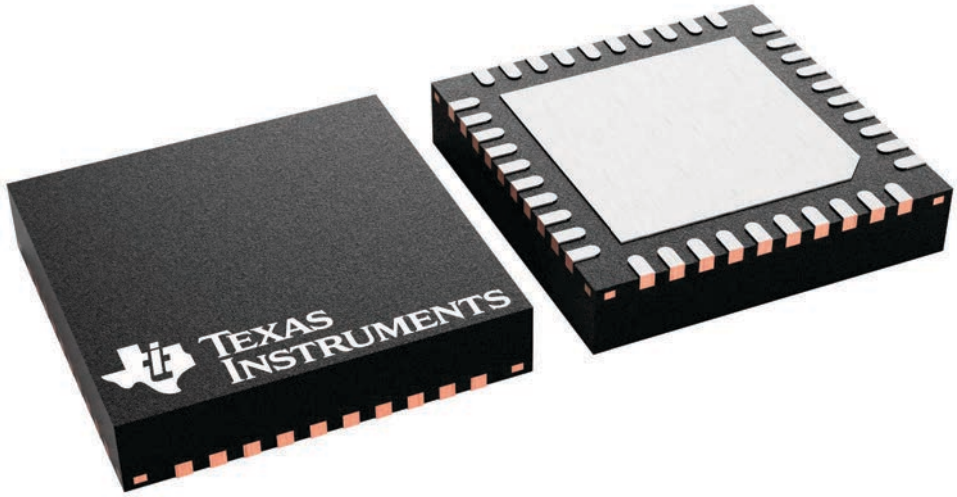
RKP 40

VQFN - 1 mm max height

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



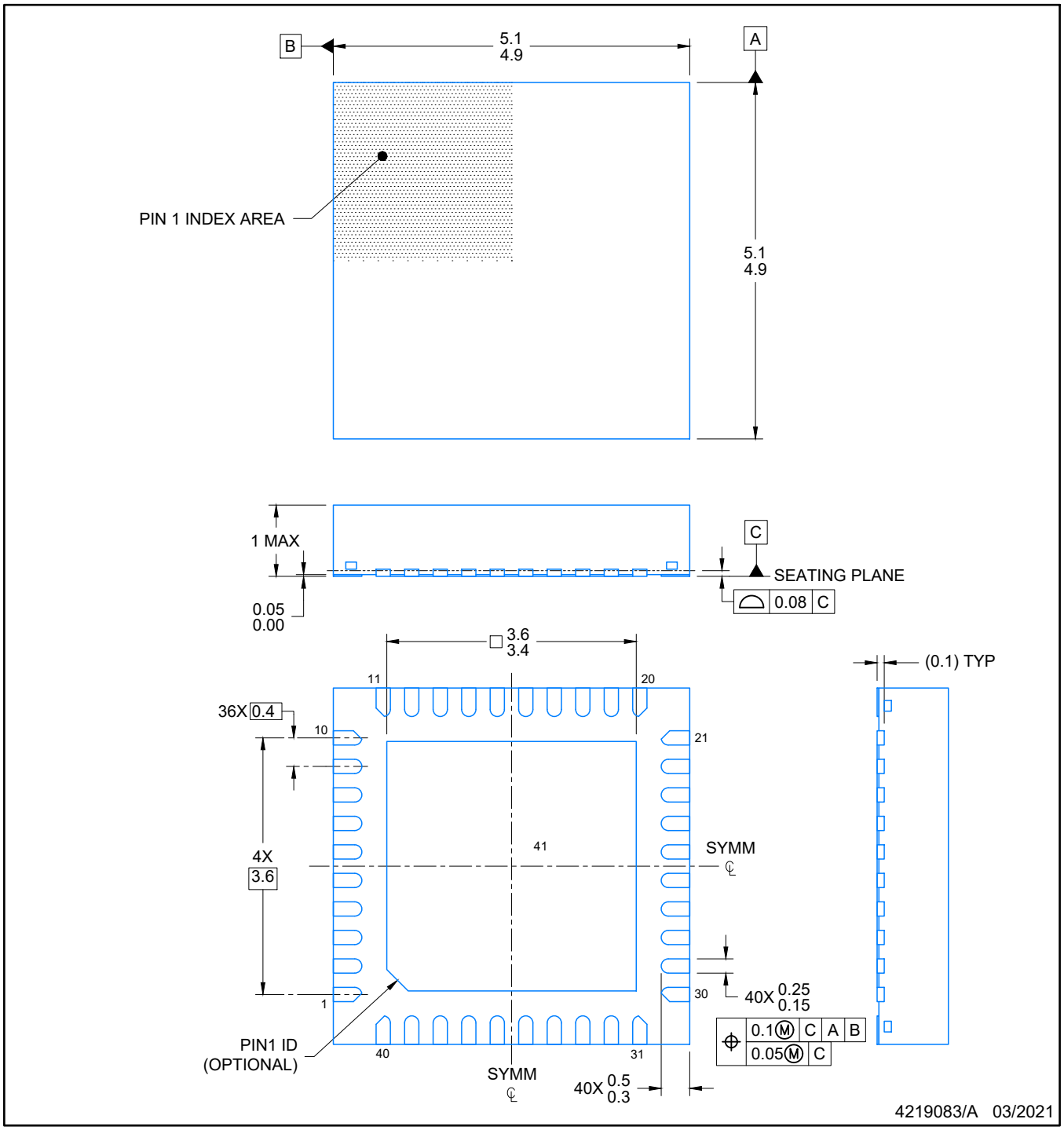
4229305/A

PACKAGE OUTLINE

RKP0040B

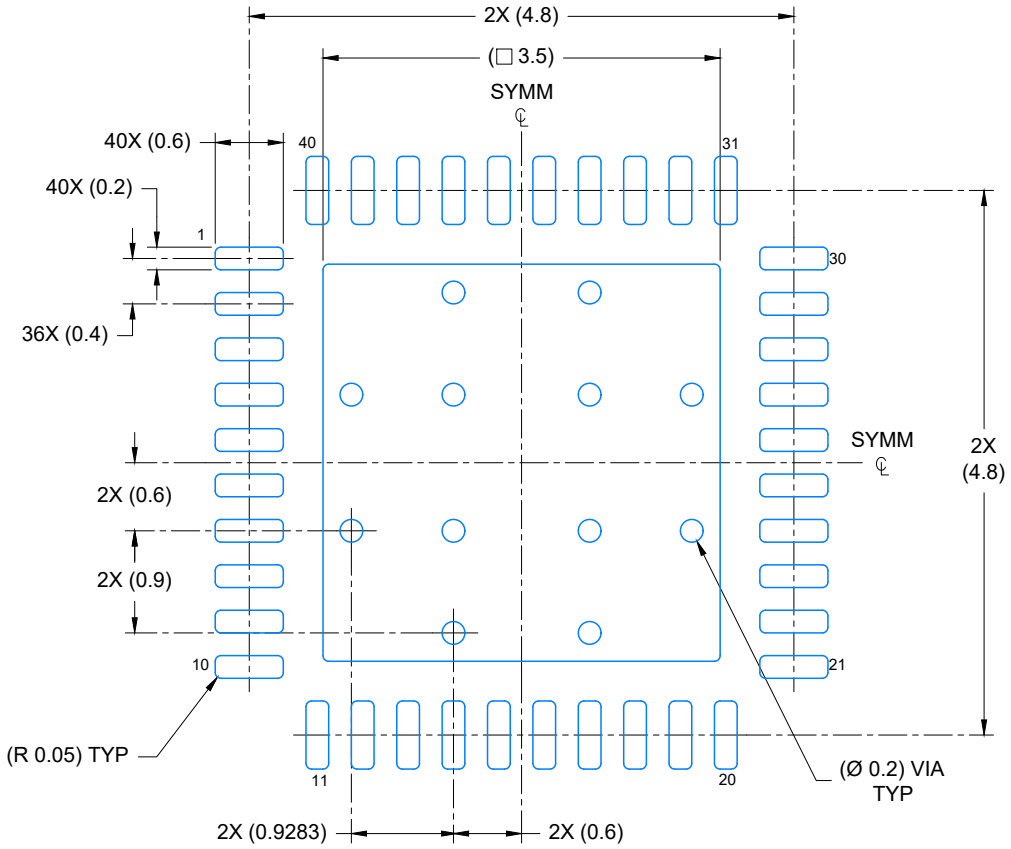
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

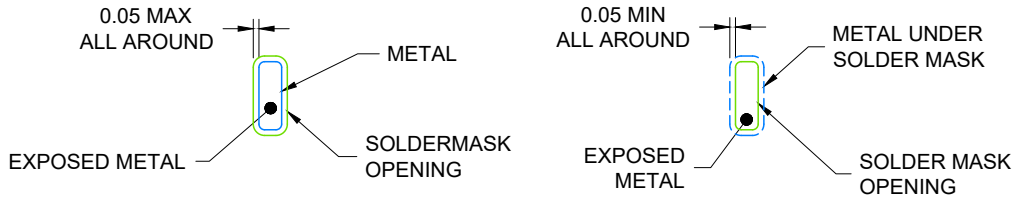


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK DEFINED (PREFERRED)

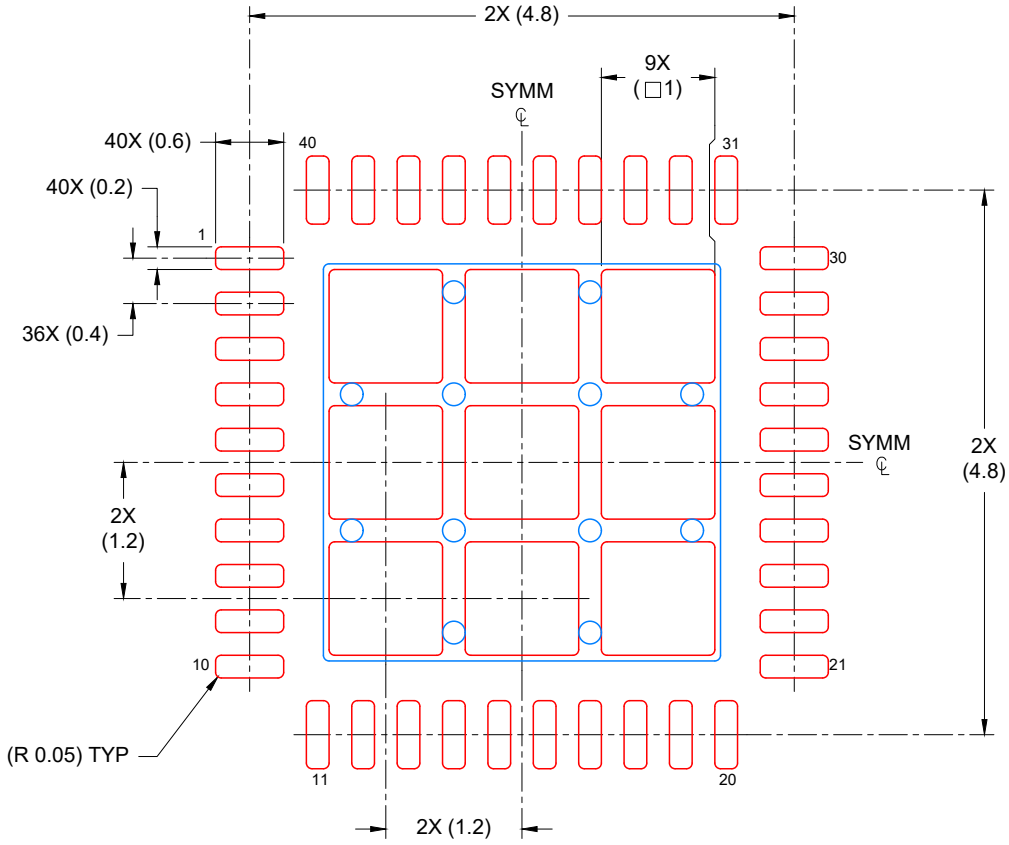
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219083/A 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 15X

4219083/A 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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