CC1200 低功率、高性能射频 (RF) 收发器

1 器件概述

1.1 特性

- RF 性能和模拟特性：
  - 高性能、单芯片收发器
    - 出色的接收器灵敏度：
      - 1.2kbps 时为 -123dBm
      - 50kbps 时为 -109dBm
    - 阻断性能：10MHz 时为 86dB
    - 邻道选择性：12.5kHz 偏移时高达 60dB
    - 极低相位噪声：10kHz 偏移 (169 MHz) 时为 -114dBc/Hz
  - 步长为 0.4dB，高达 +16dBm 的可编程输出功率
  - 自动输出功率斜升
  - 所支持的调制格式：2 - 频移键控 (FSK)，2 - 高斯频移监控 (GFSK)，4-FSK，4-GFSK，最小频移键控 (MSK)，开关键控 (OOK)
  - 发送和接收时支持高达 1.25Mbps 的数据速率
- 低流耗：
  - 针对自动低功率接收轮询的增强型无线电唤醒 (eWOR) 功能
  - 断电：0.12μA（eWOR 定时器激活时为 0.5μA）
    - RX：在 RX 嗅探模式中为 0.5mA
    - RX：在低功耗模式中，峰值电流为 19mA
    - RX：在高性能模式中，峰值电流为 23mA
    - TX: +14dBm 时为 46mA
- 其他：
  - 数据先入先出 (FIFO)：独立的 128 字节 RX 和 TX
  - 支持与 CC1190 器件无缝集成以实现范围扩展，从而使 RX 灵敏度提升 3dB 并且实现高达 +27dBm 的 TX 输出功率
- 数字特性：
  - 波形监视：针对经改进同步检测性能的高级数字信号处理
  - 安全性：硬件 AES128 加速器
  - 数据先入先出 (FIFO)：独立的 128 字节 RX 和 TX
  - 包括针对天线多样性支持的功能
  - 支持重传
  - 支持接收到的数据包自动确认
  - 针对载波监听 (LBT) 系统的自动空闲信道评估 (CCA)
  - 增加范围和提高稳定耐用性的内置编码增益支持
  - 数字接收信号强度指示 (RSSI) 测量
  - 用于实现更少占用带宽的经改进 OOK 整形，从而在满足规定要求的同时实现更高的输出功率
- 针对 802.15.4g 的专用数据包处理：
  - 循环冗余校验 (CRC) 16/32
  - 前向纠错 (FEC)，双同步检测（FEC 和无 FEC 数据包）
  - 数据白化
- 总体说明：
  - 符合 RoHS 标准的 5mm × 5mm 无脚四方扁平无引线 (QFN) 32 引脚封装 (RHB)
  - 与 CC1120 器件引脚兼容
- 法规 - 适用于符合下列标准的系统
  - 欧洲： ETSI EN 300 220，EN 54-25
  - 美国： FCC CFR47 部分 15，FCC CFR47 部分 90
  - 日本： ARIB STD-T30，T67，T108

1.2 应用

- 数据速率高达 1250kbps 的低功耗高性能无线系统
- ISM/SRD 频带：169、433、868、915 和 920MHz
- 有可能支持额外的频率频带：137 至 158.3MHz，205 至 237.5MHz，以及 274 至 316.6MHz
- 智能仪表计量（自动计量读取 (AMR) / 自动计量基础设施 (AMI)）
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业用监控和控制
- 无线医疗应用
- 无线传感器网络和有源射频识别 (RFID)
- IEEE 802.15.4g 应用
- 无线仪表总线 (M-bus)，全部模式

1.3 说明

CC1200 器件是一款全集成单芯片射频收发器，此器件设计用于在成本有效无线系统中实现极低功耗和低压运行的高性能。 所有滤波器都已集成，因此无需昂贵的外部表面声波 (SAW) 和中频 (IF) 滤波器。 该器件主要用于 ISM（工业、科学和医疗）以及处于 164-190MHz，410-475MHz 和 820-950MHz 的 SRD（短程设备）频带。

CC1200 器件提供广泛硬件支持，以实现数据包处理、数据缓冲、突发传输、空闲信道评估、链路质量指示和无线电唤醒。 CC1200 器件的主要运行参数可由 SPI 接口控制。 在典型系统中，CC1200 器件将与一个微控制器和极少的外部无源组件配合使用。

CC1200 和 CC1120 器件都是高性能收发器系列产品。 CC1120 器件多针对窄带应用进行了优化，而 CC1200 器件则针对宽带应用进行了优化，但是它也能够有效涵盖低至 12.5kHz 信道的窄带应用。

器件信息(1)

部件号	封装	封装尺寸
CC1200RHB	超薄四方扁平无引线 (VQFN) (32)	5.00mm x 5.00mm

(1) 更多信息请参见 节 8，*机械封装和可订购产品信息*

1.4 功能方框图

图 1-1 显示 CC120x 系列器件的系统方框图。

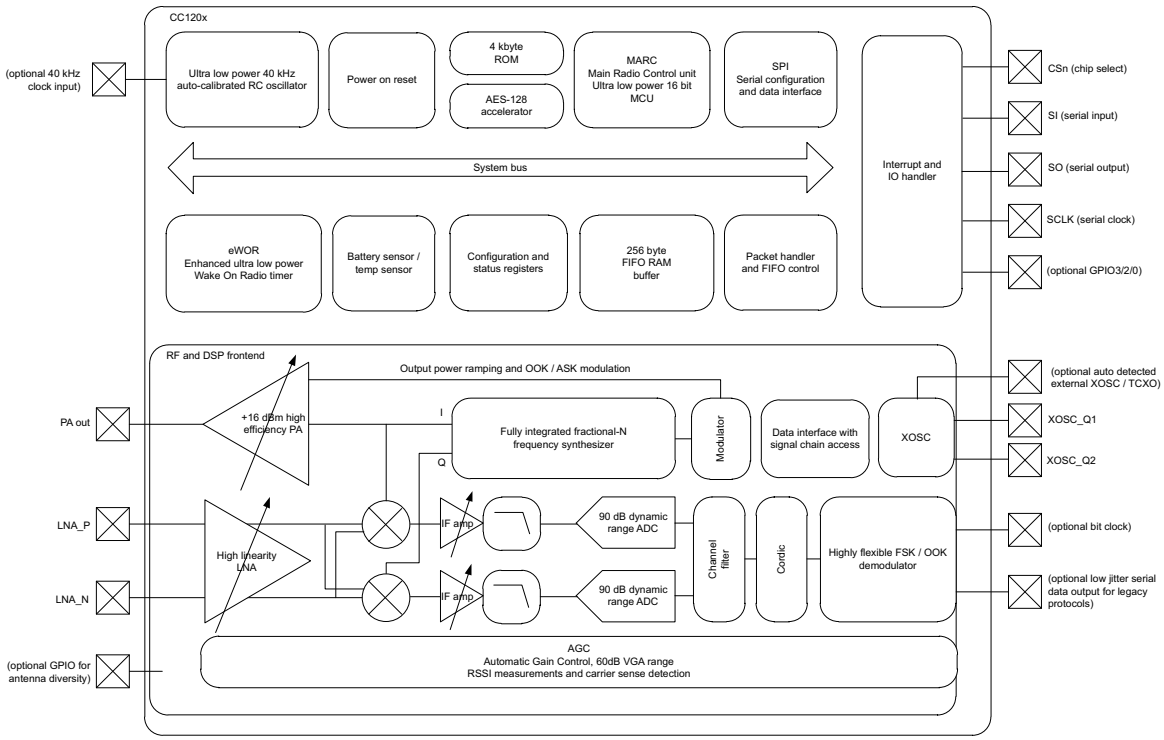


图 **1-1.** 功能方框图

内容

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

本数据手册修订历史记录强调了使 SWRS123C 器件专用数据手册变为 SWRS123D 修订版本所做的更改。

Changes from Revision C (June 2014) to Revision D	Page
• Added Ambient to the temperature range condition and removed Tj from Temperature range	7
• Added data to TCXO table	15

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1200 device.

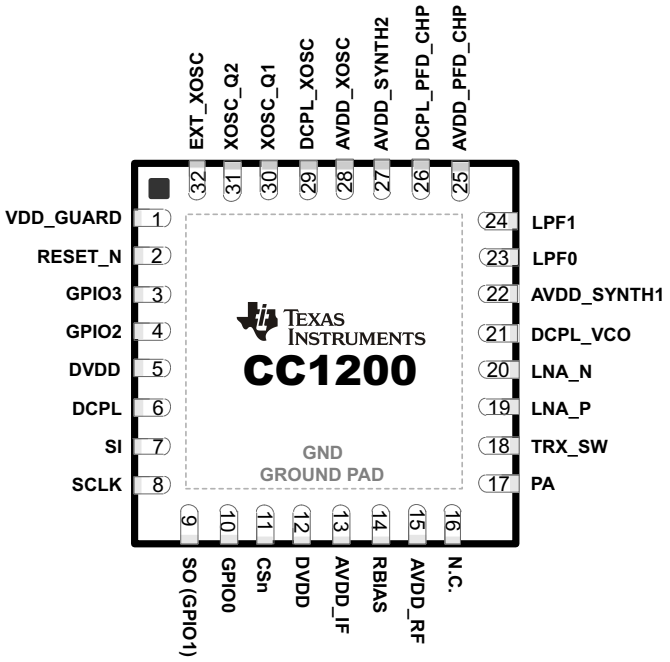


Figure 3-1. Package 5-mm × 5-mm QFN

3.2 Pin Configuration

The following table lists the pin-out configuration for the CC1200 device.

PIN NO.	PIN NAME	TYPE / DIRECTION	DESCRIPTION
1	VDD_GUARD	Power	2.0–3.6 V VDD
2	RESET_N	Digital input	Asynchronous, active-low digital reset
3	GPIO3	Digital I/O	General-purpose I/O
4	GPIO2	Digital I/O	General-purpose I/O
5	DVDD	Power	2.0–3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital input	Serial data in
8	SCLK	Digital input	Serial data clock
9	SO(GPIO1)	Digital I/O	Serial data out (general-purpose I/O)
10	GPIO0	Digital I/O	General-purpose I/O
11	CSn	Digital input	Active-low chip select
12	DVDD	Power	2.0–3.6 V VDD
13	AVDD_IF	Power	2.0–3.6 V VDD
14	RBIAS	Analog	External high-precision resistor
15	AVDD_RF	Power	2.0–3.6 V VDD
16	N.C.		Not connected
17	PA	Analog	Single-ended TX output (requires DC path to VDD)
18	TRX_SW	Analog	TX and RX switch. Connected internally to GND in TX and floating (high-impedance) in RX.
19	LNA_P	Analog	Differential RX input (requires DC path to ground)
20	LNA_N	Analog	Differential RX input (requires DC path to ground)
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0–3.6 V VDD
23	LPF0	Analog	External loop filter components
24	LPF1	Analog	External loop filter components
25	AVDD_PFD_CHP	Power	2.0–3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0–3.6 V VDD
28	AVDD_XOSC	Power	2.0–3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital input	Pin for external clock input (must be grounded if a regular crystal connected to XOSC_Q1 and XOSC_Q2 is used)
–	GND	Ground pad	The ground pad must be connected to a solid ground plane.

4 Specifications

All measurements performed on CC1200EM_868_930 rev.1.0.0, CC1200EM_420_470 rev.1.0.1, or CC1200EM_169 rev.1.2.

4.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT	CONDITION
Supply voltage (VDD, AVDD_x)	–0.3	3.9	V	All supply pins must have the same voltage
Input RF level		+10	dBm	
Voltage on any digital pin	–0.3	VDD+0.3	V	max 3.9 V
Voltage on analog pins (including DCPL pins)	–0.3	2.0	V	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under general characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–40	125	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)		–2	2	kV
		Charged device model (CDM), per JESD22-C101(2)	All pins	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions (General Characteristics)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Voltage supply range	2.0		3.6	V	All supply pins must have the same voltage
Voltage on digital inputs	0		VDD	V	
Temperature range	–40		85	°C	Ambient

4.4 Thermal Resistance Characteristics for RHB Package

		°C/W(1)	AIR FLOW (m/s)(2)
$R\theta_{JC}$	Junction-to-case (top)	21.1	0.00
$R\theta_{JB}$	Junction-to-board	5.3	0.00
$R\theta_{JA}$	Junction-to-free air	31.3	0.00
Psi_{JT}	Junction-to-package top	0.2	0.00
Psi_{JB}	Junction-to-board	5.3	0.00
$R\theta_{JC}$	Junction-to-case (bottom)	0.8	0.00

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 40 mW and an ambient temperature of 25ºC is assumed.
(2) m/s = meters per second

4.5 RF Characteristics

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency bands	820		950	MHz	
	410		475	MHz	
	164		190	MHz	
	(274)		(316.6)	MHz	Contact TI for more information about the use of these frequency bands.
	(205)		(237.5)	MHz	
	(137)		(158.3)	MHz	
Frequency resolution		30		Hz	In 820–950 MHz band
		15		Hz	In 410–475 MHz band
		6		Hz	In 164–190 MHz band
Data rate	0		1250	kbps	Packet mode
	0		625	kbps	Transparent mode

4.6 Regulatory Standards

PERFORMANCE MODE	FREQUENCY BAND	SUITABLE FOR COMPLIANCE WITH	COMMENTS
High-performance mode	820–950 MHz	ARIB STD-T108 ETSI EN 300 220 receiver, categories 2 and 3 FCC Part 15.247 FCC Part 15.249 FCC Part 90 Mask G FCC Part 90 Mask J	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190 device
	410–475 MHz	ARIB STD-T67 ARIB RCR STD-T30 ETSI EN 300 220 receiver, categories 2 and 3 FCC Part 90 Mask D FCC Part 90 Mask G	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164–190 MHz	ETSI EN 300 220 receiver, category 1 FCC Part 90 Mask D	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low-power mode	820–950 MHz	ETSI EN 300 220 receiver, categories 2 and 3 FCC Part 15.247 FCC Part 15.249	
	410–475 MHz	ETSI EN 300 220 receiver, categories 2 and 3	
	164–190 MHz	ETSI EN 300 220	

4.7 Current Consumption, Static Modes

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Power down with retention		0.12	1	µA	
		0.5		µA	Low-power RC oscillator running
XOFF mode		180		µA	Crystal oscillator / TCXO disabled
IDLE mode		1.5		mA	Clock running, system waiting with no radio activity

4.8 Current Consumption, Transmit Modes

4.8.1 868-, 915-, and 920-MHz Bands (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +14 dBm		46		mA	
TX current consumption +10 dBm		36		mA	

4.8.2 433-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		49		mA	
TX current consumption +14 dBm		46		mA	
TX current consumption +10 dBm		35		mA	

4.8.3 169-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		54		mA	
TX current consumption +14 dBm		50		mA	
TX current consumption +10 dBm		39		mA	

4.8.4 Low-Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +10 dBm		33.6		mA	

4.9 Current Consumption, Receive Modes

4.9.1 High-Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
RX Wait for sync 1.2 kbps, 4-byte preamble (50 kHz Channel Filter Bandwidth) 1.2 kbps, 3-byte preamble (11 kHz Channel Filter Bandwidth) 38.4 kbps, 12-byte preamble 50 kbps, 24-byte preamble		 0.5 3.1 3.4 2.1		 mA mA mA mA	Using RX sniff mode, where the receiver wakes up at regular intervals looking for an incoming packet. Sniff mode configured to terminate on Carrier Sense, and is measured using RSSI_VALID _COUNT = 1 (0 for 1.2 kbps with 50 kHz Channel Filter Bandwidth), AGC_WIN_SIZE = 0, and SETTLE_WAIT = 1.(1)
RX Peak Current 1.2kbps		 23.5		 mA	Peak current consumption during packet reception
Average current consumption Check for data packet every 1 second using Wake on Radio		8		µA	50 kbps, 5-byte preamble, 40-kHz RC oscillator used as sleep timer

(1) See the sniff mode design note for more information (SWRA428).

4.9.2 Low-Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
RX Peak Current Low-power RX mode 1.2 kbps		 19		 mA	Peak current consumption during packet reception at the sensitivity limit

4.10 Receive Parameters

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%. Selectivity and blocking is measured with the desired signal 3 dB greater than the sensitivity level.

4.10.1 General Receive Parameters (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Saturation		+10		dBm	
Digital channel filter programmable bandwidth	9.5		1600	kHz	
IIP3		–14		dBm	At maximum gain
Data rate offset tolerance		±14 ±1600		% ppm	With carrier sense detection enabled With carrier sense detection disabled
Spurious emissions 1–13 GHz (VCO leakage at 3.5 GHz) 30 MHz to 1 GHz		 < –56 < –57		 dBm dBm	Radiated emissions measured according to ETSI EN 300 220, f_c = 869.5 MHz
Optimum source impedance 868-, 915-, and 920-MHz bands 433-MHz band 169-MHz band		 60 + j60 / 30 + j30 100 + j60 / 50+ j30 140 + j40 / 70 + j20		 Ω Ω Ω	(Differential or single-ended RX configurations)

4.10.2 RX Performance in 868-, 915-, and 920-MHz Bands (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–122		dBm	1.2 kbps 2-FSK, DEV=4 kHz CHF=11 kHz (1)
		–113		dBm	4.8 kbps OOK
		–108		dBm	32.768 kbps 2-GFSK, DEV=50 kHz CHF=208 kHz (1)
		–110		dBm	38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz (1)
		–109		dBm	50 kbps 2-GFSK, DEV=25 kHz, CHF=104 kHz (1)
		-107		dBm	100-kbps 2-GFSK, DEV=50 kHz, CHF=208 kHz (1)
		–97		dBm	500 kbps 2-GMSK, CHF=833 kHz (1)
		–97		dBm	1 Mbps 4-GFSK, DEV=400 kHz, CHF=1.66 MHz (1)
Blocking and Selectivity 1.2-kbps 2-FSK, 12.5-kHz channel separation, 4-kHz deviation, 11-kHz channel filter		54		dB	± 12.5 kHz (adjacent channel)
		55		dB	± 25 kHz (alternate channel)
		77		dB	± 2 MHz
		82		dB	± 10 MHz
Blocking and Selectivity 32.768-kbps 2-GFSK, 200-kHz channel separation, 50-kHz deviation, 208-kHz channel filter		38		dB	± 200 kHz
		46		dB	± 400 kHz
		66		dB	± 2 MHz
		70		dB	± 10 MHz
Blocking and Selectivity 38.4-kbps 2-GFSK, 100-kHz channel separation, 20-kHz deviation, 104-kHz channel filter		44		dB	+ 100 kHz (adjacent channel)
		44		dB	± 200 kHz (alternate channel)
		64		dB	± 2 MHz
		72		dB	± 10 MHz
Blocking and Selectivity 50-kbps 2-GFSK, 200-kHz channel separation, 25-kHz deviation, 104-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		41		dB	± 200 kHz (adjacent channel)
		46		dB	± 400 kHz (alternate channel)
		65		dB	± 2 MHz
		71		dB	± 10 MHz
Blocking and Selectivity 100-kbps 2-GFSK, 50-kHz deviation, 208-kHz channel filter		45		dB	± 400 kHz (adjacent channel)
		54		dB	± 800 kHz (alternate channel)
		63		dB	± 2 MHz
		68		dB	± 10 MHz
Blocking and Selectivity 500-kbps GMSK, 833-kHz channel filter		42		dB	+ 1 MHz (adjacent channel)
		42		dB	± 2 MHz (alternate channel)
		57		dB	± 10 MHz
Blocking and Selectivity 1-Mbps 4-GFSK, 400-kHz deviation, 1.6-MHz channel filter		46		dB	± 2 MHz (adjacent channel)
		52		dB	± 4 MHz (alternate channel)
		59		dB	± 10 MHz
Image rejection (Image compensation enabled)		56		dB	1.2 kbps, DEV=4 kHz, CHF=10 kHz, image at –125 kHz

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.3 RX Performance in 433-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–123		dBm	1.2 kbps 2-FSK, DEV=4 kHz CHF=11 kHz(1)
		–111		dBm	38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz(1)
Blocking and Selectivity 1.2-kbps 2-FSK, 12.5-kHz channel separation, 4-kHz deviation, 11-kHz channel filter		60		dB	± 12.5 kHz (adjacent channel)
		61		dB	± 25 kHz (alternate channel)
		82		dB	± 2 MHz
		85		dB	± 10 MHz
Blocking and Selectivity 38.4-kbps 2-GFSK, 100-kHz channel separation, 20-kHz deviation, 104-kHz channel filter		49		dB	+ 100 kHz (adjacent channel)
		48		dB	± 200 kHz (alternate channel)
		66		dB	± 2 MHz
		74		dB	± 10 MHz

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.4 RX Performance in 169-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–122		dBm	1.2 kbps 2-FSK, DEV=4 kHz CHF=11 kHz(1)
Blocking and Selectivity 1.2 kbps 2-FSK, 12.5-kHz channel separation, 4-kHz deviation, 11-kHz channel filter		59		dB	± 12.5 kHz (adjacent channel)
		64		dB	± 25 kHz (alternate channel)
		84		dB	± 2 MHz
		86		dB	± 10 MHz
Spurious response rejection 1.2 kbps 2-FSK, 12.5-kHz channel separation, 4-kHz deviation, 11-kHz channel filter		68		dB	Spurious at ± 40 MHz from carrier
Image rejection (Image compensation enabled)		68		dB	1.2 kbps, DEV=4 kHz, CHF=10 kHz, image at –125 kHz

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.10.5 RX Performance in Low-Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Sensitivity		–110		dBm	1.2 kbps 2-FSK, DEV=4 kHz CHF=11 kHz(1)
		–96		dBm	50 kbps 2-GFSK, DEV=25 kHz, CHF=119 kHz(1)
Blocking and Selectivity 50 kbps 2-GFSK, 200-kHz channel separation, 25-kHz deviation, 104-kHz channel filter (Same modulation format as 802.15.4g Mandatory Mode)		41		dB	+ 200 kHz (adjacent channel)
		45		dB	+ 400 kHz (alternate channel)
		62		dB	± 2 MHz
		60		dB	± 10 MHz
Saturation		+10		dBm	

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

4.11 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Max output power		+14		dBm	At 915- and 920-MHz
		+15		dBm	At 915- and 920-MHz with VDD = 3.6 V
		+15		dBm	At 868 MHz
		+16		dBm	At 868 MHz with VDD = 3.6 V
		+15		dBm	At 433 MHz
		+16		dBm	At 433 MHz with VDD = 3.6 V
		+15		dBm	At 169 MHz
		+16		dBm	At 169 MHz with VDD = 3.6 V
Min output power		–12		dBm	Within fine step size range
		–38		dBm	Within coarse step size range
Output power step size		0.4		dB	Within fine step size range
Adjacent channel power		–60		dBc	4-GFSK 9.6 kbps in 12.5-kHz channel, measured in 8.75-kHz bandwidth (ETSI 300 220 compliant)
Spurious emissions (Excluding harmonics) 30 MHz–1 GHz 1–12.75 GHz		 < –57 < –50		 dBm dBm	Transmission at +14 dBm Suitable for systems targeting compliance with ETSI EN 300 220, ETSI EN 54-25, FCC Part 15, FCC Part 90, ARIB STD-T108, ARIB STD-T67, ARIB RCR STD-30 Measured in 1-MHz bandwidth
Harmonics					Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design Suitable for systems targeting compliance with ETSI EN 300-220, ETSI EN 54-25, FCC Part 15, FCC Part 90, ARIB STD-T108, ARIB STD-T67, ARIB RCR STD-30
Second Harm, 169 MHz (ETSI)		–43		dBm	
Third Harm, 169 MHz (ETSI)		–57		dBm	
Fourth Harm, 169 MHz (ETSI)		–63		dBm	
Second Harm, 433 MHz (ETSI)		–59		dBm	
Third Harm, 433 MHz (ETSI)		–51		dBm	
Fourth Harm, 433 MHz (ETSI)		–63		dBm	
Second Harm, 868 MHz (ETSI)		–50		dBm	
Third Harm, 868 MHz (ETSI)		–44		dBm	
Fourth Harm, 868 MHz (ETSI)		–56		dBm	
Second Harm, 915 MHz (FCC)		–58		dBm	
Third Harm, 915 MHz (FCC)		–46		dBm	
Fourth Harm, 915 MHz (FCC)		–62		dBm	
Second Harm, 920 MHz (ARIB)		–65		dBm	
Third Harm, 920 MHz (ARIB)		–60		dBm	
Optimum load impedance					
868-, 915-, and 920-MHz bands		35 + j35		Ω	
433-MHz band		55 + j25		Ω	
169-MHz band		80 + j0		Ω	

4.12 PLL Parameters

4.12.1 High-Performance Mode

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 868-, 915-, and 920-MHz bands 200-kHz loop bandwidth setting		–94		dBc/Hz	± 10 kHz offset
		–96		dBc/Hz	± 100 kHz offset
		–123		dBc/Hz	± 1 MHz offset
		–137		dBc/Hz	± 10 MHz offset
Phase noise in 868-, 915-, and 920-MHz bands 300-kHz loop bandwidth setting		–100		dBc/Hz	± 10 kHz offset
		–102		dBc/Hz	± 100 kHz offset
		–121		dBc/Hz	± 1 MHz offset
		–136		dBc/Hz	± 10 MHz offset
Phase noise in 868-, 915-, and 920-MHz bands 400-kHz loop bandwidth setting		–103		dBc/Hz	± 10 kHz offset
		–104		dBc/Hz	± 100 kHz offset
		–119		dBc/Hz	± 1 MHz offset
		–133		dBc/Hz	± 10 MHz offset
Phase noise in 868-, 915-, and 920-MHz bands 500-kHz loop bandwidth setting		–104		dBc/Hz	± 10 kHz offset
		–106		dBc/Hz	± 100 kHz offset
		–116		dBc/Hz	± 1 MHz offset
		–130		dBc/Hz	± 10 MHz offset
Phase noise in 433-MHz band 300-kHz loop bandwidth setting		–106		dBc/Hz	± 10 kHz offset
		–107		dBc/Hz	± 100 kHz offset
		–127		dBc/Hz	± 1 MHz offset
		–141		dBc/Hz	± 10 MHz offset
Phase noise in 169-MHz band 300-kHz loop bandwidth setting		–114		dBc/Hz	± 10 kHz offset
		–114		dBc/Hz	± 100 kHz offset
		–132		dBc/Hz	± 1 MHz offset
		–142		dBc/Hz	± 10 MHz offset

4.12.2 Low-Power Mode

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 868-, 915-, and 920-MHz bands 200-kHz loop bandwidth setting		–99		dBc/Hz	± 10 kHz offset
		–101		dBc/Hz	± 100 kHz offset
		–121		dBc/Hz	± 1 MHz offset
		–135		dBc/Hz	± 10 MHz offset

4.13 Wake-up and Timing

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated

The turnaround behavior to and from RX and/or TX is highly configurable, and the time it takes will depend on how the device is set up. See the CC120X user guide (SWRU346) for more information.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Powerdown to IDLE		0.24		ms	Depends on crystal
IDLE to RX/TX		133		µs	Calibration disabled
		369		µs	Calibration enabled
RX/TX turnaround		43		µs	
RX-to-RX turnaround		369		µs	With PLL calibration
		0		µs	Without PLL calibration
TX-to-TX turnaround		369		µs	With PLL calibration
		0		µs	Without PLL calibration
RX/TX to IDLE time		237		µs	Calibrate when leaving RX/TX enabled
		0		µs	Calibrate when leaving RX/TX disabled
Frequency synthesizer calibration		314		µs	When using SCAL strobe
Minimum required number of preamble bytes		0.5		bytes	Required for RF front-end gain settling only. Digital demodulation does not require preamble for settling.
Time from start RX until valid RSSI (1) Including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy)		4.2		ms	12.5-kHz channels
		0.25		ms	120-kHz channels

(1) See the design note on RSSI and response time. It is written for the CC112X devices, but the same principles apply for the CC1200 device.

4.14 40-MHz Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Crystal frequency	38.4		40	MHz	It is expected that there will be degraded sensitivity at multiples of XOSC/2 in RX, and an increase in spurious emissions when the RF channel is close to multiples of XOSC in TX. We recommend that the RF channel is kept RX_BW/2 away from XOSC/2 in RX, and that the level of spurious emissions be evaluated if the RF channel is closer than 1 MHz to multiples of XOSC in TX.
Load capacitance (C_L)		10		pF	
ESR			60	Ω	Simulated over operating conditions
Start-up time		0.24		ms	Depends on crystal

4.15 40-MHz Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency	38.4		40	MHz	
TCXO with CMOS output					TCXO with CMOS output directly coupled to pin EXT_OSC
High input voltage	1.4		VDD	V	
Low input voltage	0		0.6	V	
Rise / Fall time			2	ns	
Clipped sine output					TCXO clipped sine output connected to pin EXT_OSC through series capacitor
Clock input amplitude (peak-to-peak)	0.8		1.5	V	

4.16 32-kHz Clock Input

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency		32		kHz	
32-kHz clock input pin input high voltage	0.8 x VDD			V	
32-kHz clock input pin input low voltage			0.2 x VDD	V	

4.17 40-kHz RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency		40		kHz	After calibration (frequency calibrated against the 40-MHz crystal or TCXO)
Frequency accuracy after calibration		±0.1		%	Relative to frequency reference (that is, 40-MHz crystal or TCXO)
Initial calibration time		1.32		ms	

4.18 I/O and Reset

T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Logic input high voltage	0.8 x VDD			V	
Logic input low voltage			0.2 x VDD	V	
Logic output high voltage	0.8 x VDD			V	At 4-mA output load or less
Logic output low voltage			0.2 x VDD	V	
Power-on reset threshold		1.3		V	Voltage on DVDD pin

4.19 Temperature Sensor

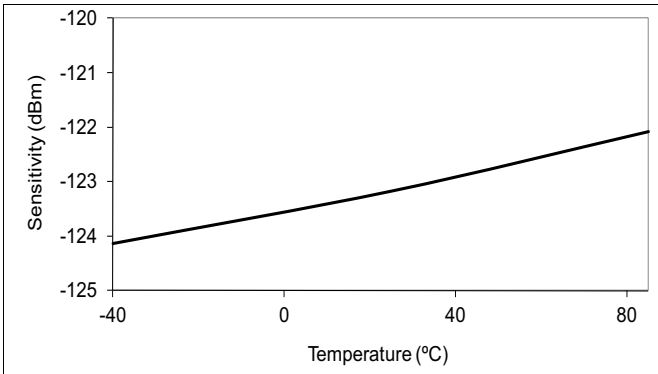
T_A = 25°C, VDD = 3.0 V if nothing else stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Temperature sensor range	–40		85	°C	
Temperature coefficient		2.66		mV / °C	Change in sensor output voltage versus change in temperature
Typical output voltage		794		mV	Typical sensor output voltage at TA = 25°C, VDD = 3.0 V
VDD coefficient		1.17		mV / V	Change in sensor output voltage versus change in VDD

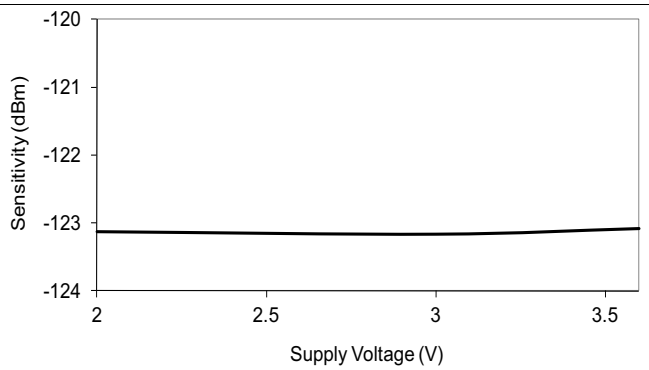
The CC1200 device can be configured to provide a voltage proportional to temperature on GPIO1. The temperature can be estimated by measuring this voltage (see Section 4.19, *Temperature Sensor*). For more information, see the temperature sensor design note (SWRA415).

4.20 Typical Characteristics

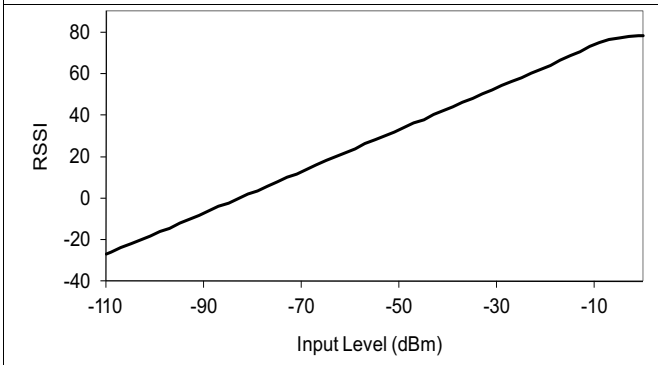
T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else stated



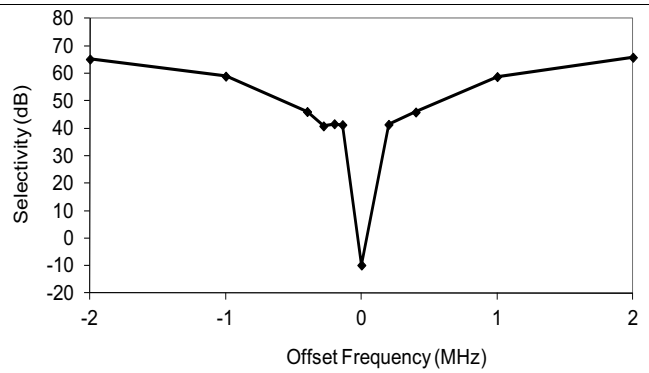
1.2 kbps, 4-kHz Deviation, 11-kHz Channel Filter Bandwidth
Figure 4-1. Sensitivity vs Temperature (434 MHz)



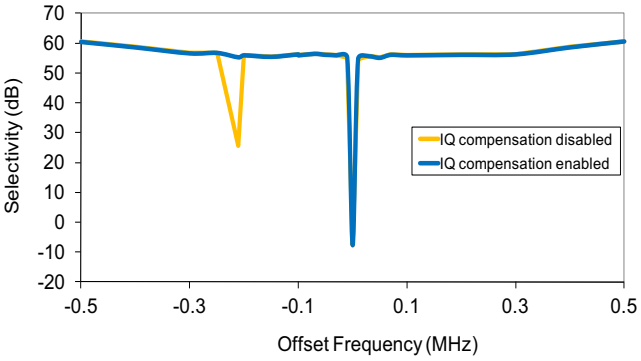
1.2 kbps, 4-kHz Deviation, 11-kHz Channel Filter Bandwidth
Figure 4-2. Sensitivity vs Temperature (434 MHz)



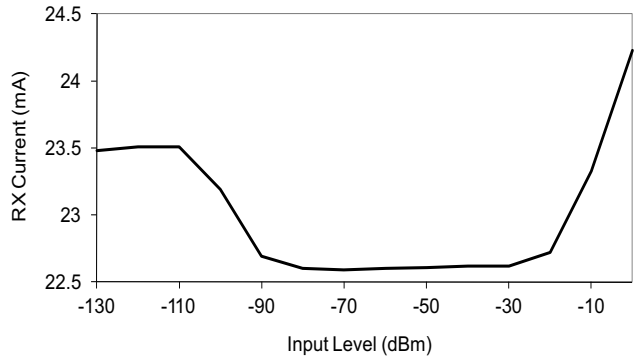
50 kbps GFSK, 25-kHz Deviation, 104-kHz Channel Filter Bandwidth
Figure 4-3. RSSI vs Input Level



50 kbps, 25-kHz Deviation, 104-kHz Channel Filter Bandwidth; Image Frequency at –0.28-MHz Offset (Compensation Enabled)
Figure 4-4. Selectivity vs Offset Frequency (100-kHz Channels)

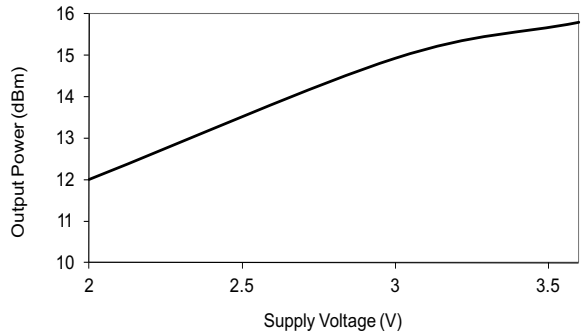


1.2 kbps, 4-kHz Deviation, 11-kHz Channel Filter Bandwidth; Image Frequency at –0.21-MHz Offset
Figure 4-5. Selectivity vs Offset Frequency (12.5-kHz Channels)

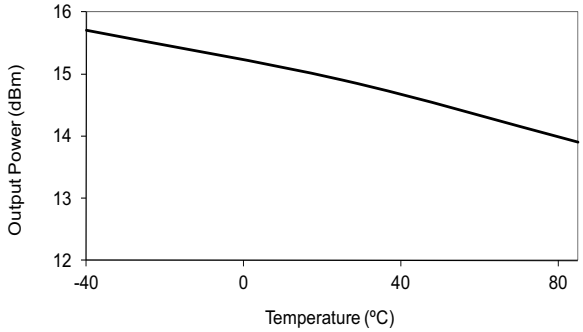


1.2 kbps FSK, 4-kHz Deviation, 11-kHz Channel Filter Bandwidth
Figure 4-6. RX Current vs Input Level

Typical Characteristics *(continued)*



Maximum Output Power Setting (0x7F)
Figure 4-7. Output Power vs Supply Voltage



Maximum Power Setting (0x7F)
Figure 4-8. Output Power vs Temperature

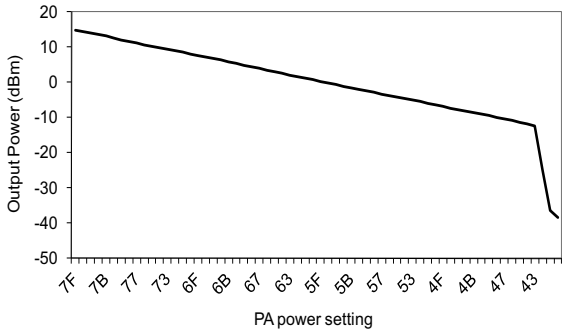


Figure 4-9. Output Power at 868 MHz PA Power Setting

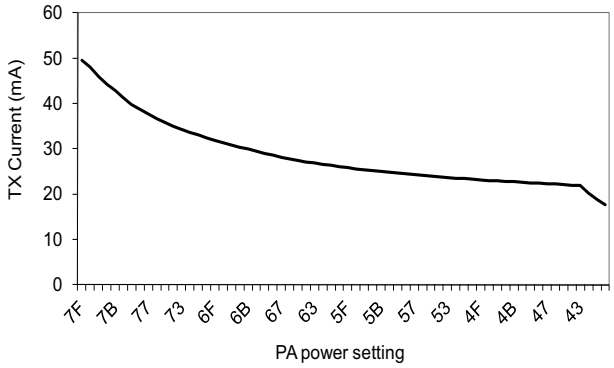
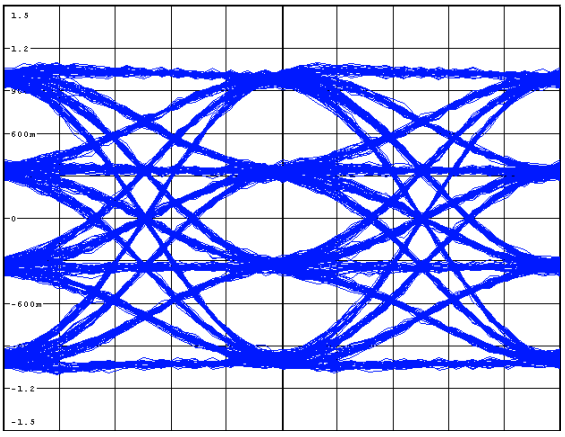
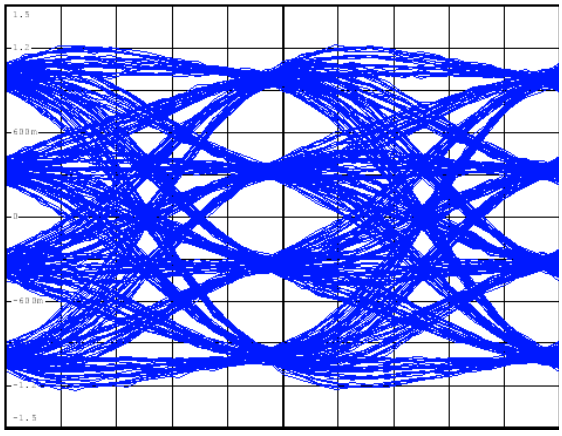


Figure 4-10. TX Current at 868 MHz vs PA Power Setting

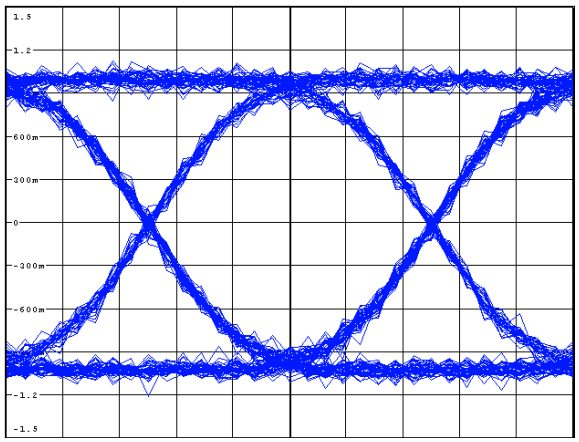


1 Mbps 4-GFSK, 400-kHz Deviation, 500-kHz Loop Bandwidth
Figure 4-11. Eye Diagram



1 Mbps 4-GFSK, 400-kHz Deviation, 300-kHz Loop Bandwidth
Figure 4-12. Eye Diagram

Typical Characteristics *(continued)*



50 kbps GFSK, 25-kHz Deviation, 200-kHz Loop Bandwidth

Figure 4-13. Eye Diagram

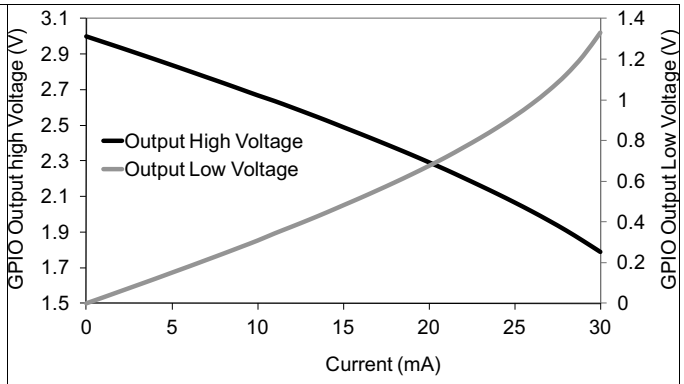
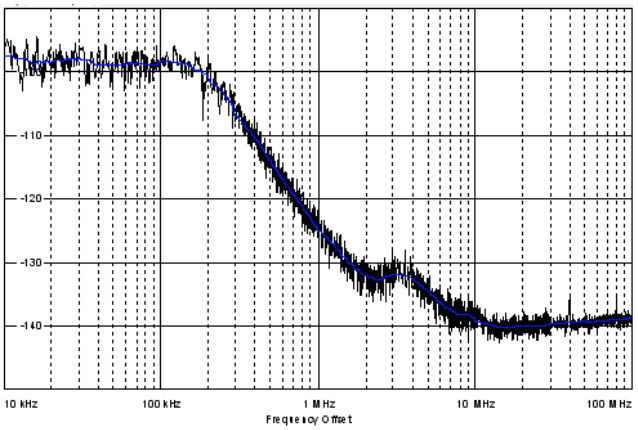
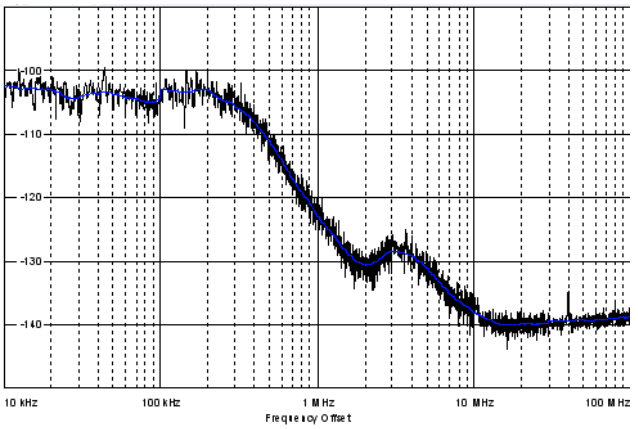


Figure 4-14. GPIO Output High and Low Voltage vs Current Being Sourced and Sinked



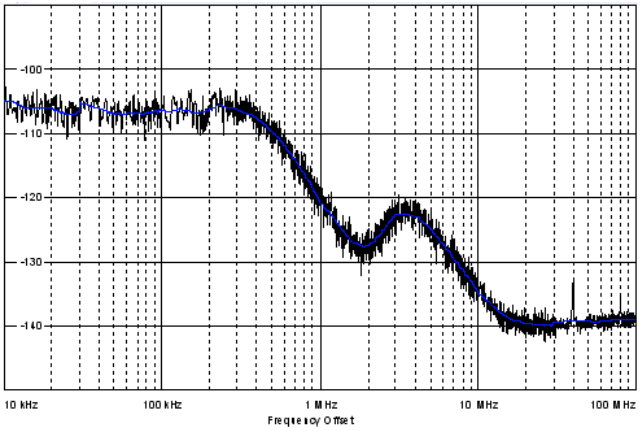
200-kHz Loop Bandwidth

Figure 4-15. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)



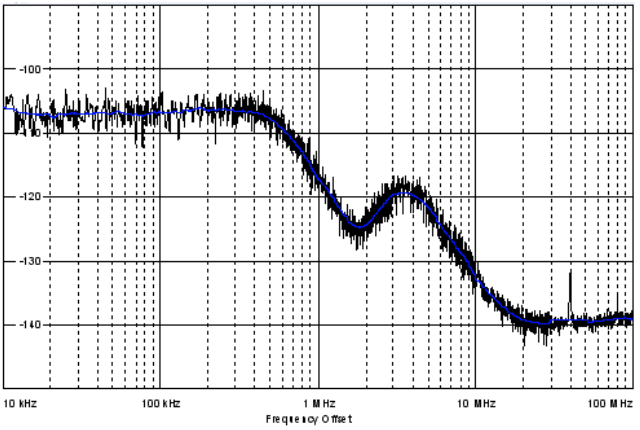
300-kHz Loop Bandwidth

Figure 4-16. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)



400-kHz Loop Bandwidth

Figure 4-17. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)



500-kHz Loop Bandwidth

Figure 4-18. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)

5 Detailed Description

5.1 Block Diagram

Figure 5-1 shows the system block diagram of the CC120x family of devices.

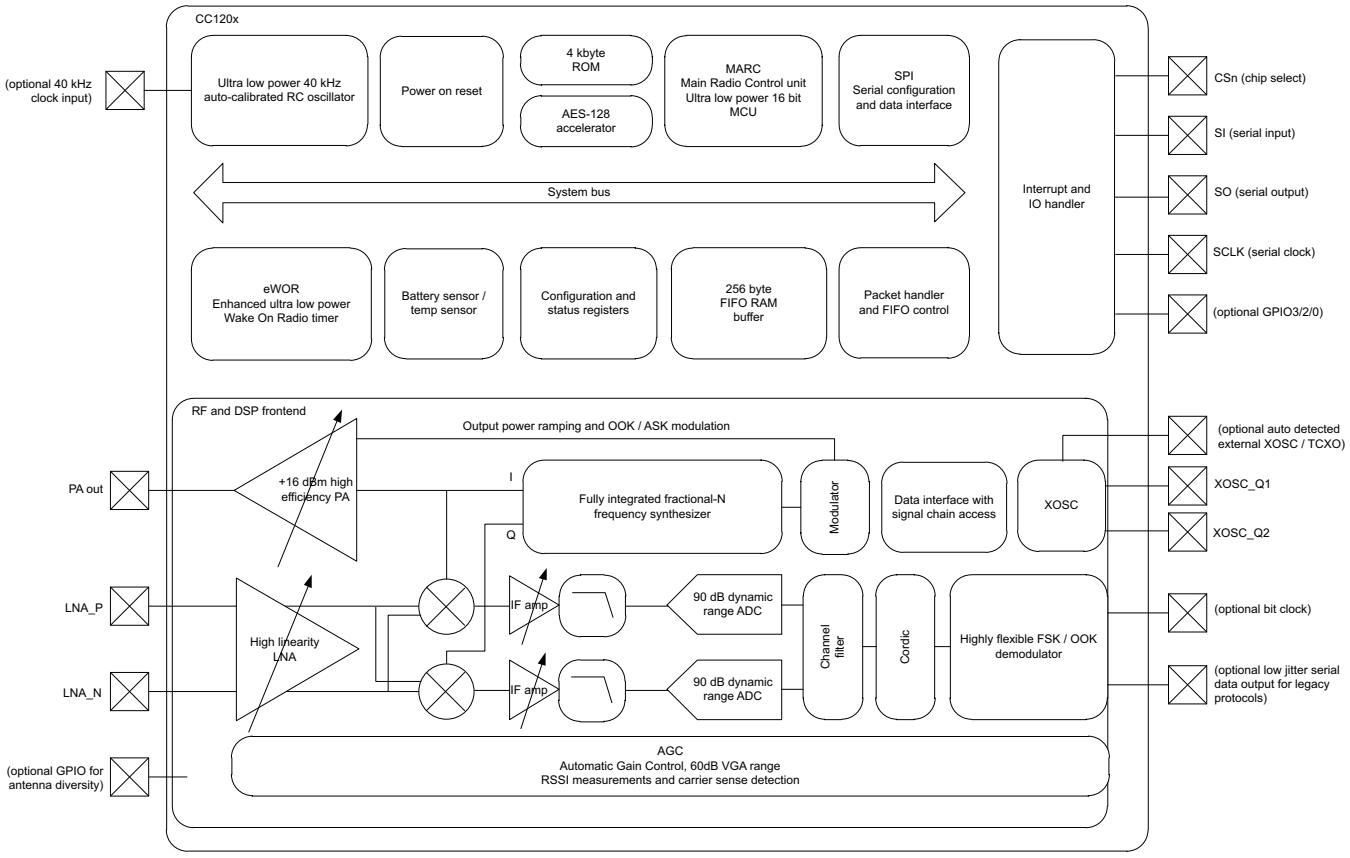


Figure 5-1. System Block Diagram

5.2 Frequency Synthesizer

At the center of the CC1200 device there is a fully integrated, fractional-N, ultra-high-performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, providing very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the analog-to-digital converter (ADC) and the digital part. To reduce system cost, the CC1200 device has high-accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies. This compensation enables the use of lower cost crystals. If a TCXO is used, the CC1200 device automatically turns on and off the TCXO when needed to support low-power modes and Wake-On-Radio operation.

5.3 Receiver

The CC1200 device features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and is down-converted in quadrature (I/Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic-range ADCs.

An advanced automatic gain control (AGC) unit adjusts the front-end gain, and enables the CC1200 device to receive strong and weak signals, even in the presence of strong interferers. High-attenuation channels and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase and magnitude signal to support the FSK and OOK modulation schemes.

NOTE

A unique I/Q compensation algorithm removes any problem of I/Q mismatch, thus avoiding time-consuming and costly I/Q image calibration steps.

5.4 Transmitter

The CC1200 transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To use the spectrum effectively, the CC1200 device has extensive data filtering and shaping in TX mode to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high-power RF amplifiers.

5.5 Radio Control and User Interface

The CC1200 digital control system is built around the main radio control (MARC), which is implemented using an internal high-performance, 16-bit ultra-low-power processor. MARC handles power modes, radio sequencing, and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in power-down mode until a valid RF packet is received. This greatly reduces power consumption. When the host MCU receives a valid RF packet, it burst-reads the data. This reduces the required computing power.

The CC1200 radio control and user interface are based on the widely used CC1101 transceiver. This relationship enables an easy transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats, the CC1200 device also supports two serial modes.

- Synchronous serial mode: The CC1200 device performs bit synchronization and provides the MCU with a bit clock with associated data.
- Transparent mode: The CC1200 device outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

5.6 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. When the CC1200 device enters RX mode, it listens and then returns to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra-low-power RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

5.7 RX Sniff Mode

The CC1200 device supports quick start up times, and requires few preamble bits. RX Sniff Mode uses these conditions to dramatically reduce the current consumption while the receiver is waiting for data.

Because the CC1200 device can wake up and settle much faster than the duration of most preambles, it is not required to be in RX mode continuously while waiting for a packet to arrive. Instead, the enhanced Wake-On-Radio feature can be used to put the device into sleep mode periodically. By setting an appropriate sleep time, the CC1200 device can wake up and receive the packet when it arrives with no performance loss. This sequence removes the need for accurate timing synchronization between transmitter and receiver, and lets the user trade off current consumption between the transmitter and receiver.

For more information, see the RX Sniff Mode design note (SWRA428).

5.8 Antenna Diversity

Antenna diversity can increase performance in a multipath environment. An external antenna switch is required. The CC1200 device uses one of the GPIO pins to automatically control the switch. This device also supports differential output control signals typically used in RF switches.

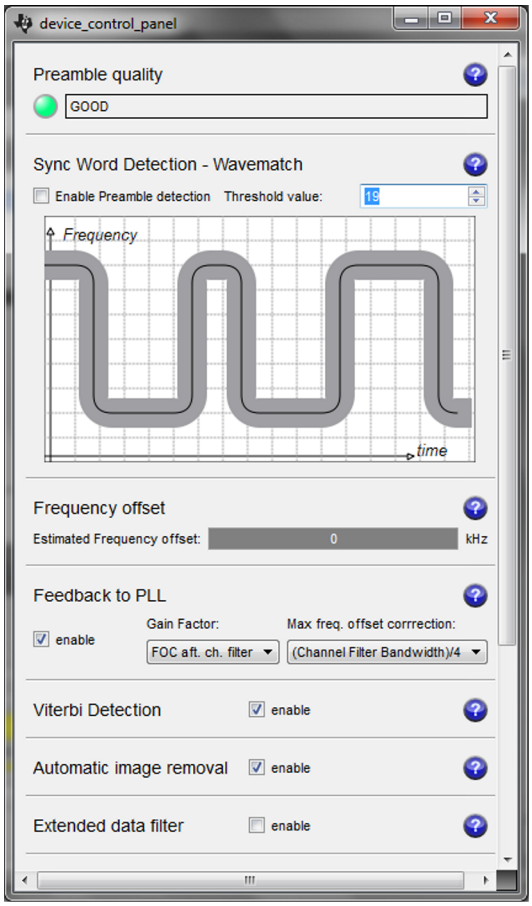
If antenna diversity is enabled, the GPIO alternates between high and low states until a valid RF input signal is detected. An optional acknowledge packet can be transmitted without changing the state of the GPIO.

An incoming RF signal can be validated by received signal strength or by using the automatic preamble detector. Using the automatic preamble detector ensures a more robust system and avoids the need to set a defined signal strength threshold (such a threshold sets the sensitivity limit of the system).

5.9 WaveMatch

Advanced capture logic locks onto the synchronization word and does not require preamble settling bytes. Therefore, receiver settling time is reduced to the settling time of the AGC, typically 4 bits.

The WaveMatch feature also greatly reduces false sync triggering on noise, further reducing the power consumption and improving sensitivity and reliability. The same logic can also be used as a high-performance preamble detector to reliably detect a valid preamble in the channel.



See SWRC046 for more information.

Figure 5-2. Receiver Configurator in SmartRF™ Studio

6 Typical Application Circuit

NOTE

This section is intended only as an introduction.

Very few external components are required for the operation of the CC1200 device. Figure 6-1 shows a typical application circuit. The board layout will greatly influence the RF performance of the CC1200 device. Also, Figure 6-1 does not show decoupling capacitors for power pins.

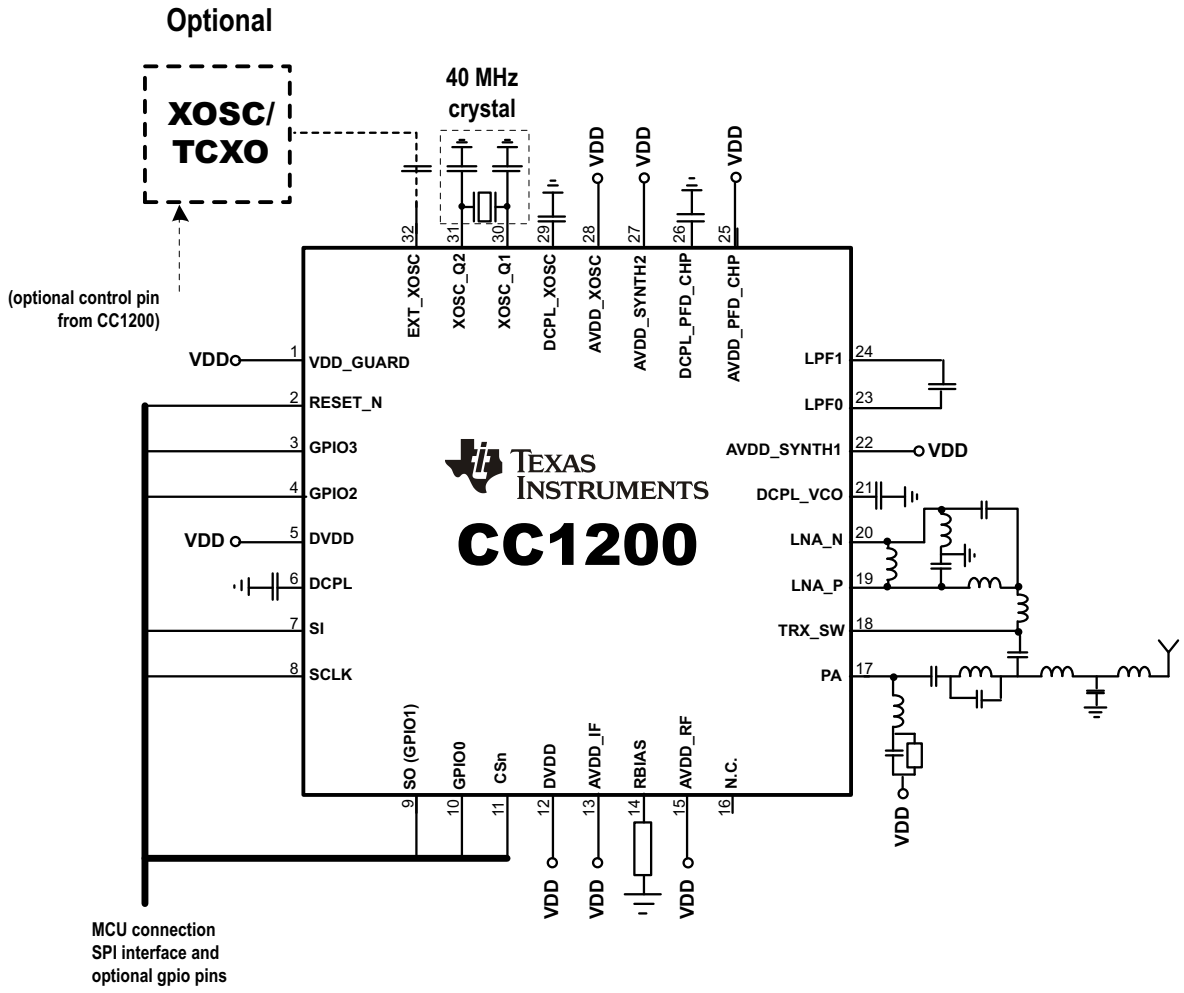


Figure 6-1. Typical Application Circuit

For more information, see the reference designs available for the CC1200 device in 节 7.2, *Documentation Support*.

7 器件和文档支持

7.1 器件支持

7.1.1 开发支持

7.1.1.1 配置软件

CC1200 器件可使用 SmartRF Studio 软件 (SWRC046) 进行配置。 强烈建议使用 SmartRF Studio 软件来获取最优寄存器设置并评估相关性能和功能。

7.1.2 器件和支持开发工具命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。 每个器件都具有以下三个前缀中的一个：X、P 或无（无前缀）（例如，CC1200）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。 这些前缀代表了产品开发的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发发展流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

TMDS 完全合格的开发支持产品.

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀表示封装类型（例如，RHB），且温度范围（例如，“空白”是默认的商业级温度范围）提供了读取任一 CC1200 器件完整器件名称的图例。

要获得 QFN 封装类型的 CC1200 器件订购部件号，请参见本文档的“封装选项附录”（TI 网站 www.ti.com），或者联系您的 TI 销售代表。

7.2 文档支持

以下文档对 CC1200 处理器加以补充。 www.ti.com 网站上提供了这些文档的副本。 *提示：*请在 www.ti.com 上提供的搜索框中输入文献编号。

SWRR106 CC112x IPC 868MHz 和 915MHz 2 层参考设计

SWRR107 CC112x IPC 868MHz 和 915MHz 4 层参考设计

SWRR122 CC1200EM 420MHz 至 470MHz 参考设计

SWRR121 CC1200EM 868MHz 至 930MHz 参考设计

SWRC046 SmartRF Studio 软件

SWRA428 CC112x/CC120x 嗅探模式应用手册

7.3 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

TI E2E™ 在线社区 ***TI 工程师对工程师 (E2E) 社区。*** **此社区的创建目的是为了促进工程师之间协作。 在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。**

德州仪器 (TI) 嵌入式处理器维基网站 ***德州仪器 (TI) 嵌入式处理器维基网站。*** 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.4 商标

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7.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、首字母缩略词和定义。

8 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC1200RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CC1200
CC1200RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CC1200

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

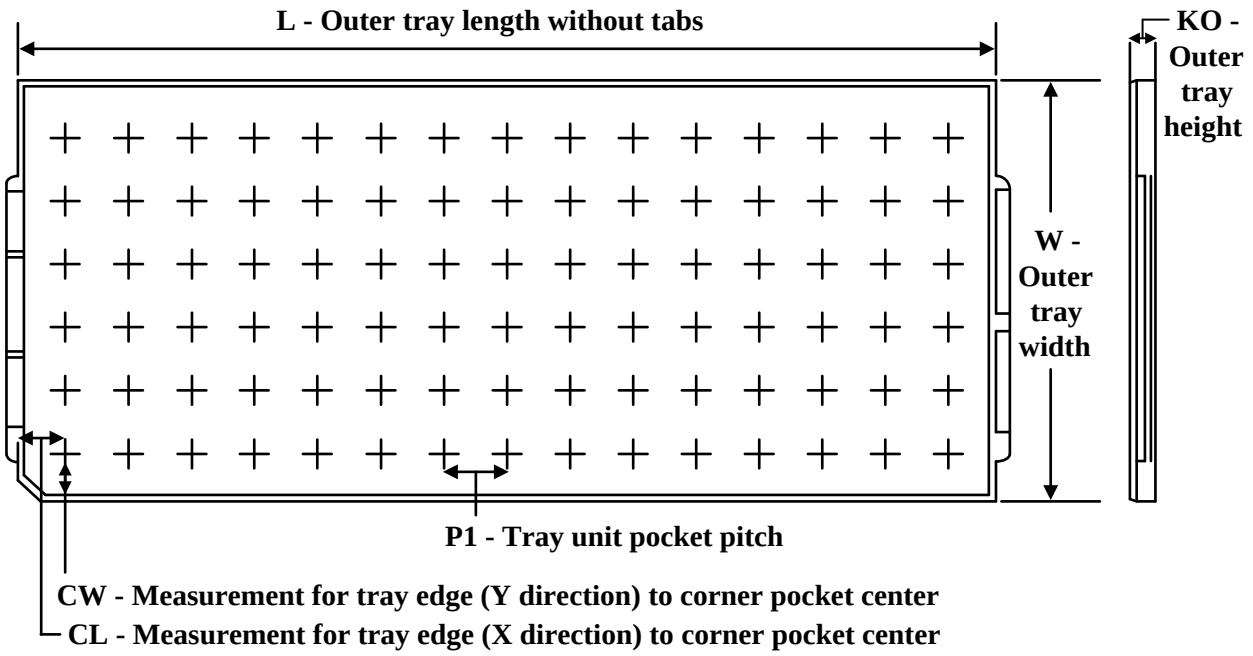
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC1200RHBR	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1200RHBT	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1200RHBT	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

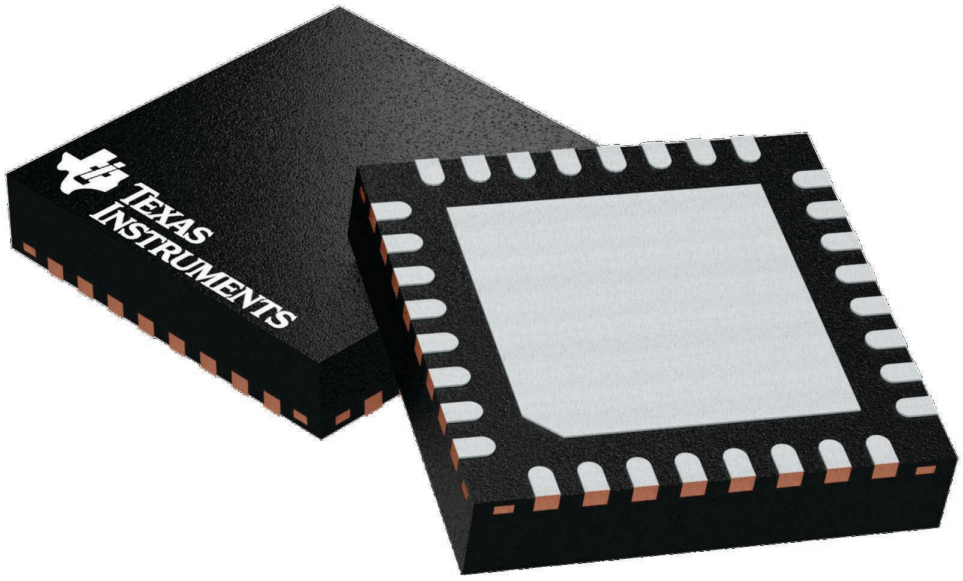
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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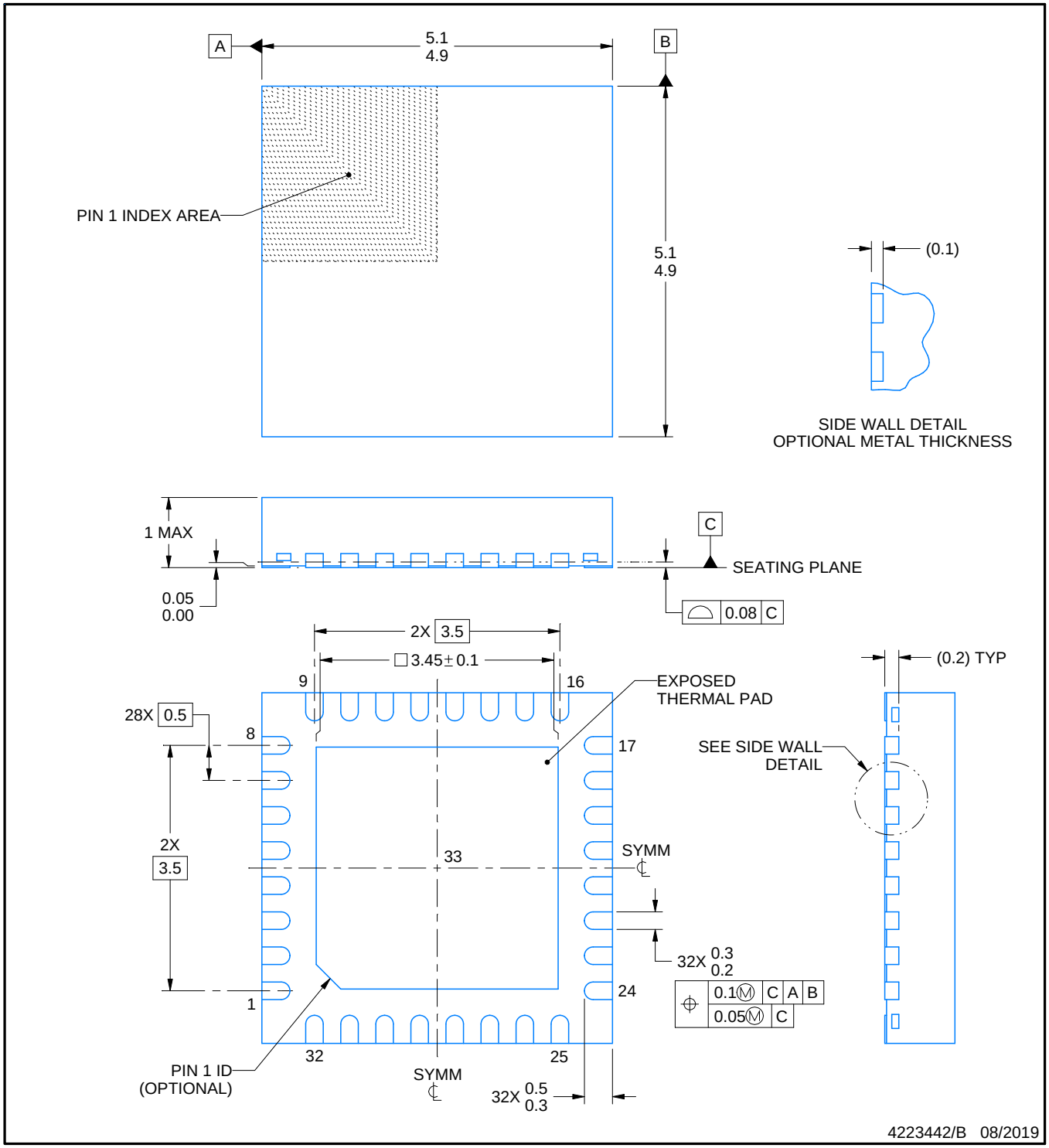
RHB0032E

PACKAGE OUTLINE

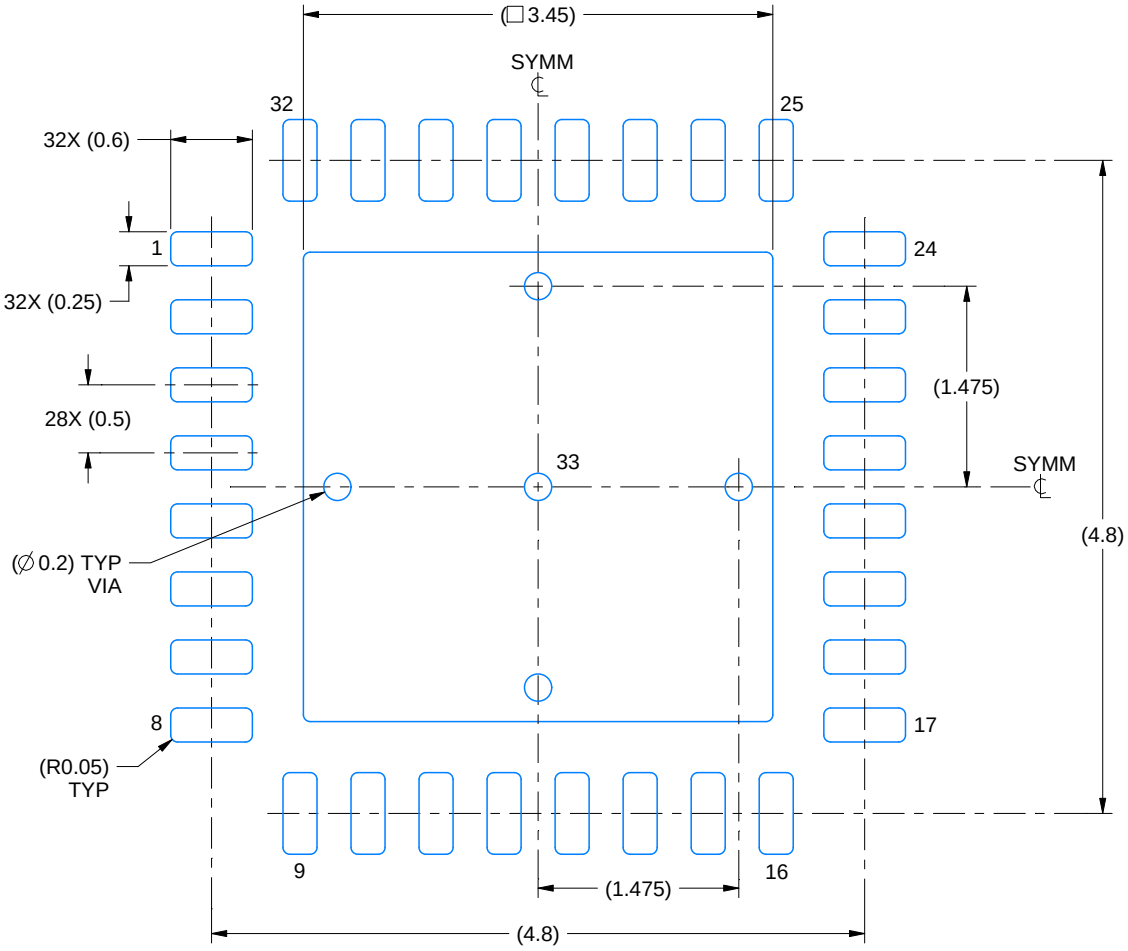
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

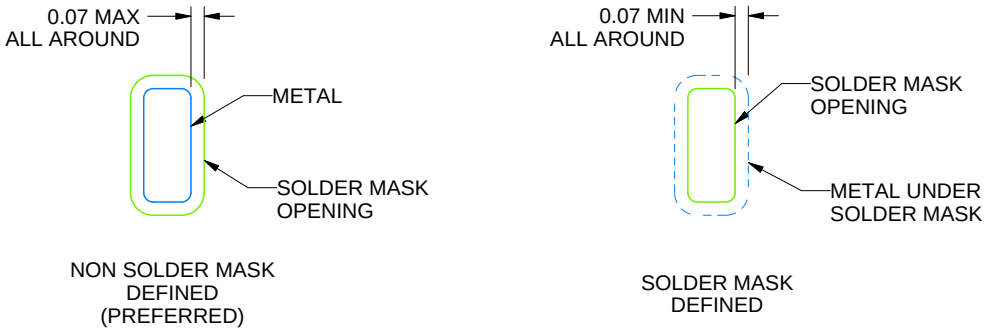


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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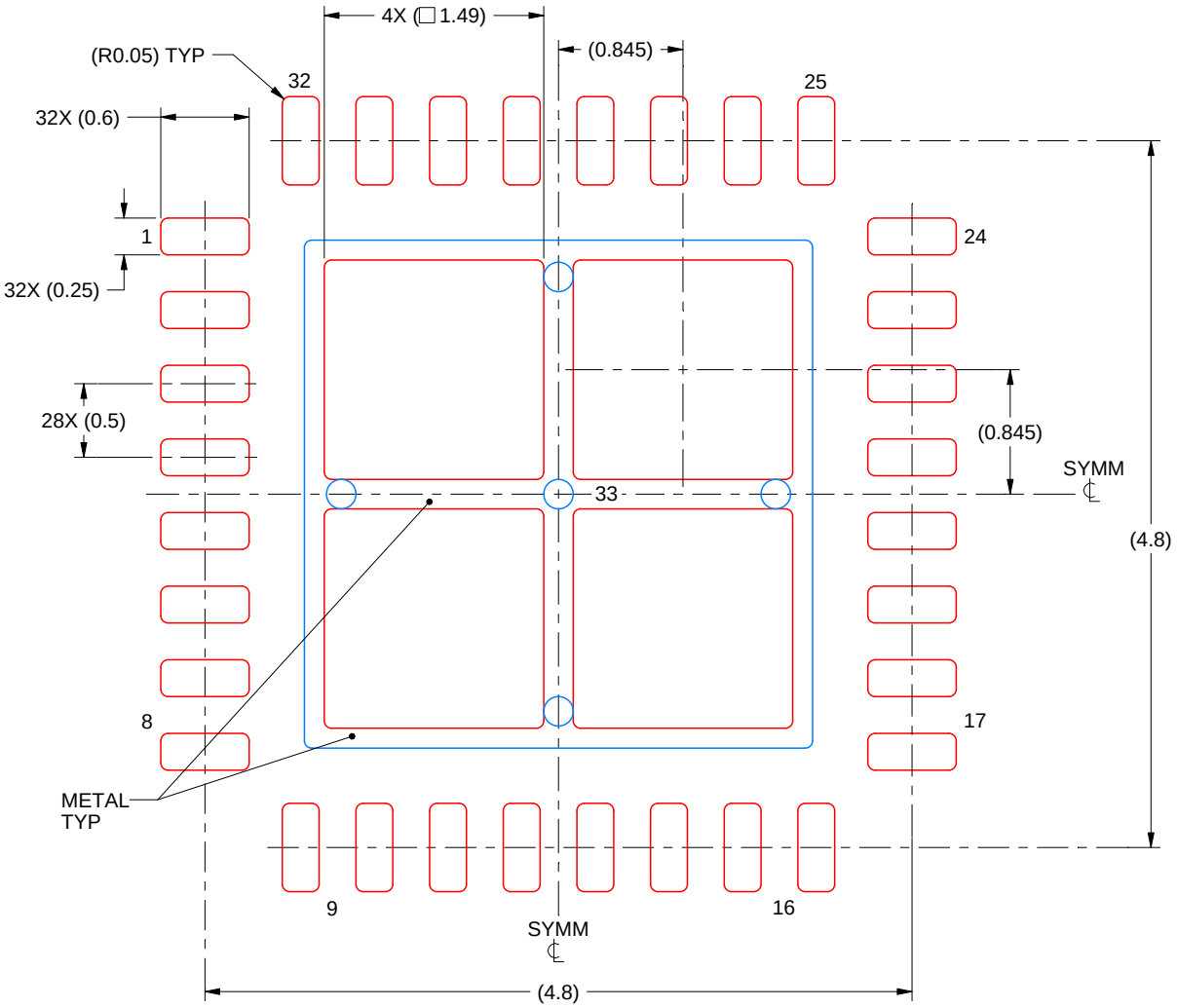
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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