BQ34Z100-R2 采用 Impedance Track™ 技术的宽量程电量监测计

1 特性

- 支持锂离子、磷酸铁锂、PbA、镍氢和镍镉化学物质
- 对电压为 3V 至 16.7 KV 的电池使用已获得专利的 Impedance Track™ 技术估算容量
  - 老化补偿
  - 自放电补偿
- 支持的电池容量高达 7000Ah，并且提供标准配置选项
- 支持的充电和放电电流高达 8160 A，并且提供标准配置选项
- 外部负温度系数 (NTC) 热敏电阻支持
- 支持与主机系统的两线制 I^{2}C 和 HDQ 单线制通信接口
- SHA-1/HMAC 认证
- 一个或者四个 LED 直接显示控制
- 五个 LED 和通过端口扩展器的更多显示
- 节能模式（典型电池组运行范围条件）
  - 正常工作：< 145µA 平均电流
  - 睡眠：< 84µA 平均电流
  - 全睡眠：< 30µA 平均电流
- 封装：14 引脚 TSSOP

2 应用

- 轻型电动车辆
- 医疗仪器
- 移动无线电
- 电动工具
- 不间断电源 (UPS)

3 说明

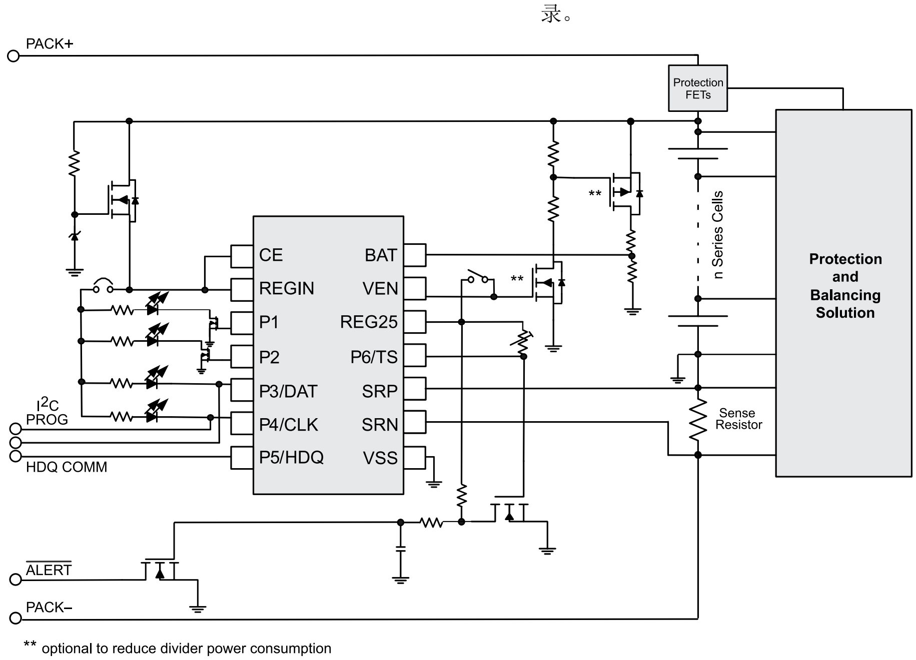
BQ34Z100-R2 器件是适用于锂离子、铅酸、镍氢和镍镉电池的 Impedance Track™ 电量监测计，并且独立于电池串联配置工作。通过外部电压转换电路可轻松支持 3V 至 16.7KV 的电池，此电路可通过自动控制来降低系统功耗。

BQ34Z100-R2 器件提供多个接口选项，其中包括一个 I^{2}C 外设接口、一个 HDQ 外设接口、一个或四个直接 LED 接口以及一个 ALERT 输出引脚。此外，BQ34Z100-R2 还支持外部端口扩展器，连接四个以上的 LED。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
BQ34Z100-R2	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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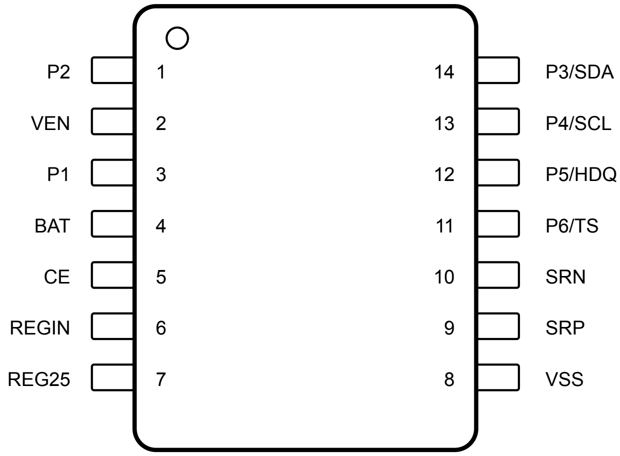
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions



Not to scale

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
P2	1	O	LED 2 or Not Used (connect to VSS)
VEN	2	O	Active High Voltage Translation Enable. This signal is optionally used to switch the input voltage divider on/off to reduce the power consumption (typ 45 µA) of the divider network. If not used, then this pin can be left floating or tied to VSS.
P1	3	O	LED 1 or Not Used (connect to VSS). This pin is also used to drive an LED for single-LED mode. Use a small signal N-FET (Q1) in series with the LED as shown on 图 8-4.
BAT	4	I	Translated Battery Voltage Input
CE	5	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low.
REGIN	6	P	Internal integrated LDO input. Decouple with a 0.1-µF ceramic capacitor to VSS.
REG25	7	P	2.5-V output voltage of the internal integrated LDO. Decouple with 1-µF ceramic capacitor to VSS.
VSS	8	P	Device ground
SRP	9	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is nearest the BAT – connection.
SRN	10	I	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is nearest the PACK – connection.
P6/TS	11	I	Pack thermistor voltage sense (use a 103AT-type thermistor)
P5/HDQ	12	I/O	Open-drain HDQ Serial communication line (target). If not used, then this pin can be left floating or tied to VSS.
P4/SCL	13	I	Target I^2C serial communication clock input. Use with a 10-kΩ pullup resistor (typical). This pin is also used for LED 4 in the four-LED mode. If not used, then this pin can be left floating or tied to VSS.
P3/SDA	14	I/O	Open-drain target I^2C serial communication data line. Use with a 10-kΩ pullup resistor (typical). This pin is also used for LED 3 in the four-LED mode. If not used, then this pin can be left floating or tied to VSS.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{REGIN}	Regulator Input Range	–0.3	5.5	V
V_{CC}	Supply Voltage Range	–0.3	2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, HDQ, VEN)	–0.3	5.5	V
V_{BAT}	Bat Input pin	–0.3	5.5	V
V_I	Input Voltage range to all other pins (P1, P2, SRP, SRN)	–0.3	VCC + 0.3	V
ESD	Human-body model (HBM), BAT pin		1.5	kV
	Human-body model (HBM), all other pins		2	kV
T_A	Operating free-air temperature range	–40	85	°C
T_F	Functional temperature range	–40	100	°C
T_{STG}	Storage temperature range	–65	150	°C
	Lead temperature (soldering, 10 s)	–40	100	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = –40°C to 85°C; Typical Values at T_A = 25°C C_{LDO25} = 1.0 µF, and V_{REGIN} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{REGIN}	Supply Voltage	No operating restrictions	2.7		4.5	V
		No FLASH writes	2.45		2.7	V
C_{REGIN}	External input capacitor for internal LDO between REGIN and VSS	Nominal capacitor values specified. Recommend a 10% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between VCC and VSS		0.47	1		µF
I_{CC}	NORMAL operating-mode current	Gas Gauge in NORMAL mode, I_{LOAD} > ***Sleep Current***		145		µA
I_{SLP}	SLEEP operating-mode current	Gas Gauge in SLEEP mode, I_{LOAD} < ***Sleep Current***		84		µA
I_{SLP+}	FULLSLEEP operating-mode current	Gas Gauge in FULL SLEEP mode, I_{LOAD} < ***Sleep Current***		30		µA
V_{OL}	Output voltage, low (SCL, SDA, HDQ, VEN)	I_{OL} = 3 mA			0.4	V
$V_{OH(PP)}$	Output voltage, high	I_{OH} = –1 mA	V_{CC} – 0.5			V
$V_{OH(OD)}$	Output voltage, high (SDA, SCL, HDQ, VEN)	External pull-up resistor connected to V_{CC}	V_{CC} – 0.5			V
V_{IL}	Input voltage, low		–0.3		0.6	V

6.3 Recommended Operating Conditions (continued)

T_A = −40°C to 85°C; Typical Values at T_A = 25°C C_{LDO25} = 1.0 μF, and V_{REGIN} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{IH(OD)}$	Input voltage, high (SDA, SCL, HDQ)		1.2		6	V
V_{A1}	Input voltage range (TS)		VSS − 0.05		1	V
V_{A2}	Input voltage range (BAT)		VSS − 0.125		5	V
V_{A3}	Input voltage range (SRP, SRN)		VSS − 0.125		0.125	V
I_{LKG}	Input leakage current (I/O pins)				0.3	μA
t_{PUCD}	Power-up communication delay			250		ms

6.4 Thermal Information

THERMAL METRIC[1]		BQ34Z100-R2 TSSOP (PW) 14 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	103.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	31.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*, SPRA953.

6.5 Electrical Characteristics: Power-On Reset

T_A = −40°C to 85°C; Typical Values at TA = 25°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at REG25		2.05	2.20	2.31	V
V_{HYS}	Power-on reset hysteresis		45	115	185	mV

6.6 Electrical Characteristics: LDO Regulator

T_A = 25°C, C_{LDO25} = 1.0 μF, V_{REGIN} = 3.6 V (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	2.7 V ≤ V_{REGIN} ≤ 4.5 V, I_{OUT} ≤ 16 mA	T_A = −40°C to 85°C	2.3	2.5	2.7	V
		2.45 V ≤ V_{REGIN} < 2.7 V (low battery), I_{OUT} ≤ 3 mA	T_A = −40°C to 85°C	2.3			V
I_{SHORT} [2]	Short Circuit Current Limit	V_{REG25} = 0 V	T_A = −40°C to 85°C			250	mA

(1) LDO output current, I_{OUT}, is the sum of internal and external load currents.
(2) Specified by design. Not production tested.

6.7 Electrical Characteristics: Internal Temperature Sensor Characteristics

T_A = −40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{TEMP}	Temperature sensor voltage gain			−2		mV/°C

6.8 Electrical Characteristics: Low-Frequency Oscillator

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(1) (2)	TA = 0°C to 60°C	–1.5%	0.25%	1.5%	
		TA = –20°C to 70°C	–2.5%	0.25%	2.5%	
		TA = –40°C to 85°C	–4%	0.25%	4%	
$t_{(LSXO)}$	Start-up time(3)			500		μs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

6.9 Electrical Characteristics: High-Frequency Oscillator

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency			8.389		MHz
$f_{(EIO)}$	Frequency error(1) (2)	T_A = 0°C to 60°C	–2%	0.38%	2%	
		T_A = –20°C to 70°C	–3%	0.38%	3%	
		T_A = –40°C to 85°C	–4.5%	0.38%	4.5%	
$t_{(SXO)}$	Start-up time(2)			2.5	5	ms

(1) The frequency error is measured from 2.097 MHz.
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

6.10 Electrical Characteristics: Integrating ADC (Coulomb Counter) Characteristics

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SR)}$	Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$	$V_{(SR)} = V_{(SRN)} - V_{(SRP)}$	–0.125		0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
I_{NL}	Integral nonlinearity error			±0.007%	±0.034%	FSR(2)
$Z_{IN(SR)}$	Effective input resistance(1)		2.5			MΩ
$I_{lkg(SR)}$	Input leakage current(1)				0.3	µA

(1) Specified by design. Not tested in production.
(2) Full-scale reference

6.11 Electrical Characteristics: ADC (Temperature and Cell Measurement) Characteristics

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(ADC)}$	Input voltage range		0.05		1	V
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
Z_{ADC1}	Effective input resistance (TS)(1)		8			MΩ
Z_{ADC2}	Effective input resistance (BAT)(1)	BQ34Z100-R2 not measuring cell voltage	8			MΩ
		BQ34Z100-R2 measuring cell voltage		100		KΩ

6.11 Electrical Characteristics: ADC (Temperature and Cell Measurement) Characteristics (continued)

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(ADC)}$	Input leakage current[(1)]				0.3	µA

(1) Specified by design. Not tested in production.

6.12 Electrical Characteristics: Data Flash Memory Characteristics

T_A = –40°C to 85°C, 2.4 V < REG25 < 2.6 V; Typical Values at T_A = 25°C and REG25 = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention[(1)]		10			Years
	Flash-programming write cycles[(1)]		20,000			Cycles
$t_{WORDPROG}$	Word programming time[(1)]				2	ms
I_{CCPROG}	Flash-write supply current[(1)]			5	10	mA

(1) Specified by design. Not tested in production.

6.13 Timing Requirements: HDQ Communication

T_A = –40°C to 85°C, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to BQ34Z100-R2		190			µs
$t_{(CYCD)}$	Cycle time, BQ34Z100-R2 to host		190	205	250	µs
$t_{(HW1)}$	Host sends 1 to BQ34Z100-R2		0.5		50	µs
$t_{(DW1)}$	BQ34Z100-R2 sends 1 to host		32		50	µs
$t_{(HW0)}$	Host sends 0 to BQ34Z100-R2		86		145	µs
$t_{(DW0)}$	BQ34Z100-R2 sends 0 to host		80		145	µs
$t_{(RSPS)}$	Response time, BQ34Z100-R2 to host		190		950	µs
$t_{(B)}$	Break time		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(RISE)}$	HDQ line rising time to logic 1 (1.2 V)				950	ns
$t_{(RST)}$	HDQ Reset		1.8		2.2	s

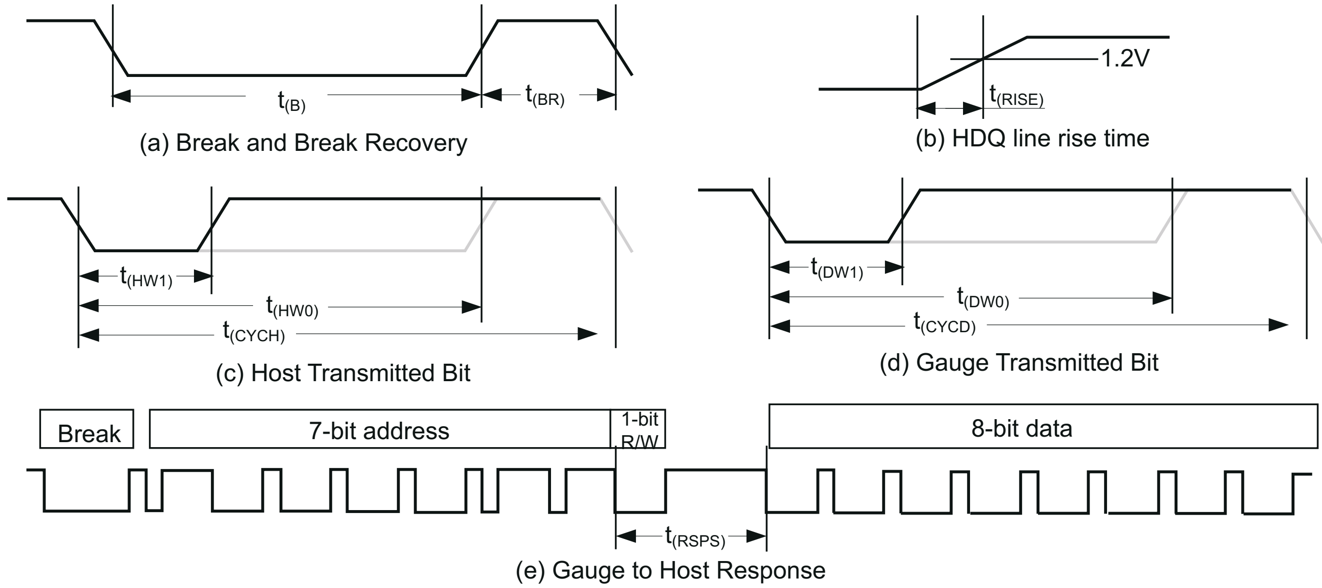


图 6-1. Timing Diagrams

6.14 Timing Requirements: I2C-Compatible Interface

T_A = –40°C to 85°C, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		600			ns
$t_{w(L)}$	SCL pulse width (low)		1.3			μs
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
t_{BUF}	Bus free time between stop and start		66			μs
f_{SCL}	Clock frequency				400	kHz

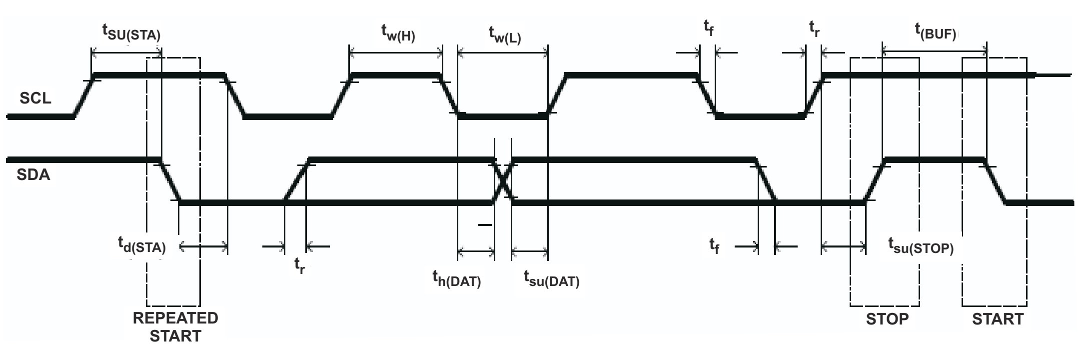


图 6-2. I2C-Compatible Interface Timing Diagrams

6.15 Typical Characteristics

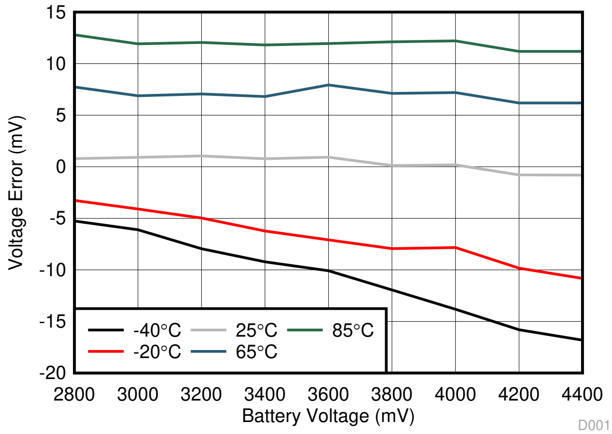


图 6-3. $V_{(Err)}$ Across VIN (0 mA)

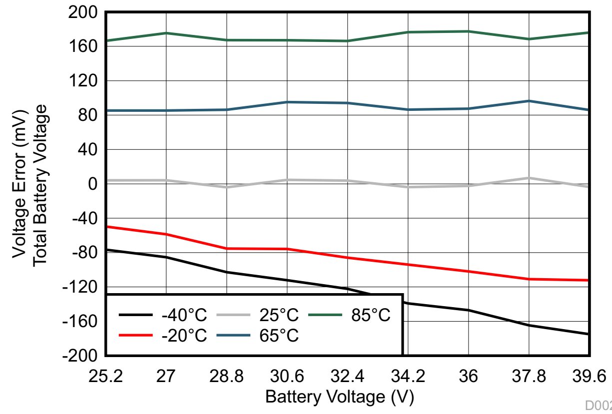


图 6-4. $V_{(Err)}$ Across VIN (0 mA) 9 s

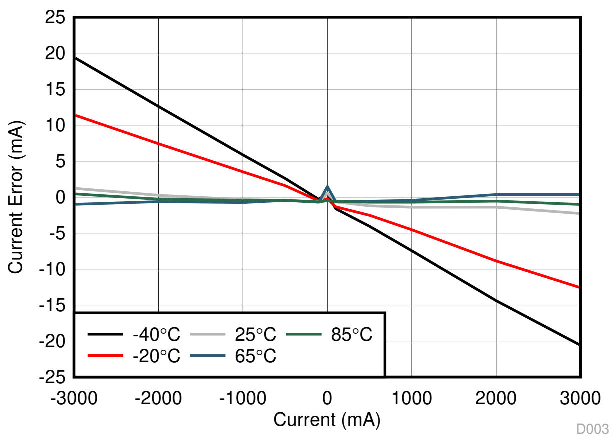


图 6-5. $I_{(Err)}$

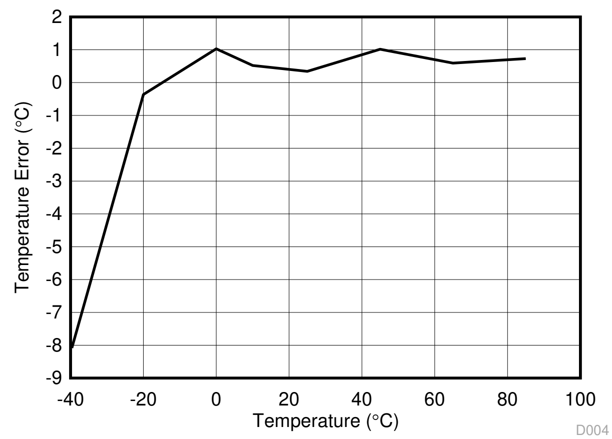
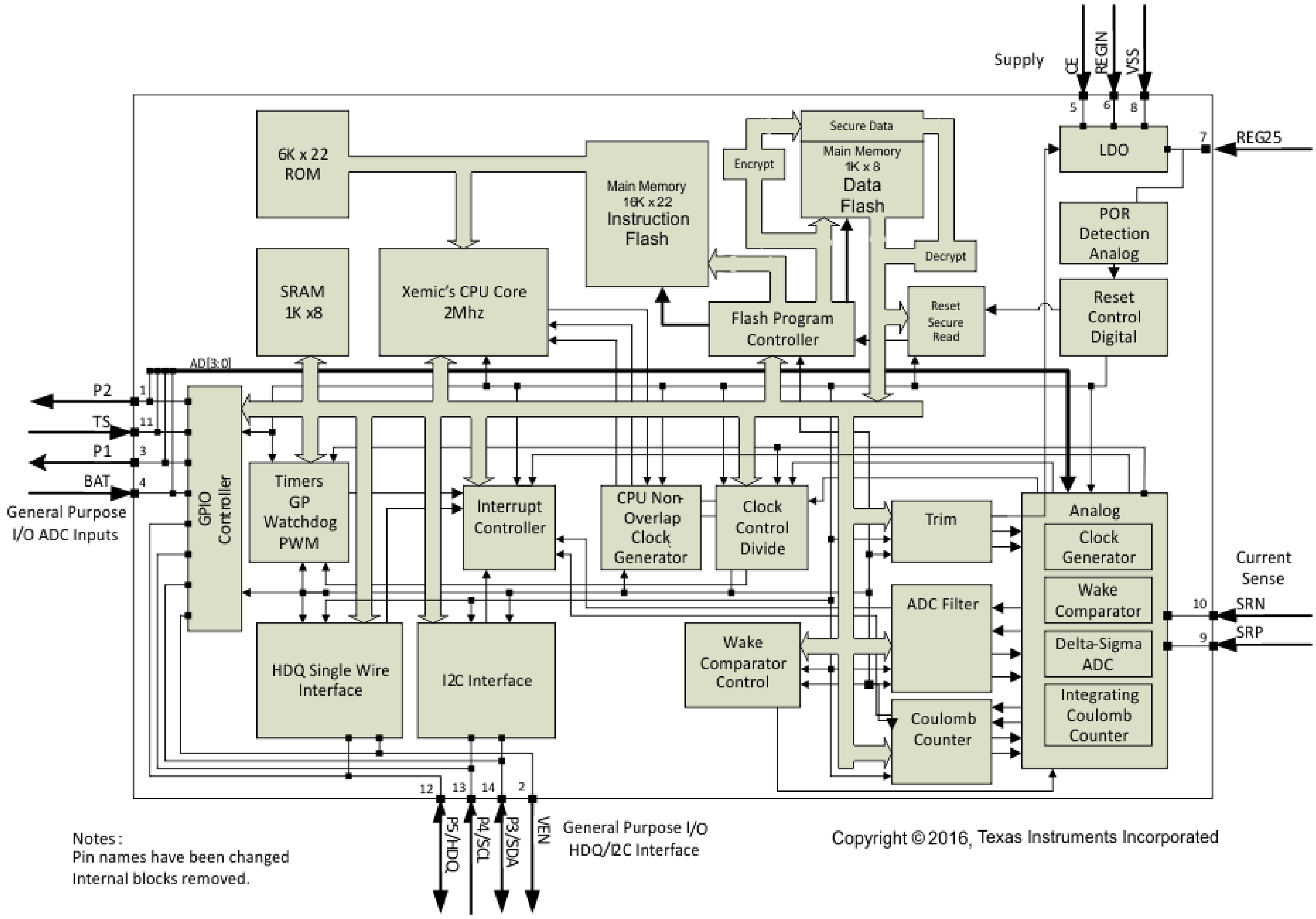


图 6-6. $T_{(Err)}$

7 Functional Block Diagram



8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

8.1 Application Information

The BQ34Z100-R2 is a flexible gas gauge device with many options. The major configuration choices comprise the battery chemistry, digital interface, and display.

8.2 Typical Applications

图 8-1 is a simplified diagram of the main features of the BQ34Z100-R2. Specific implementations detailing the main configuration options are shown later in this section.

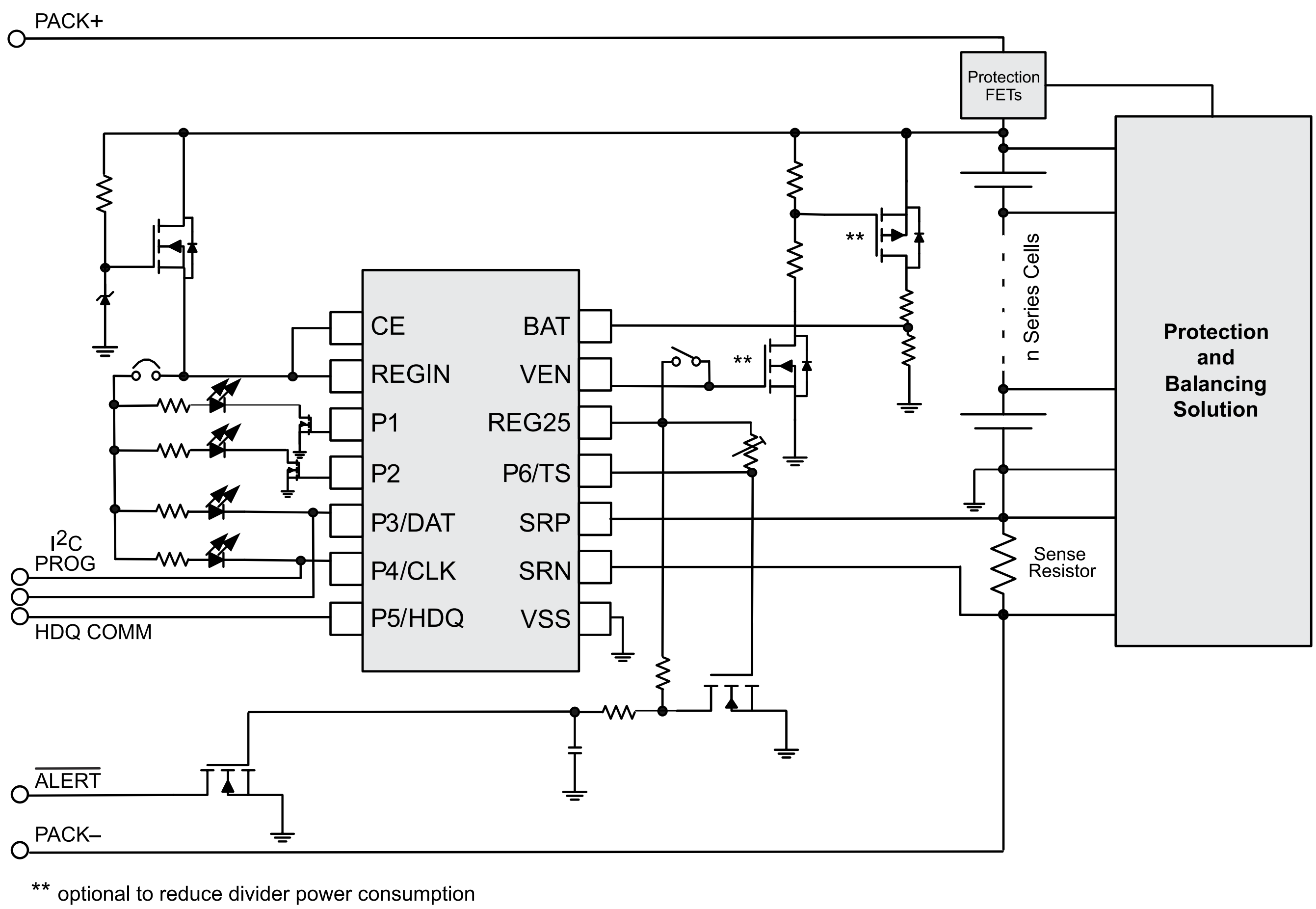


图 8-1. BQ34Z100-R2 Simplified Implementation

The BQ34Z100-R2 can be used to provide a single Li-ion cell gas gauge with a 5-bar LED display.

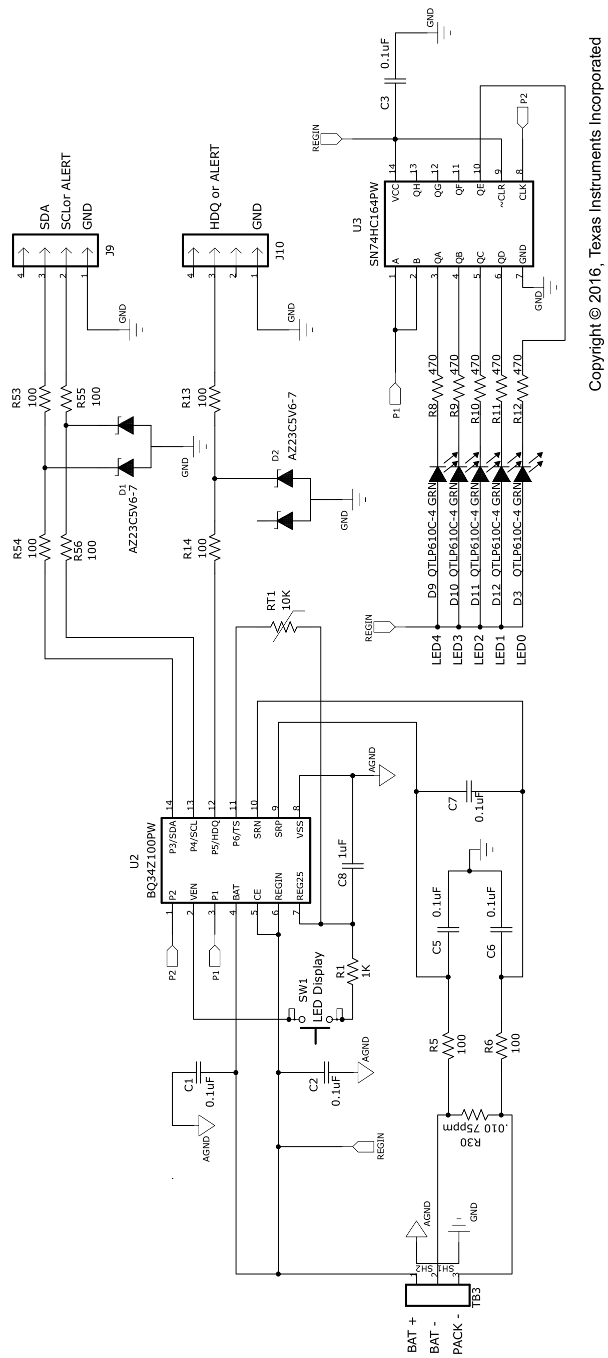


图 8-2. 1-Cell Li-ion and 5-LED Display

The BQ34Z100-R2 can also be used to provide a gas gauge for a multi-cell Li-ion battery with a 5-bar LED display.

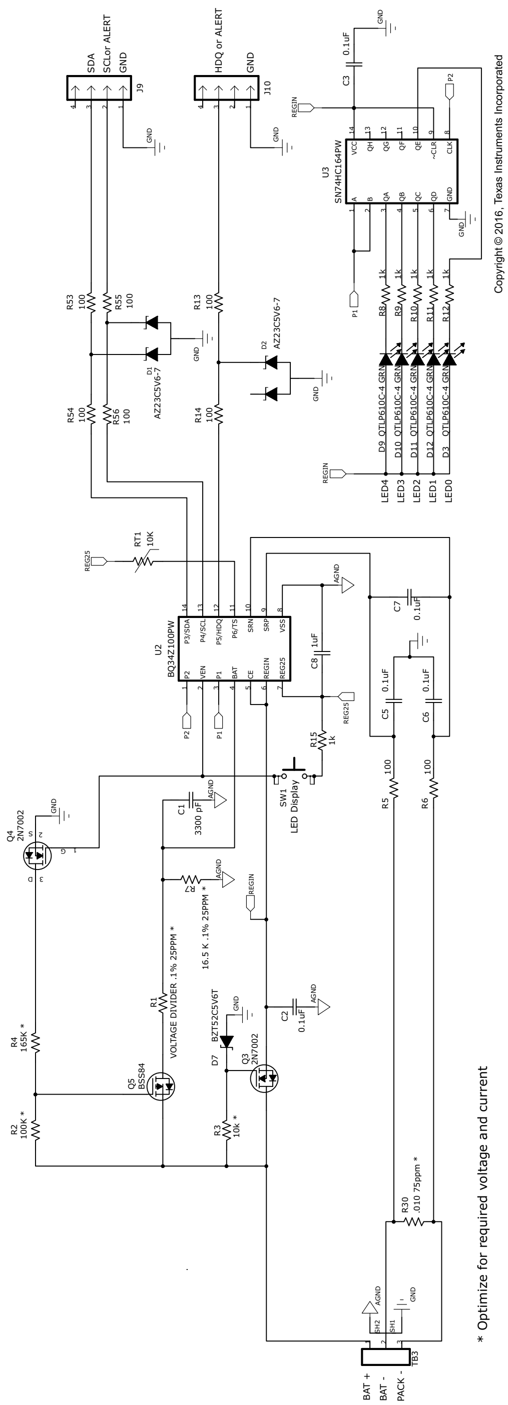


图 8-3. Multi-Cell and 5-LED Display

图 8-4 shows the BQ34Z100-R2 full features enabled.

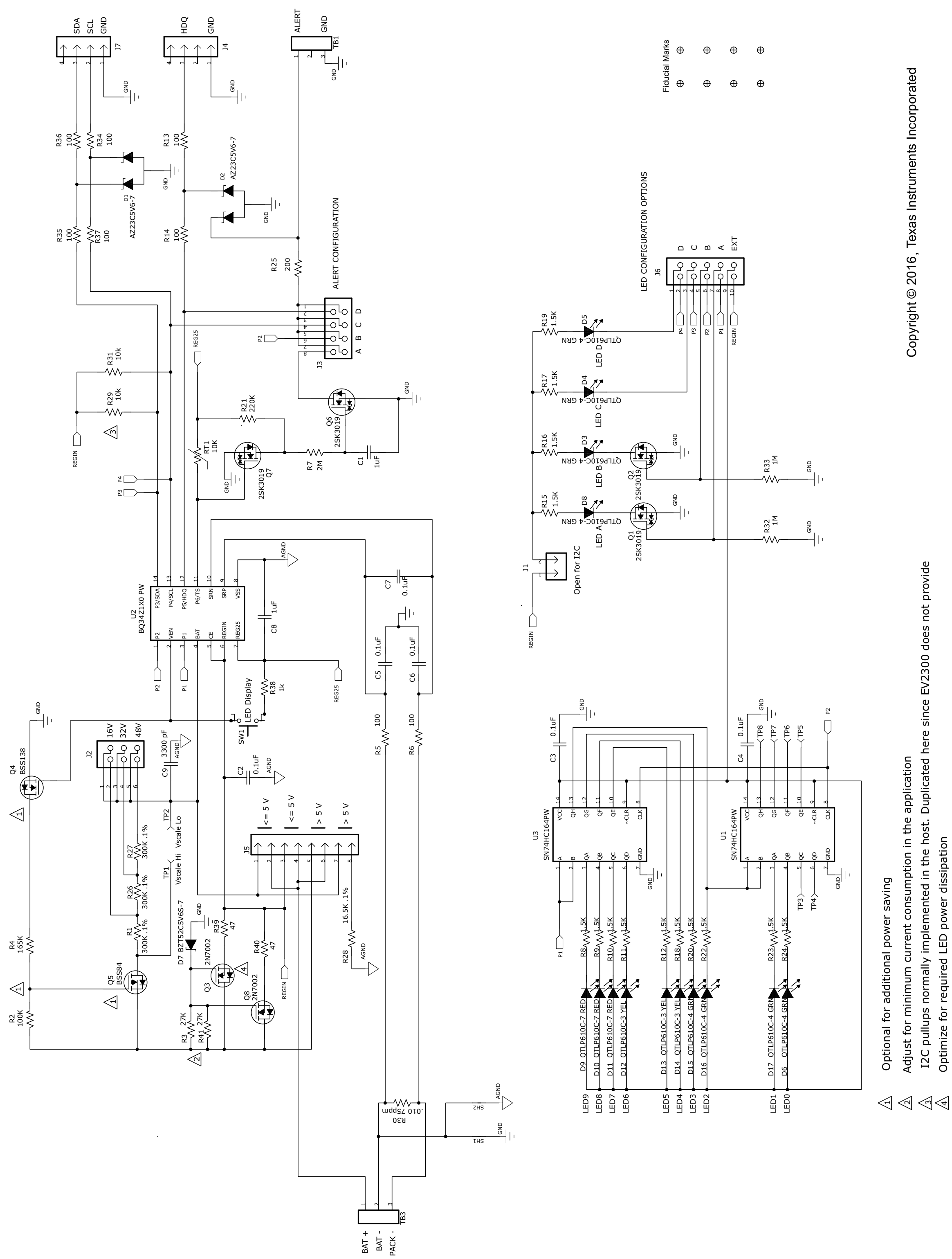


图 8-4. Full-Featured Evaluation Module EVM

8.2.1 Design Requirements

For additional design guidelines, refer to the *BQ34Z100 EVM Wide Range Impedance Track Enabled Battery Fuel Gauge User's Guide* (SLUU904).

8.2.2 Detailed Design Procedure

8.2.2.1 Step-by-Step Design Procedure

8.2.2.1.1 STEP 1: Review and Modify the Data Flash Configuration Data.

While many of the default parameters in the data flash are suitable for most applications, the following should first be reviewed and modified to match the intended application.

- ***Design Capacity***: Enter the value in mAh divided by *CurrScale()* for the battery, even from the “design energy” point of view.
- ***Design Energy***: Enter the value in cWh divided by *EnergyScale()* .
- ***Cell Charge Voltage Tx-Ty***: Enter the desired cell charge voltage for each JEITA temperature range.

8.2.2.1.2 STEP 2: Review and Modify the Data Flash Configuration Registers.

- ***LED_Comm Configuration***: See in the *BQ34Z100-R2 Technical Reference Manual* to aid in selection of an LED mode. Note that the pin used for the optional Alert signal is dependent upon the LED mode selected.
- ***Alert Configuration***: See the *BQ34Z100-R2 Technical Reference Manual* to aid in selection of which faults trigger the $\overline{\text{ALERT}}$ pin.
- ***Number of Series Cells***
- ***Pack Configuration***: Ensure that the VOLSEL bit is set for multicell applications and cleared for single-cell applications.

8.2.2.1.3 STEP 3: Design and Configure the Voltage Divider.

If the battery contains more than 1-s cells, a voltage divider network is required. Design the divider network, based on the formula below. The voltage division required is from the highest expected battery voltage, down to approximately 900 mV. For example, using a lower leg resistor of 16.5 KΩ where the highest expected voltage is 32000 mV:

Rseries = 16.5 KΩ (32000 mV – 900 mV)/900 mV = 570.2 KΩ

Based on price and availability, a 600-K resistor or pair of 300-K resistors could be used in the top leg along with a 16.5-K resistor in the bottom leg.

Set the ***Voltage Divider*** in the Data Flash Calibration section of the Evaluation Software to 32000 mV with *VoltScale()* =1.

Use the Evaluation Software to calibrate to the applied nominal voltage; for example, 24000 mV. After calibration, a slightly different value appears in the ***Voltage Divider*** parameter, which can be used as a default value for the project. For the applications with voltage higher than 65535 mV, please refer to the *BQ34Z100-R2 Technical Reference Manual*.

Following the successful voltage calibration, calculate and apply the value to ***Flash Update OK Cell Volt*** as: ***Flash Update OK Cell Volt*** = 2800 mV × ***Number Of Series Cells*** × 5000 / ***Voltage Divider*** */VoltScale()* .

8.2.2.1.4 STEP 4: Determine the Sense Resistor Value.

To ensure accurate current measurement, the input voltage generated across the current sense resistor should not exceed +/ – 125 mV. For applications with a very high dynamic range, it is allowable to extend this range to absolute maximum of +/ – 300 mV for overload conditions where a protector device will be taking independent protective action. In such an overloaded state, current reporting and gauging accuracy will not function correctly.

The value of the current sense resistor should be entered into both ***CC Gain*** and ***CC Delta*** parameters in the Data Flash Calibration section of the Evaluation Software.

8.2.2.1.5 STEP 5: Review and Modify the Data Flash Gas Gauging Configuration, Data, and State.

- ***Load Select***: See *Current Model Used When Load Mode = 0* and *Constant-Power Model Used When Load Mode* = 1 in the *BQ34Z100-R2 Technical Reference Manual*.
- ***Load Mode***: See *Current Model Used When Load Mode = 0* and *Constant-Power Model Used When Load Mode* = in the *BQ34Z100-R2 Technical Reference Manual*.

- ***Cell Terminate Voltage***: This is the theoretical voltage where the system begins to fail. It is defined as a zero state-of-charge. Generally, a more conservative level is used to have some reserve capacity. Note the value is for a single cell only.
- ***Quit Current***: Generally, this should be set to a value slightly above the expected idle current of the system.
- ***Qmax Cell 0***: Start with the C-rate value of your battery.

8.2.2.1.6 STEP 6: Determine and Program the Chemical ID.

Use the BQChem feature in the Evaluation Software to select and program the chemical ID matching your cell. If no match is found, use the procedure defined in TI's (*Mathcad Chemistry Selection Tool* (SLUC138)).

8.2.2.1.7 STEP 7: Calibrate.

Follow the steps on the **Calibration** screen in the Evaluation Software. Achieving the best possible calibration is important before moving on to Step 8. For mass production, calibration is not required for single-cell applications. For multi-cell applications, only voltage calibration is required. Current and temperature may be calibrated to improve gauging accuracy if needed.

8.2.2.1.8 STEP 8: Run an Optimization Cycle.

Refer to the *Preparing Optimized Default Flash Constants for Specific Battery Types Application Report* (SLUA334B).

9 Power Supply Recommendations

Power supply requirements for the BQ34Z100-R2 are simplified due to the presence of the internal LDO voltage regulation. The REGIN pin accepts any voltage level between 2.7 V and 4.5 V, which is optimum for a single-cell Li-ion application. For higher battery voltage applications, a simple pre-regulator can be provided to power the bq34Z100-R2 and any optional LEDs. Decoupling the REGIN pin should be done with a 0.1-μF 10% ceramic X5R capacitor placed close to the device. While the pre-regulator circuit is not critical, special attention should be paid to its quiescent current and power dissipation. The input voltage should handle the maximum battery stack voltage. The output voltage can be centered within the 2.7-V to 4.5-V range as recommended for the REGIN pin.

For high stack count applications, a commercially available LDO is often the best quality solution, but comes with a cost tradeoff. To lower the BOM cost, the following approaches are recommended.

In 图 9-1, Q1 is used to drop the battery stack voltage to roughly 4 V to power the BQ34Z100-R2 REGIN pin and also to feed the anode of any LEDs used in the application. To avoid unwanted quiescent current consumption, R1 should be set as high as is practical. It is recommended to use a low-current Zener diode.

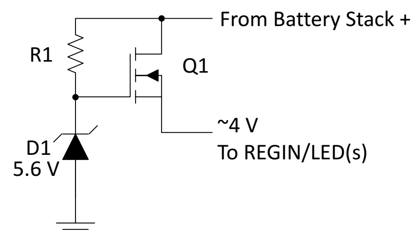


图 9-1. Q1 Dropping Battery Stack Voltage to 4 V

Alternatively, if the range of a high-voltage battery stack can be well defined, a simple source follower based on a resistive divider can be used to lower the BOM cost and the quiescent current. For example:

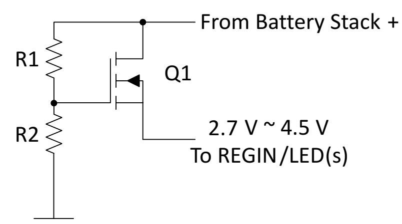


图 9-2. Source Follower on a Resistive Divider

Power dissipation of the linear pre-regulator may become an important design decision when multiple LEDs are employed in the application. For example, the BQ34Z100-R2 EVM uses a pair of FETs in parallel to inexpensively dissipate enough power for 10-LED evaluation.

10 Layout

10.1 Layout Guidelines

10.1.1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Some of the key areas of concern are described in the following sections, and can help to enable success.

10.1.2 Power Supply Decoupling Capacitor

Power supply decoupling from VCC to ground is important for optimal operation of the gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

10.1.3 Capacitors

Power supply decoupling for the gas gauges requires a pair of 0.1-µF ceramic capacitors for (BAT) and (VCC) pins. These should be placed reasonably close to the IC without using long traces back to VSS. The LDO voltage regulator, whether external or internal to the main IC, requires a 0.47-µF ceramic capacitor to be placed fairly close to the regulation output pin. This capacitor is for amplifier loop stabilization and as an energy well for the 2.5-V supply.

10.1.4 Communication Line Protection Components

The 5.6-V Zener diodes, used to protect the communication pins of the gas gauge from ESD, should be located as close as possible to the pack connector. The grounded end of these Zener diodes should be returned to the Pack(–) node rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

In some applications, it is sometimes necessary to cause transitions on the communication lines to trigger events that manage the gas gauge power modes. An example of one of these transitions is detecting a sustained low logic level on the communication lines to detect that a pack has been removed. Given that most of the gas gauges do not have internal pulldown networks, it is necessary to add a weak pulldown resistor to accomplish this when there's an absence of a strong pullup resistor on the system side. If the weak pulldown resistor is used, it may take less board space to use a small capacitor in parallel instead of the Zener diode to absorb any ESD transients that are received through communication lines.

10.2 Layout Example

10.2.1 Ground System

The gas gauge requires a low-current ground system separate from the high-current PACK(–) path. ESD ground is defined along the high-current path from the PACK(–) terminal to low-side protector FETs (if present) or the sense resistor. It is important that the low-current ground systems only connect to the BAT(–) path at the sense resistor Kelvin pick-off point. It is recommended to use an optional inner layer ground plane for the low-current ground system. In 图 10-1, the green is an example of using the low-current ground as a shield for the gas gauge circuit. Notice how it is kept separate from the high-current ground, which is shown in red. The high-current path is joined with the low-current path only at one point, shown with the small blue connection between the two planes.

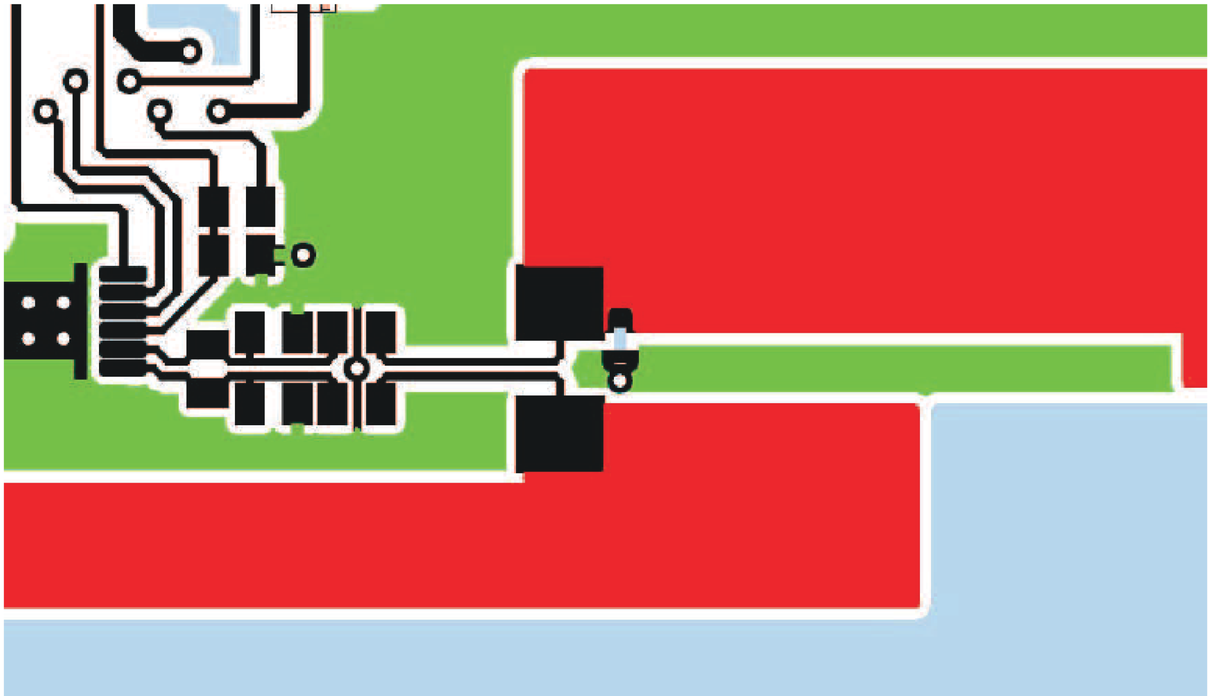


图 10-1. Differential Filter Component with Symmetrical Layout

10.2.2 Kelvin Connections

Kelvin voltage sensing is very important to accurately measure current and cell voltage. Notice how the differential connections at the sense resistor do not add any voltage drop across the copper etch that carries the high current path through the sense resistor. See 图 10-1 and 图 10-2.

10.2.3 Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for V_{CC}, additional benefit is possible by using this recommended pattern for the coulomb counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100-Ω resistors, as shown in 图 10-2.

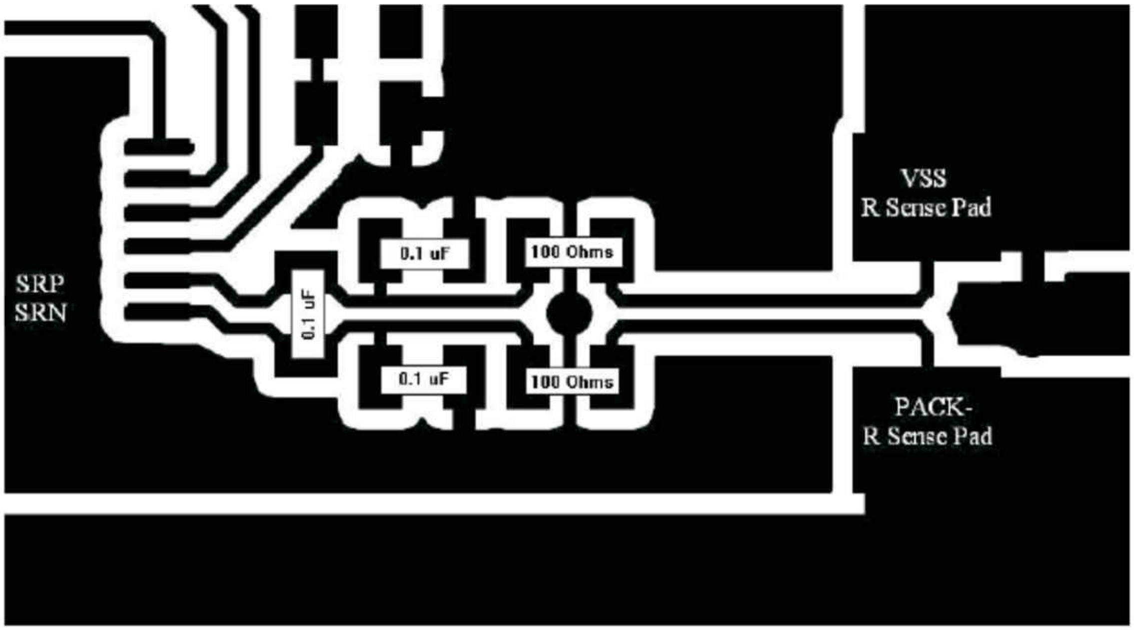


图 10-2. Differential Connection Between SRP and SRN Pins with Sense Resistor

10.2.4 ESD Spark Gap

Protect the communication lines from ESD with a spark gap at the connector. 图 10-3 shows the recommended pattern with its 0.2-mm spacing between the points.

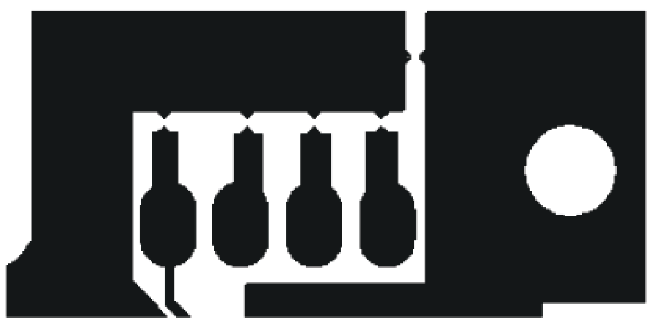


图 10-3. Recommended Spark-Gap Pattern Helps Protect Communication Lines from ESD

11 Device and Documentation Support

11.1 Documentation Support

For related documentation, see the following:

- *BQ34Z100-R2 Technical Reference Manual*
- *BQ34Z100-R2 High Cell Count and High Capacity Applications* application report

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ34Z100PWR-R2	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	34Z100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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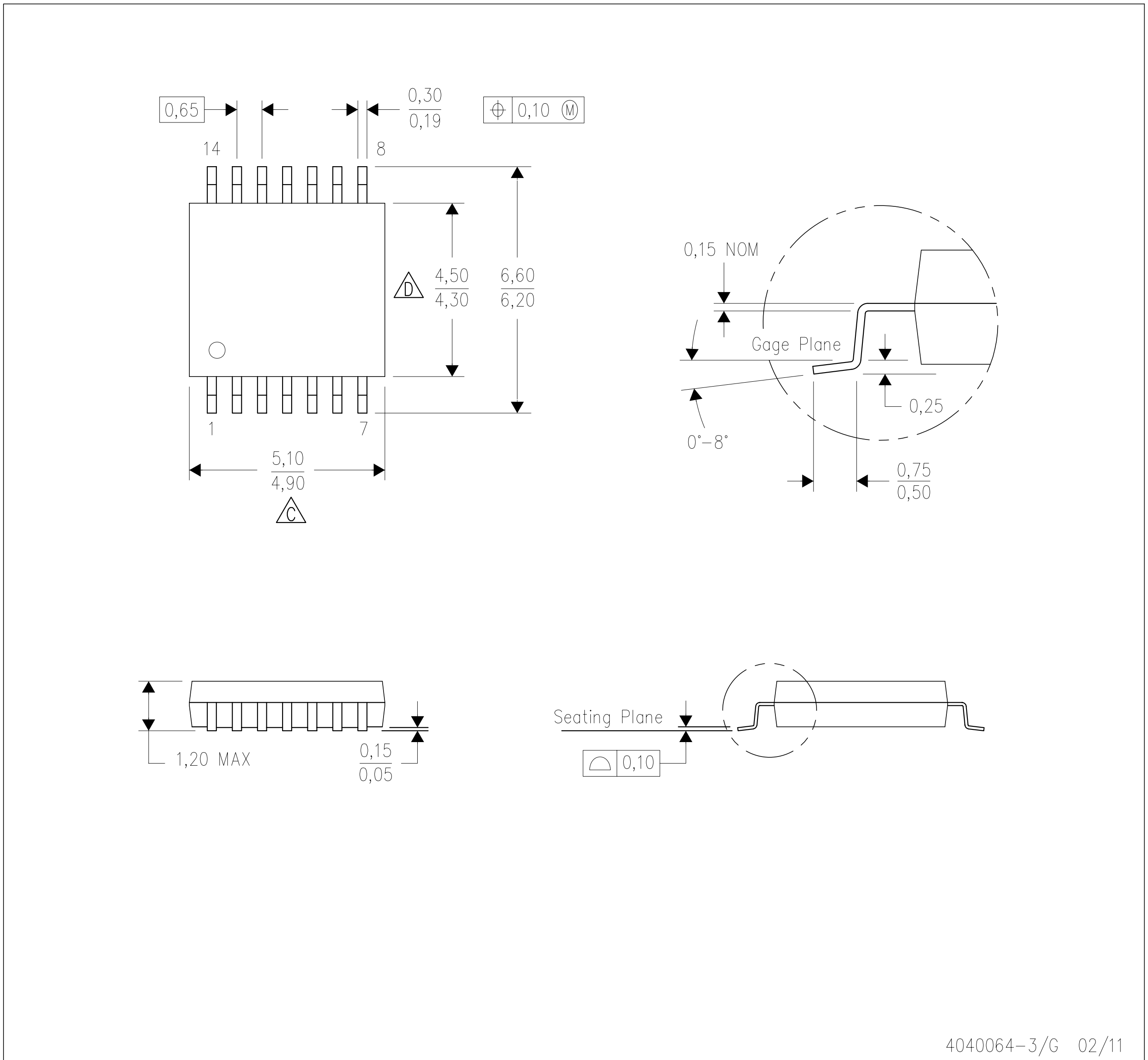
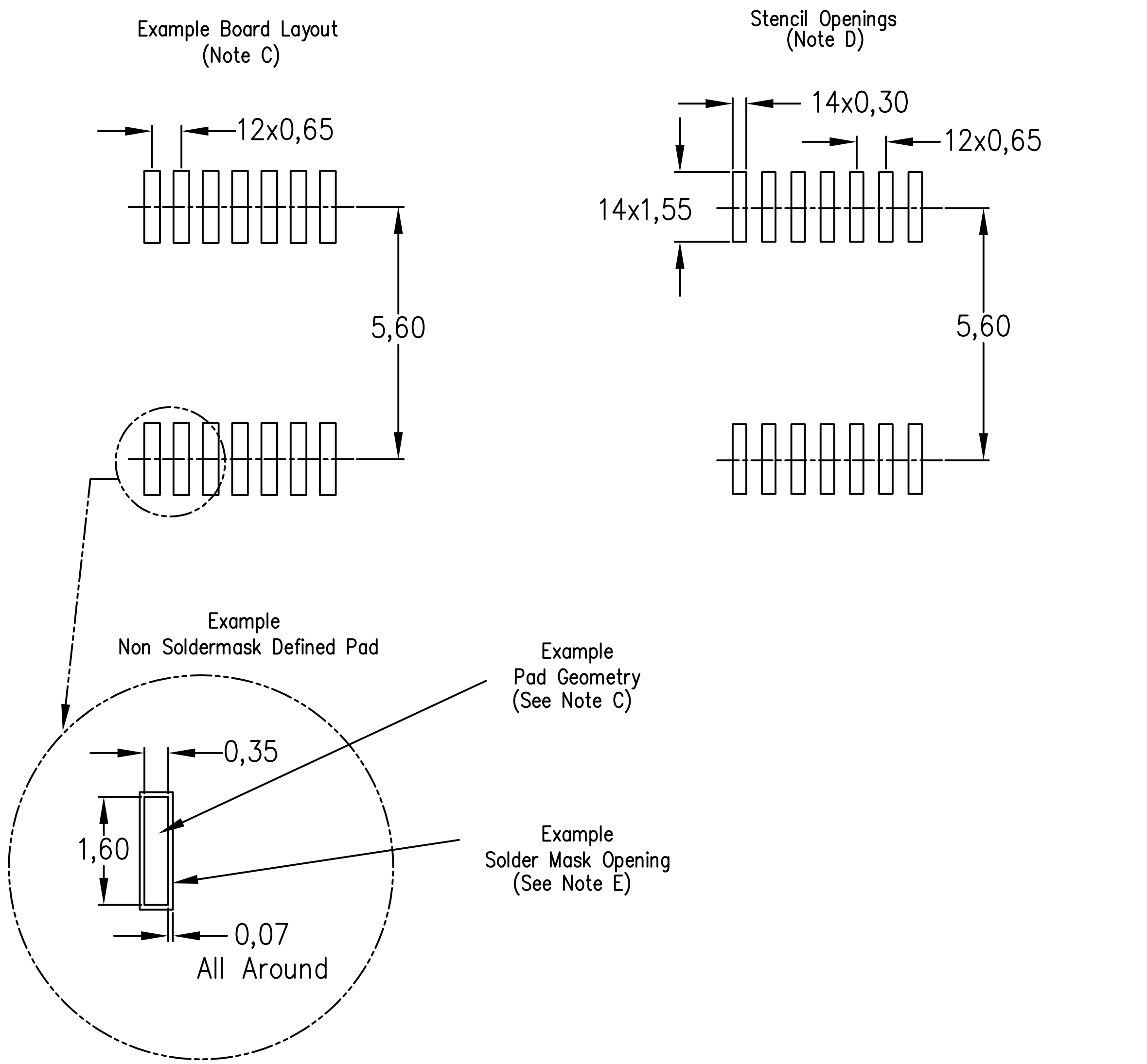
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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