ADC121S705 12-Bit, 500 kSPS to 1 MSPS, Differential Input, Micro Power A/D Converter

Check for Samples: ADC121S705

FEATURES

- **True Differential Inputs**
- **Ensured performance from 500 kSPS to 1 MSPS**
- **External Reference**
- **Wide Input Common-Mode Voltage Range**
- **SPI™/QSPI™/MICROWIRE/DSP Compatible Serial Interface**

APPLICATIONS

- **Automotive Navigation**
- **Portable Systems**
- **Medical Instruments**
- **Instrumentation and Control Systems**
- **Motor Control**
- **Direct Sensor Interface**

KEY SPECIFICATIONS

- **Conversion Rate: 500 kSPS to 1 MSPS**
- **INL: ± 0.95 LSB (Max)**
- **DNL: ±0.95 LSB (Max)**
- **Offset Error: ±3.0 LSB (Max)**
- **Gain Error: ±6.5 LSB (Max)**
- **SINAD: 69.5 db (Min)**
- **Power Consumption at V_A = 5V**
  - **Active, 1 MSPS: 11.5 mW (Typ)**
  - **Active, 500 kSPS: 9.0 mW (Typ)**
  - **Power-Down: 1.5 µW (Typ)**

DESCRIPTION

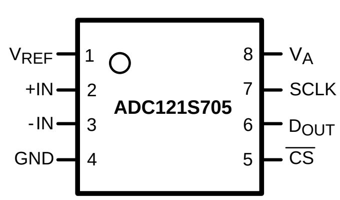
The ADC121S705 is a 12-bit, 500 kSPS to 1 MSPS sampling Analog-to-Digital (A/D) converter that features a fully differential, high impedance analog input and an external reference. The reference voltage can be varied from 1.0V to V_A, with a corresponding resolution between 244µV and V_A divided by 4096.

The output serial data is binary 2's complement and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. The differential input, low power consumption, and small size make the ADC121S705 ideal for direct connection to transducers in battery operated systems or remote data acquisition applications.

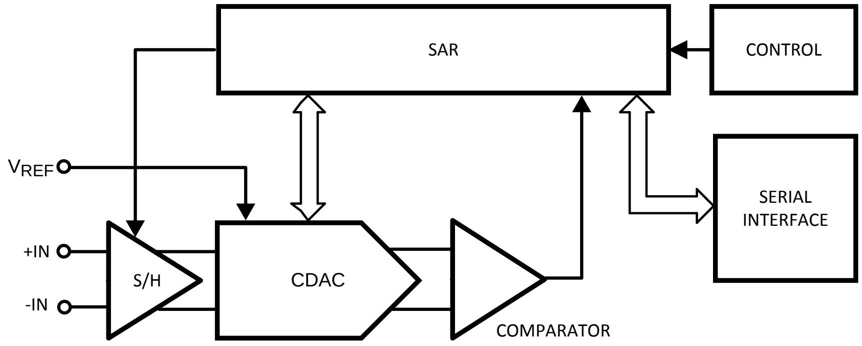
Operating from a single 5V supply, the supply current when operating at 1 MSPS is typically 2.3 mA. The supply current drops down to 0.3 µA typically when the ADC121S705 enters power-down mode. The ADC121S705 is available in the VSSOP-8 package. Operation is ensured over the industrial temperature range of −40°C to +105°C and clock rates of 8 MHz to 16 MHz.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Connection Diagram



Block Diagram



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	V_{REF}	Voltage Reference Input. A voltage reference between 1V and V_A must be applied to this input. V_{REF} must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF. A bulk capacitor value of 1.0 µF to 10 µF in parallel with the 0.1 µF is recommended for enhanced performance.
2	+IN	Non-Inverting Input. +IN is the positive analog input for the differential signal applied to the ADC121S705.
3	−IN	Inverting Input. −IN is the negative analog input for the differential signal applied to the ADC121S705.
4	GND	Ground. GND is the ground reference point for all signals applied to the ADC121S705.
5	$\overline{CS}$	Chip Select Bar. $\overline{CS}$ is active low. The ADC121S705 is in Normal Mode when $\overline{CS}$ is LOW and Power-Down Mode when $\overline{CS}$ is HIGH. A conversion begins on the fall of $\overline{CS}$.
6	D_{OUT}	Serial Data Output. The conversion result is provided on D_{OUT}. The serial data output word is comprised of 4 null bits and 12 data bits (MSB first). During a conversion, the data is outputted on the falling edges of SCLK and is valid on the rising edges.
7	SCLK	Serial Clock. SCLK is used to control data transfer and serves as the conversion clock.
8	V_A	Power Supply input. A voltage source between 4.5V and 5.5V must be applied to this input. V_A must be decoupled to GND with a ceramic capacitor value of 0.1 µF in parallel with a bulk capacitor value of 1.0 µF to 10 µF.

Absolute Maximum Ratings[1][2][3]

Analog Supply Voltage V_A		−0.3V to 6.5V
Voltage on Any Pin to GND		−0.3V to (V_A +0.3V)
Input Current at Any Pin[4]		±10 mA
Package Input Current[4]		±50 mA
Power Consumption at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	2500V
	Machine Model	250v
	Charge Device Model	750V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC121S705 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is a 220 pF capacitor discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings[1][2]

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage, V_A	+4.5V to +5.5V
Reference Voltage, V_{REF}	1.0V to V_A
Input Common-Mode Voltage, V_{CM}	See Figure 59
Digital Input Pins Voltage Range	0 to V_A
Clock Frequency	8 MHz to 16 MHz
Differential Analog Input Voltage	$-V_{REF}$ to $+V_{REF}$

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(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance[1][2]

Package	θ_{JA}
8-lead VSSOP	200°C / W

(1) Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
(2) Reflow temperature profiles are different for lead-free packages.

ADC121S705 Converter Electrical Characteristics(1)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 8 to 16 MHz, f_{IN} = 100 kHz, C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limits	Units(2)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non-Linearity			±0.6	**±0.95**	LSB (max)
DNL	Differential Non-Linearity			±0.4	**±0.95**	LSB (max)
OE	Offset Error			−0.4	**±3**	LSB (max)
FSE	Positive Full-Scale Error			+0.1	**±2**	LSB (max)
	Negative Full-Scale Error			-1.0	**±6**	LSB (max)
GE	Gain Error			+1.0	**±6.5**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz, −0.1 dBFS		72.2	**69.5**	dBc (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz, −0.1 dBFS		72.8	**71**	dBc (min)
THD	Total Harmonic Distortion	f_{IN} = 100 kHz, −0.1 dBFS		−81.6	**−72**	dBc (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz, −0.1 dBFS		83.9	**72**	dBc (min)
ENOB	Effective Number of Bits	f_{IN} = 100 kHz, −0.1 dBFS		11.7	**11.25**	bits (min)
FPBW	−3 dB Full Power Bandwidth	Output at 70.7%FS with FS Input	Differential Input	26		MHz
			Single-Ended Input	22		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Differential Input Range				**$-V_{REF}$**	V (min)
					$+V_{REF}$	V (max)
I_{DCL}	DC Leakage Current	$V_{IN} = V_{REF}$ or $V_{IN} = -V_{REF}$			**±1**	µA (max)
C_{INA}	Input Capacitance	In Track Mode		17		pF
		In Hold Mode		3		pF
CMRR	Common Mode Rejection Ratio	See Specification Definitions for the test condition		76		dB
V_{REF}	Reference Voltage Range				**1.0**	V (min)
					V_A	V (max)
I_{REF}	Reference Current	$\overline{CS}$ low, f_{SCLK} = 16 MHz, f_S = 1 MSPS, output = FF8h		55		µA
		$\overline{CS}$ low, f_{SCLK} = 8 MHz, f_S = 500 kSPS, output = FF8h		28		µA
		$\overline{CS}$ high, f_{SCLK} = 0		0.2		µA
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage			2.6	**3.6**	V (min)
V_{IL}	Input Low Voltage			2.5	**1.5**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_A			**±1**	µA (max)
C_{IND}	Input Capacitance			2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA		V_A − 0.12	**V_A − 0.2**	V (min)
		I_{SOURCE} = 1 mA		V_A − 0.16		V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		0.01	**0.4**	V (max)
		I_{SINK} = 1 mA		0.05		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current	Force 0V or V_A			**±1**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance	Force 0V or V_A		2	**4**	pF (max)
	Output Coding			Binary 2'S Complement		

(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.
(2) Tested limits are specified to AOQL (Average Outgoing Quality Level).

ADC121S705 Converter Electrical Characteristics[1] (continued)

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 8 to 16 MHz, f_{IN} = 100 kHz, C_L = 25 pF, unless otherwise noted. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units[2]
POWER SUPPLY CHARACTERISTICS					
V_A	Analog Supply Voltage			**4.5**	V (min)
				5.5	V (max)
I_{VA} (Normal)	Supply Current, Normal Mode (Operational)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz	2.3	**3**	mA (max)
		f_{SCLK} = 8 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz	1.8		mA
I_{VA} (PD)	Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz	56		µA (max)
		f_{SCLK} = 0 [3]	0.3	**2**	µA (max)
PWR (Normal)	Power Consumption, Normal Mode (Operational)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_A = 5.0V	11.5		mW
		f_{SCLK} = 8 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_A = 5.0V	9.0		mW
PWR (PD)	Power Consumption, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz, V_A = 5.0V	280		µW
		f_{SCLK} = 0, V_A = 5.0V	1.5		µW
PSRR	Power Supply Rejection Ratio	See the Specification Definitions for the test condition	−85		dB
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Maximum Clock Frequency		20	**16**	MHz (min)
f_{SCLK}	Minimum Clock Frequency		0.8	**8**	MHz (max)
f_S	Maximum Sample Rate[4]		1.25	**1**	MSPS (min)
t_{ACQ}	Track/Hold Acquisition Time			**2.5**	SCLK cycles (min)
				3.0	SCLK cycles (max)
t_{CONV}	Conversion Time			**13**	SCLK cycles
t_{AD}	Aperture Delay	See Specification Definitions	6		ns

(3) Data sheet min/max specification limits are specified by design, test, or statistical analysis.
(4) While the maximum sample rate is f_{SCLK}/16, the actual sample rate may be lower than this by having the $\overline{CS}$ rate slower than f_{SCLK}/16.

ADC121S705 Timing Specifications[1]

The following specifications apply for V_A = +4.5V to 5.5V, V_{REF} = 2.5V, f_{SCLK} = 8 MHz to 16 MHz, C_L = 25 pF, **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
t_{CSH}	$\overline{CS}$ Hold Time after an SCLK rising edge			**5**	ns (min)
t_{CSSU}	$\overline{CS}$ Setup Time prior to an SCLK rising edge			**5**	ns (min)
t_{DH}	D_{OUT} Hold time after an SCLK Falling edge		7	**2.5**	ns (min)
t_{DA}	D_{OUT} Access time after an SCLK Falling edge		18	**22**	ns (max)
t_{DIS}	D_{OUT} Disable Time after the rising edge of $\overline{CS}$[2]			**20**	ns (max)
t_{EN}	D_{OUT} Enable Time after the falling edge of $\overline{CS}$		8	**20**	ns (max)
t_{CH}	SCLK High Time			**25**	ns (min)
t_{CL}	SCLK Low Time			**25**	ns (min)
t_r	D_{OUT} Rise Time		7		ns
t_f	D_{OUT} Fall Time		7		ns

(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.
(2) t_{DIS} is the time for D_{OUT} to change 10% while being loaded by the Timing Test Circuit.

Timing Diagrams

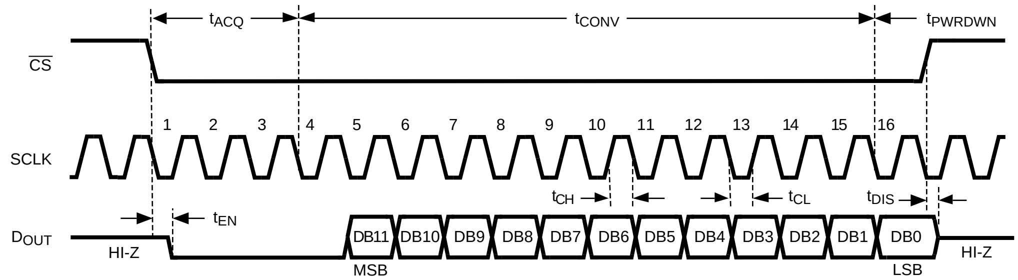


Figure 1. ADC121S705 Single Conversion Timing Diagram

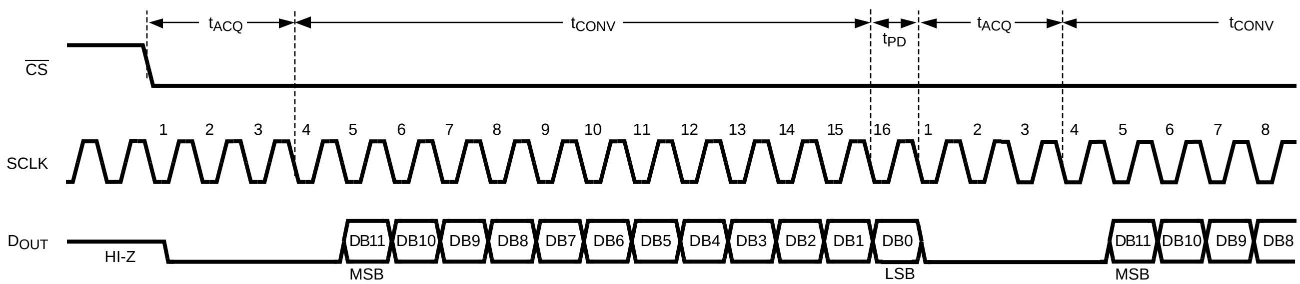


Figure 2. ADC121S705 Continuous Conversion Timing Diagram

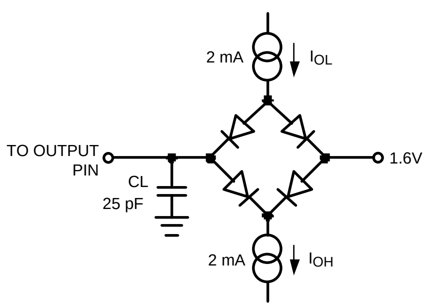


Figure 3. Timing Test Circuit

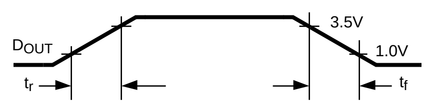


Figure 4. Rise and Fall Times

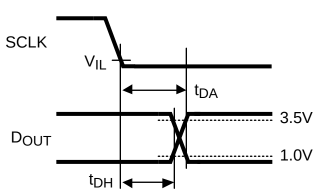


Figure 5. Hold and Access Times

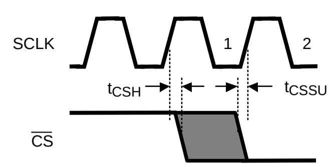


Figure 6. Valid $\overline{CS}$ Assertion Times

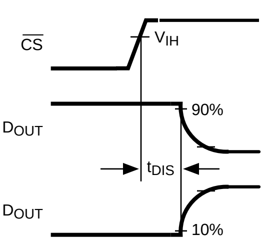


Figure 7. Voltage Waveform for t_{DIS}

Specification Definitions

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is acquired or held for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

$$CMRR = 20\ LOG\ (\Delta\ Common\ Input\ /\ \Delta\ Output\ Offset) \quad (1)$$

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between Positive Full-Scale Error and Negative Full-Scale Error and can be calculated as:

$$Gain\ Error = Positive\ Full\text{-}Scale\ Error - Negative\ Full\text{-}Scale\ Error \quad (2)$$

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC121S705 is ensured not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from negative full scale to the next code and $-V_{REF}$ + 0.5 LSB

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 000h to 001h and 1/2 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and V_{REF} minus 1.5 LSB.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC121S705, V_A is changed from 4.5V to 5.5V.

$$PSRR = 20\ LOG\ (\Delta Offset\ /\ \Delta V_A) \quad (3)$$

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}} \quad (4)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

Typical Performance Characteristics

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

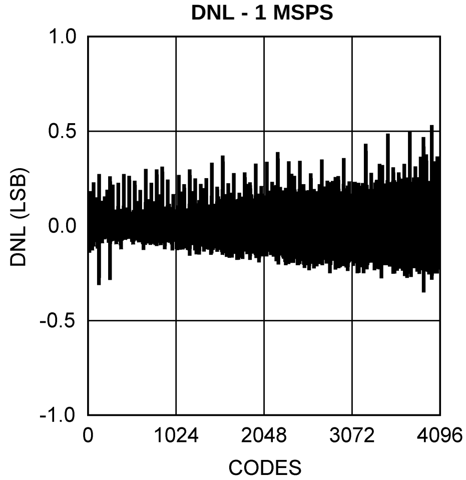


Figure 8.

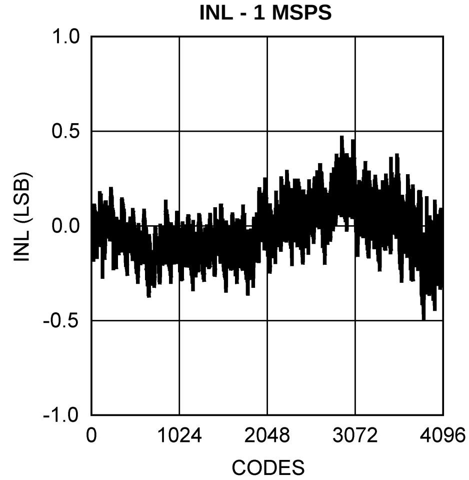


Figure 9.

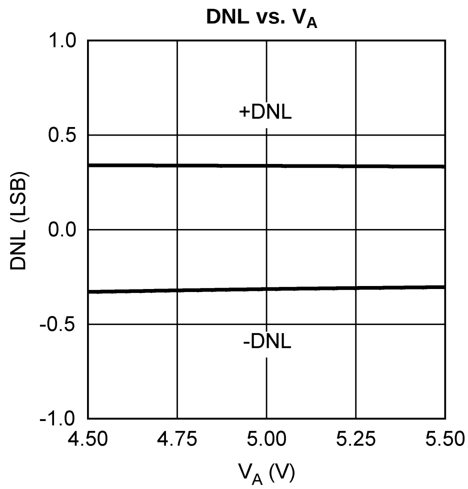


Figure 10.

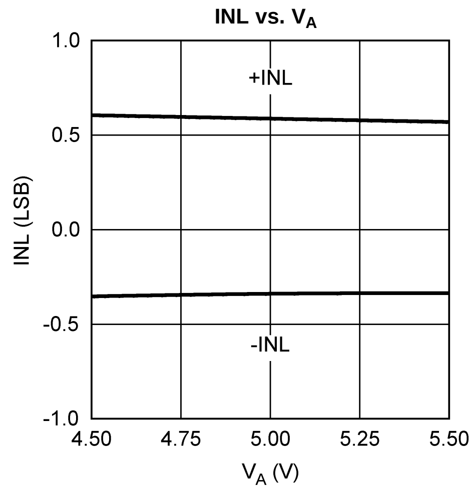


Figure 11.

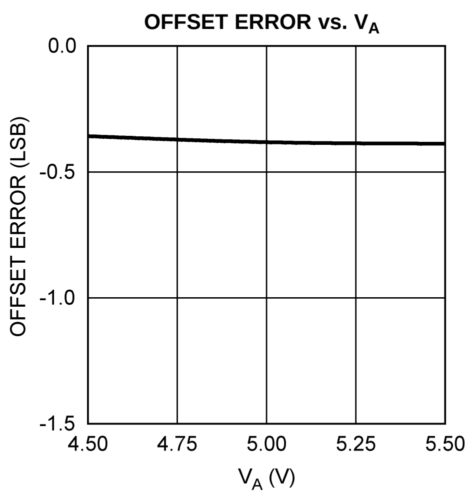


Figure 12.

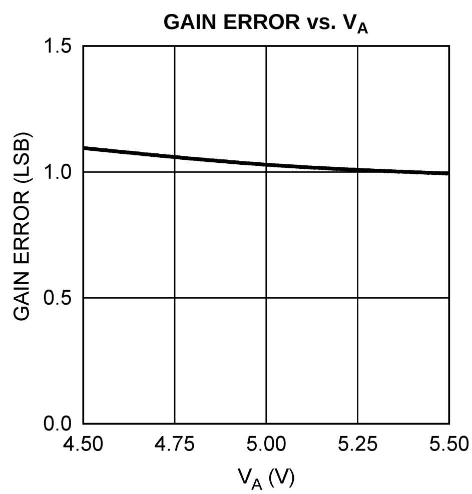


Figure 13.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

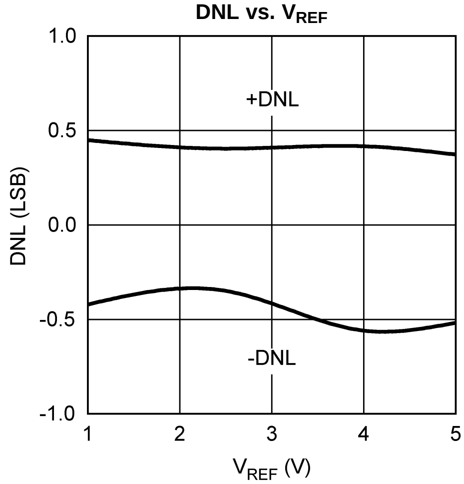


Figure 14.

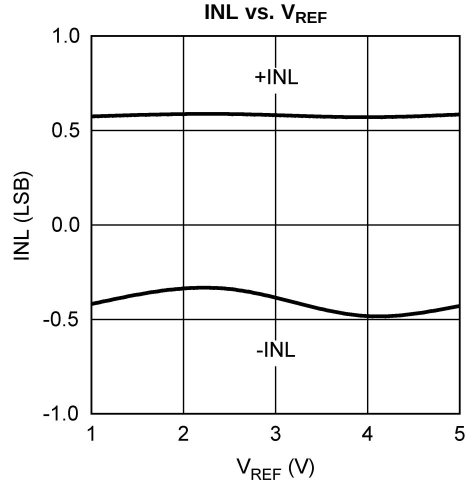


Figure 15.

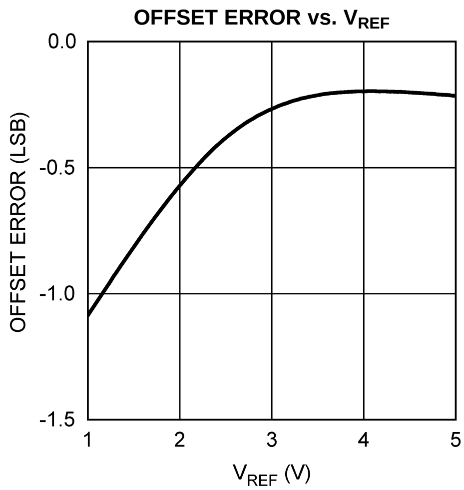


Figure 16.

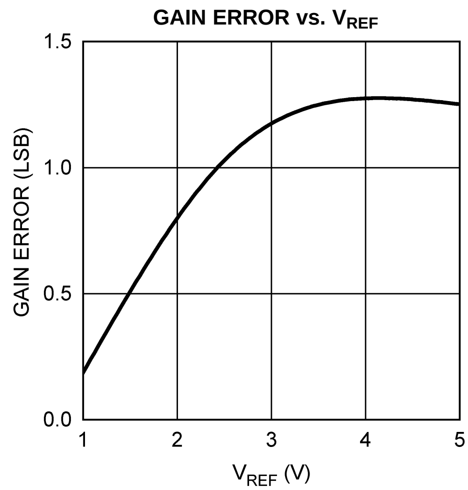


Figure 17.

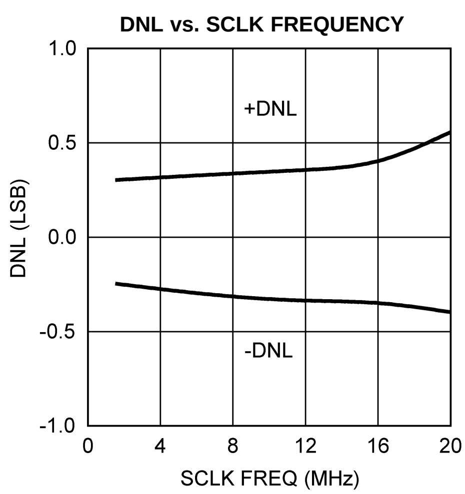


Figure 18.

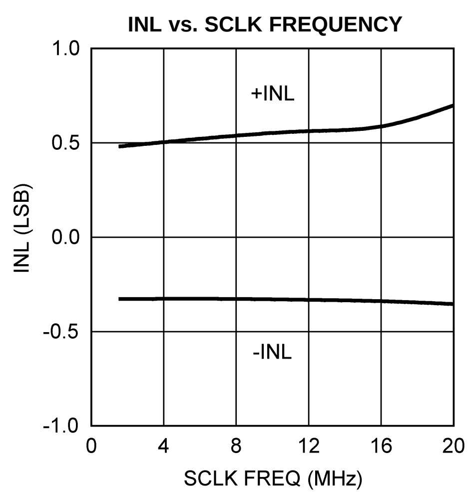


Figure 19.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

OFFSET ERROR vs. SCLK FREQUENCY

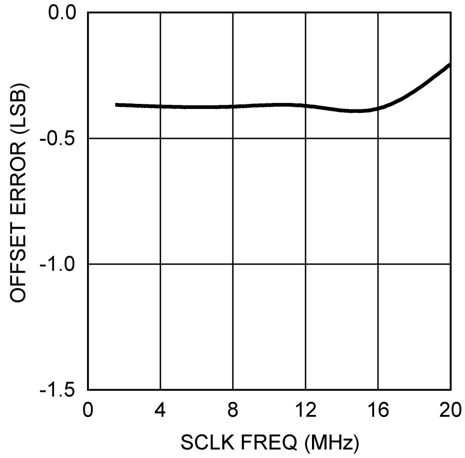


Figure 20.

GAIN ERROR vs. SCLK FREQUENCY

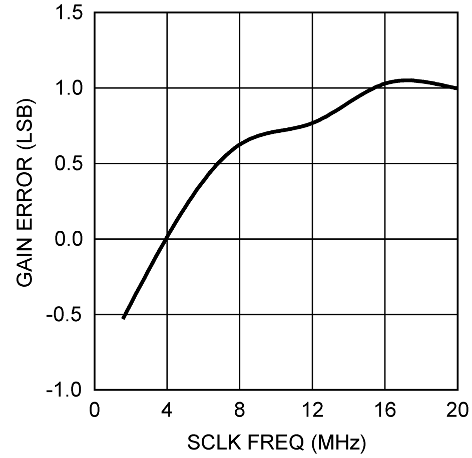


Figure 21.

DNL vs. SCLK DUTY CYCLE

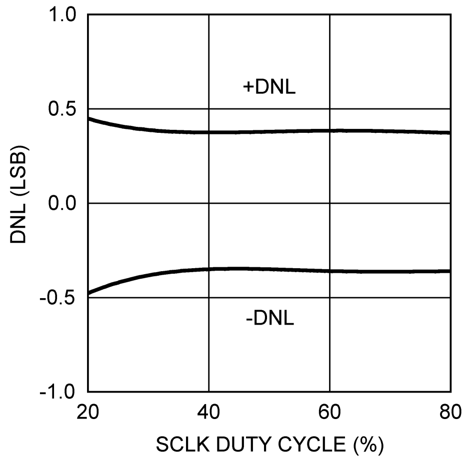


Figure 22.

INL vs. SCLK DUTY CYCLE

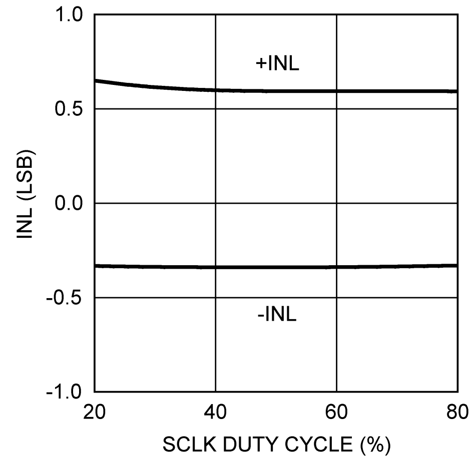


Figure 23.

OFFSET ERROR vs. SCLK DUTY CYCLE

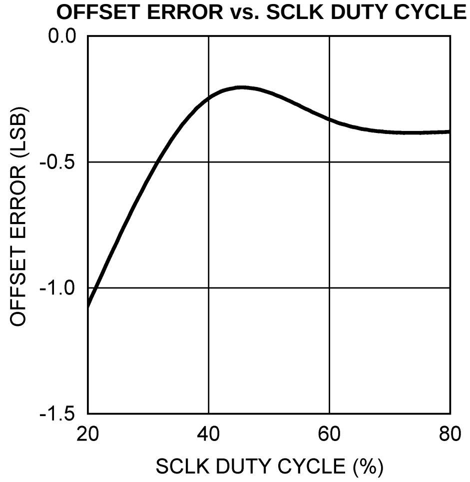


Figure 24.

GAIN ERROR vs. SCLK DUTY CYCLE

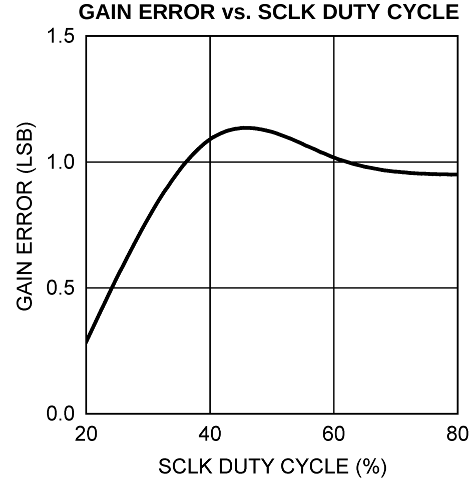
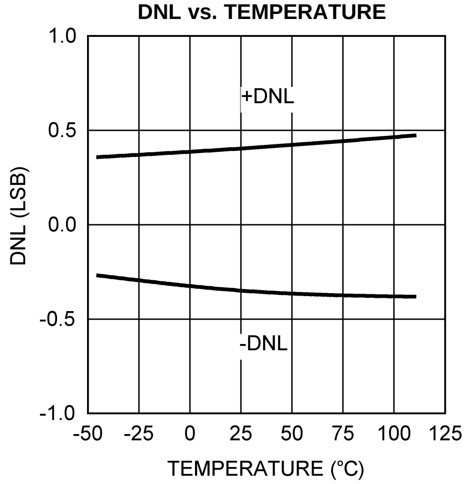


Figure 25.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.



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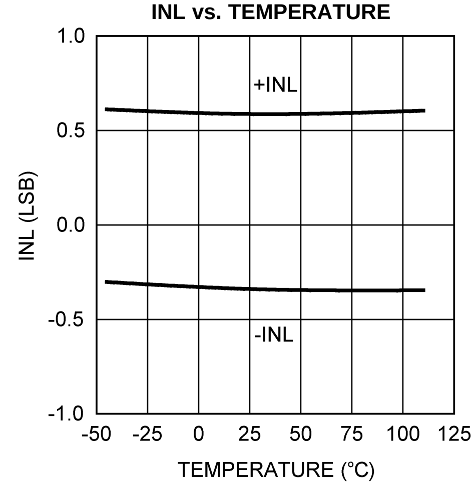

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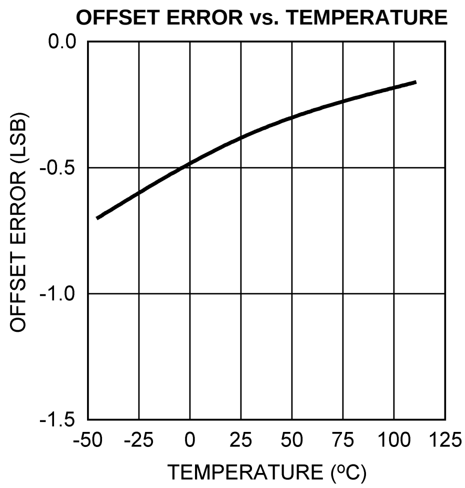

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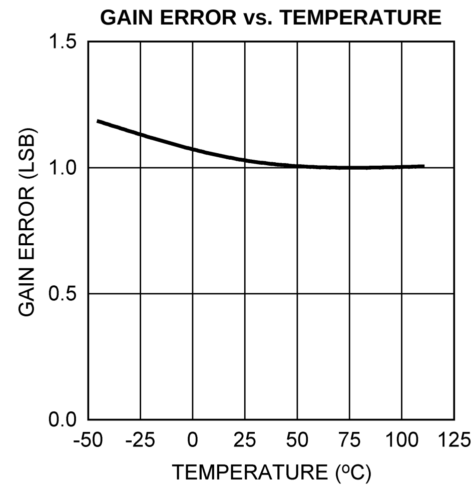

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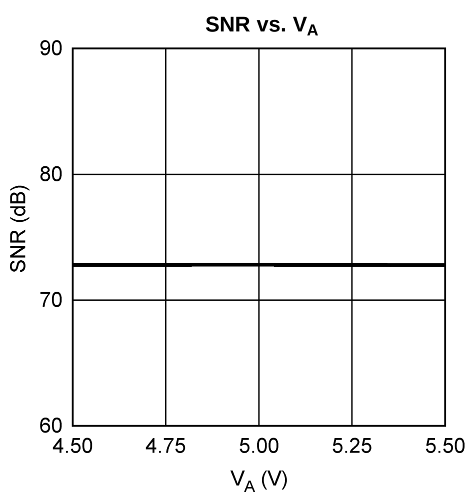

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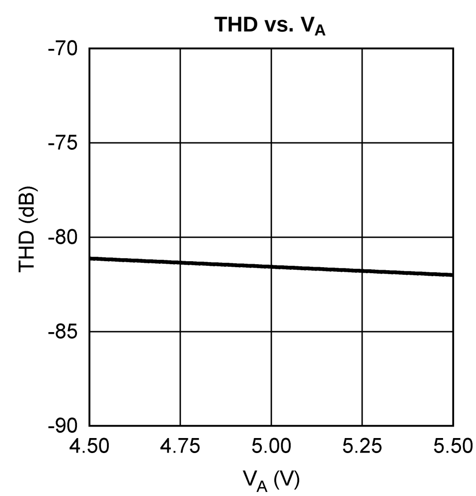
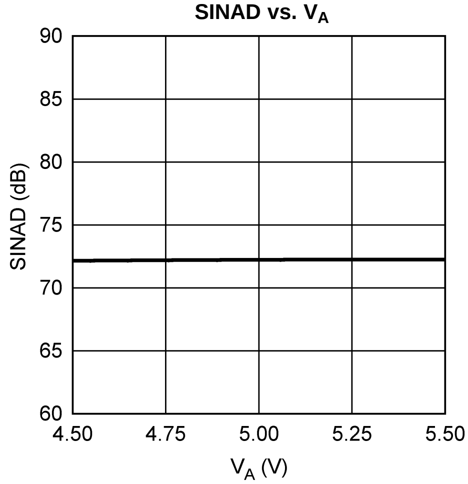


Figure 31.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.



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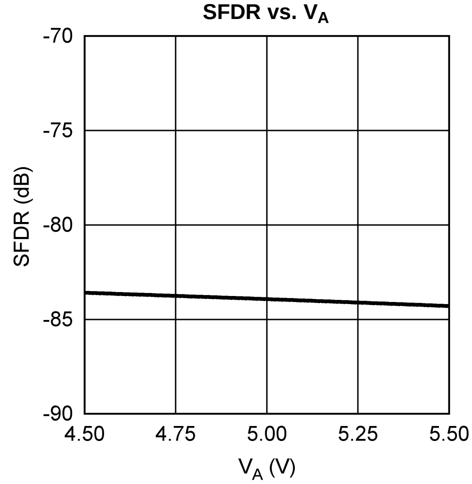


Figure 33.

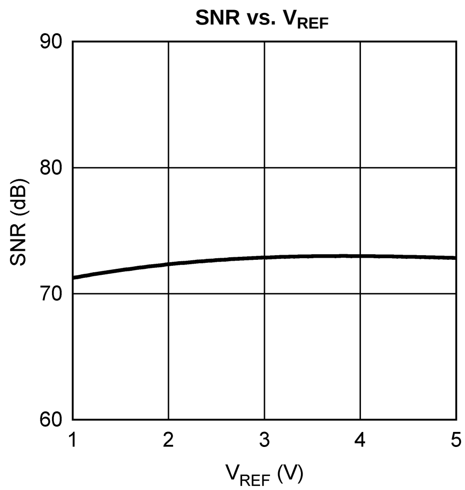


Figure 34.

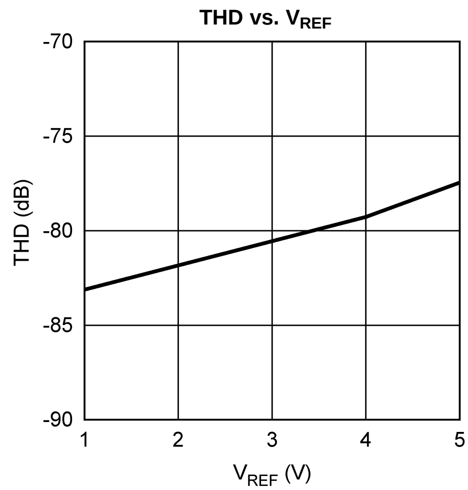
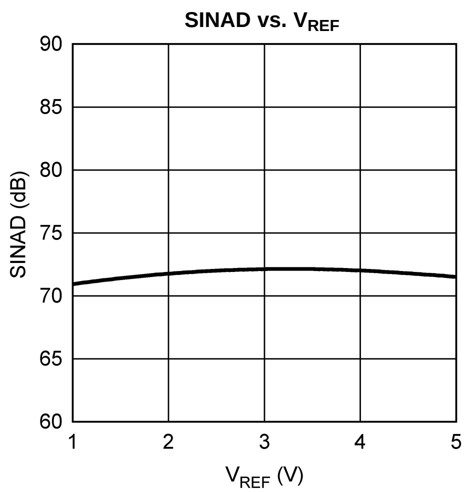


Figure 35.



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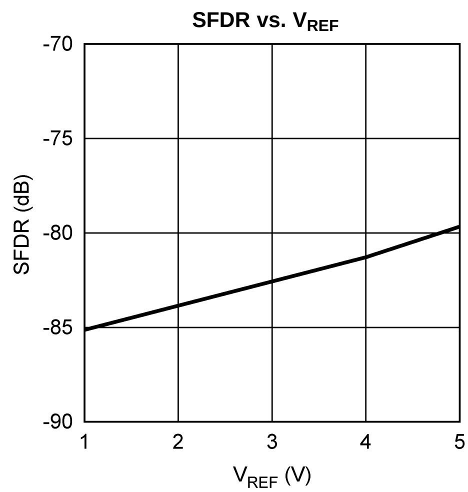


Figure 37.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

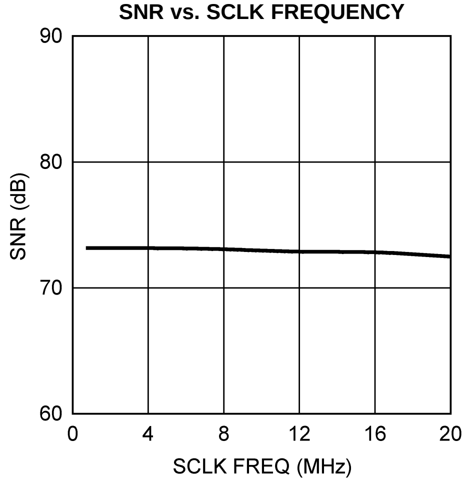
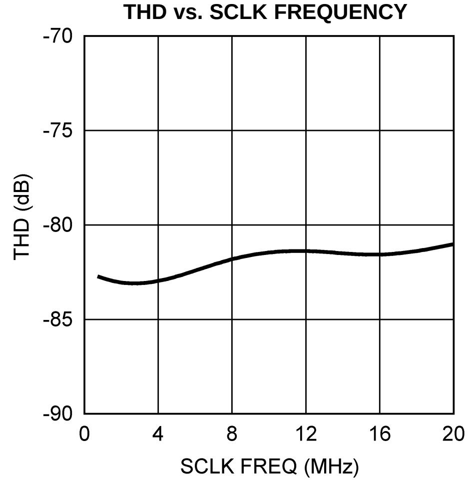


Figure 38.



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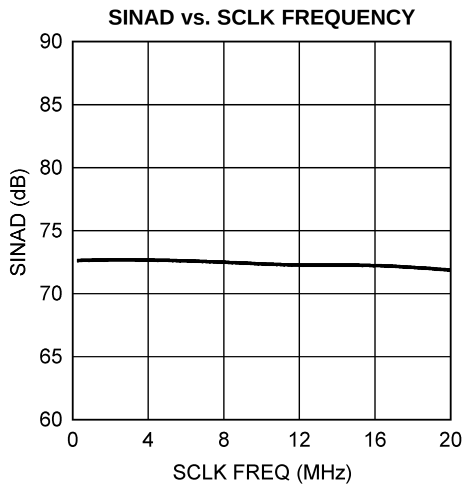

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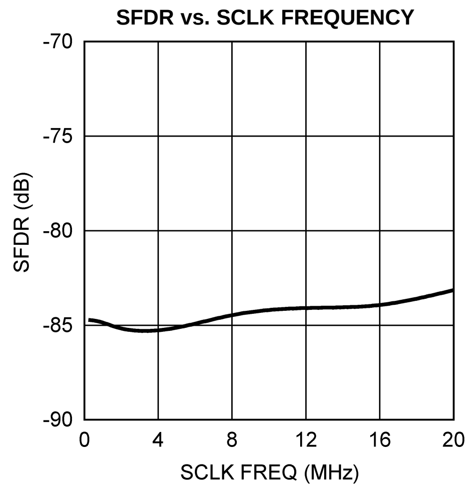

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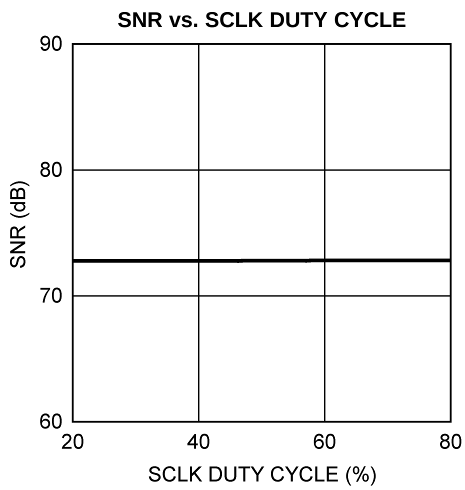

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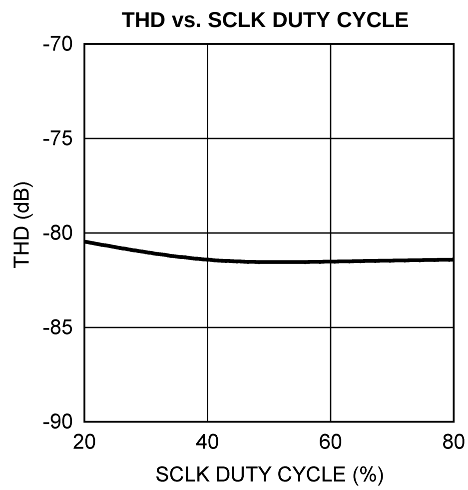


Figure 43.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

SINAD vs. SCLK DUTY CYCLE

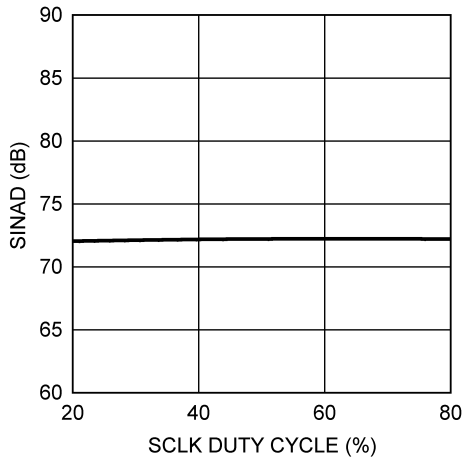


Figure 44.

SFDR vs. SCLK DUTY CYCLE

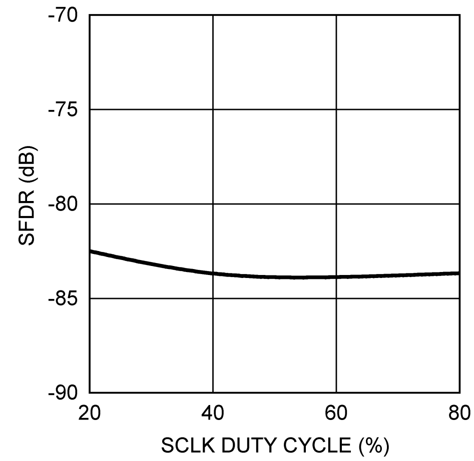


Figure 45.

SNR vs. INPUT FREQUENCY

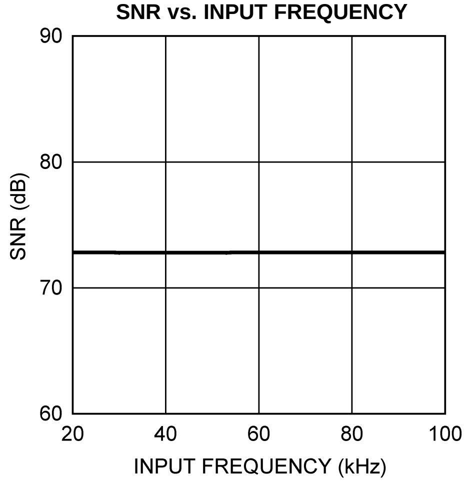


Figure 46.

THD vs. INPUT FREQUENCY

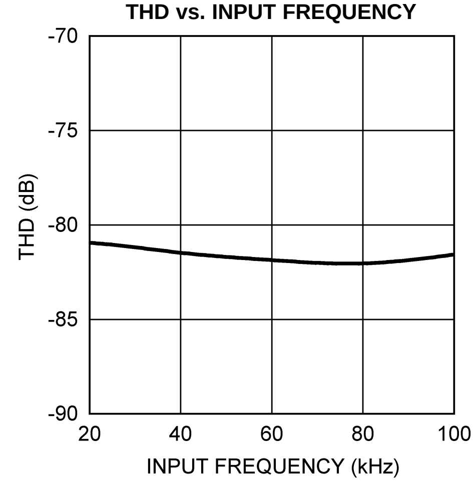


Figure 47.

SINAD vs. INPUT FREQUENCY

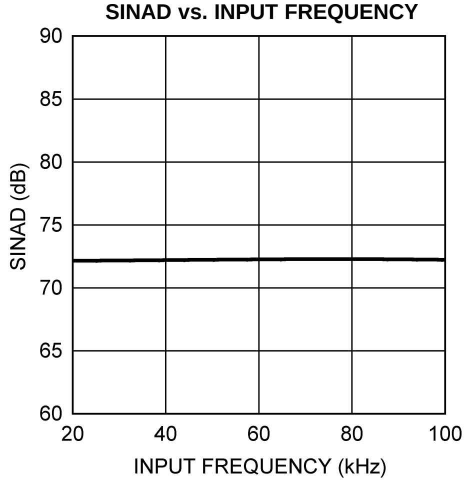


Figure 48.

SFDR vs. INPUT FREQUENCY

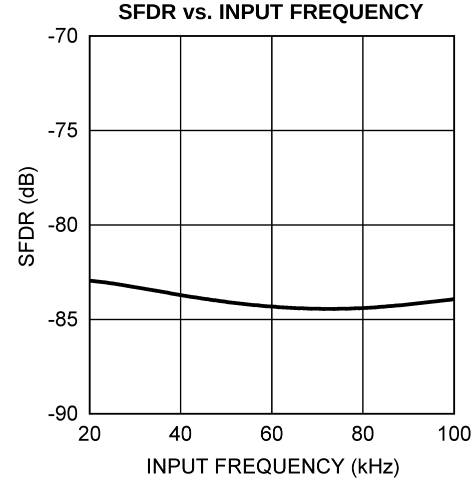
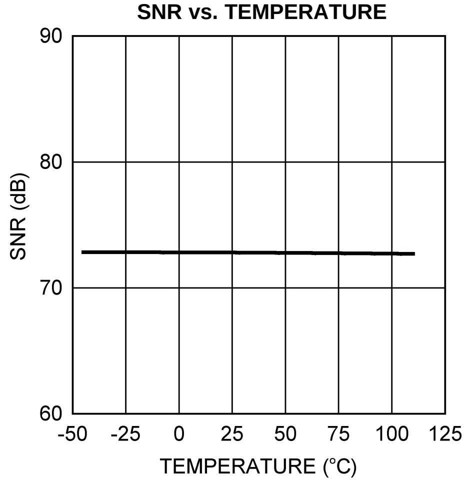


Figure 49.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.



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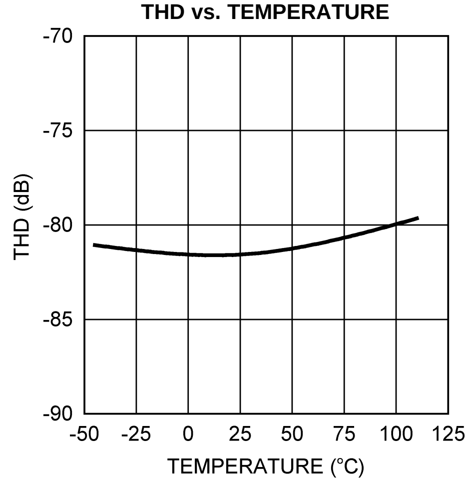

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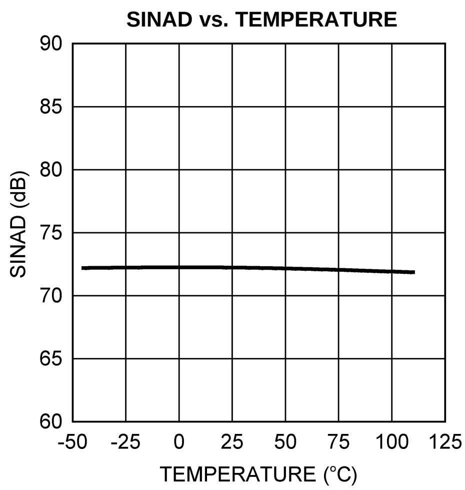

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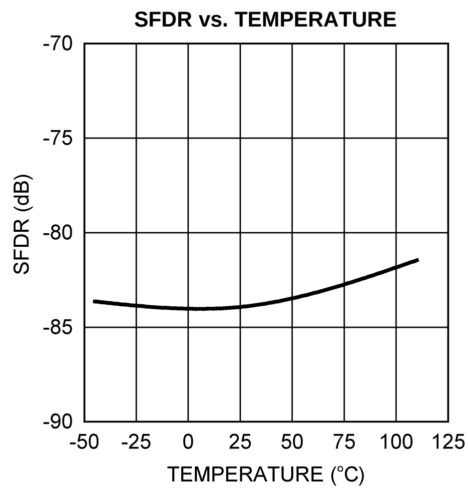

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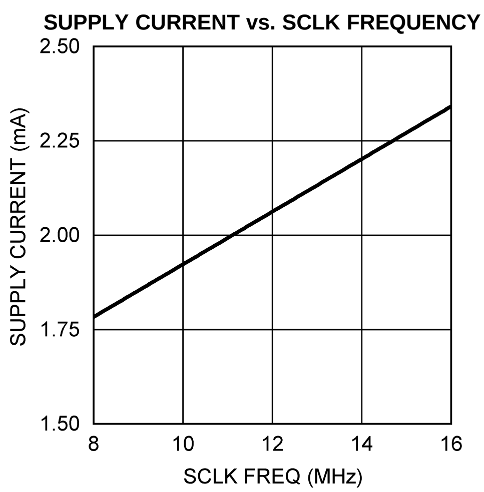

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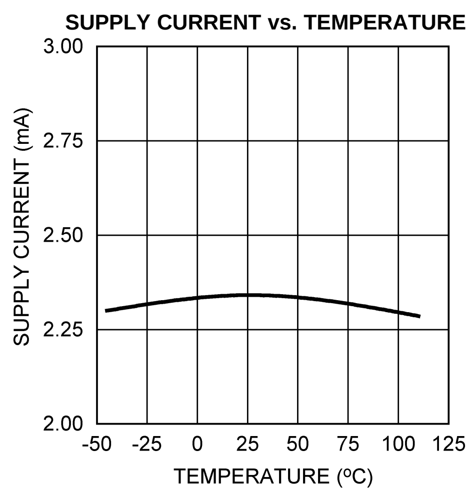

Figure 55.

Typical Performance Characteristics (continued)

V_A = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

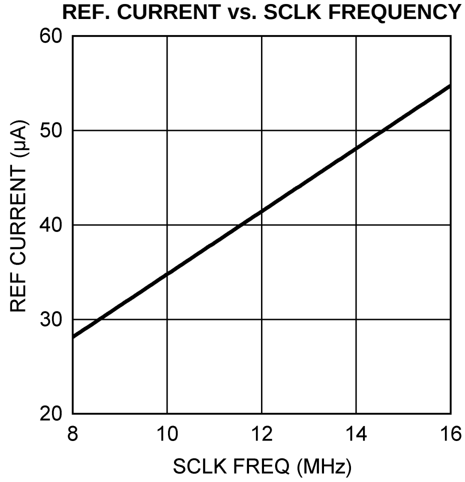

Figure 56.

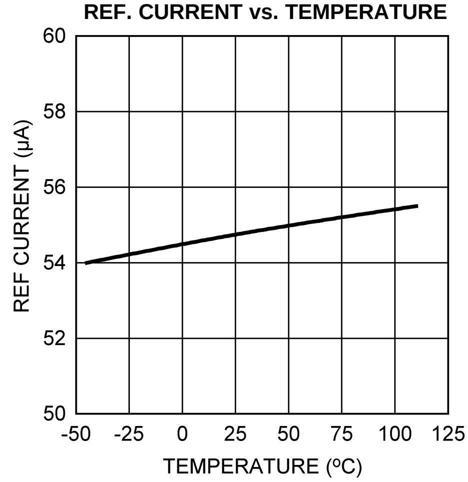

Figure 57.

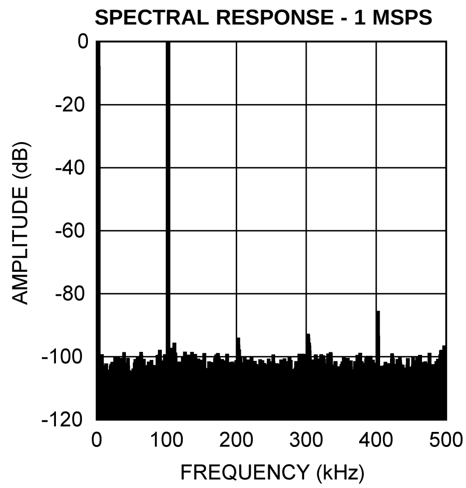

Figure 58.

Functional Description

The ADC121S705 analog-to-digital converter uses a successive approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample/hold function. The architecture and process allow the ADC121S705 to acquire and convert an analog signal at sample rates up to 1 MSPS while consuming very little power.

The ADC121S705 requires an external reference, external clock, and a single +5V power source that can be as low as +4.5V. The external reference can be any voltage between 1V and V_A. The value of the reference voltage determines the range of the analog input, while the reference input current depends upon the conversion rate.

The external clock can take on values as indicated in the Electrical Characteristics of this data sheet. The duty cycle of the clock is essentially unimportant, provided the minimum clock high and low times are met. The minimum clock frequency is set by internal capacitor leakage. Each conversion requires 16 SCLK cycles to complete. If less than 12 bits of conversion data are required, $\overline{CS}$ can be brought high at any point during the conversion. This procedure of terminating a conversion prior to completion is often referred to as short cycling.

The analog input is presented to the two input pins: +IN and –IN. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit first, at the D_{OUT} pin. The digital data that is provided at the D_{OUT} pin is that of the conversion currently in progress. With $\overline{CS}$ held low after the conversion is complete, the ADC121S705 continuously converts the analog input. The digital data on D_{OUT} can be clocked into the receiving device on the SCLK rising edges. See Serial Digital Interface and Timing Diagrams for more information.

REFERENCE INPUT

The externally supplied reference voltage sets the analog input range. The ADC121S705 will operate with a reference voltage in the range of 1V to V_A.

As the reference voltage is reduced, the range of input voltages corresponding to each digital output code is reduced. That is, a smaller analog input range corresponds to one LSB (Least Significant Bit). The size of one LSB is equal to twice the reference voltage divided by 4096. When the LSB size goes below the noise floor of the ADC121S705, the noise will span an increasing number of codes and overall performance will suffer. For example, dynamic signals will have their SNR degrade, while D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, since offset and gain errors are specified in LSB, any offset and/or gain errors inherent in the A/D converter will increase in terms of LSB size as the reference voltage is reduced.

The reference input and the analog inputs are connected to the capacitor array through a switch matrix when the input is sampled. Hence, the only current required at the reference and at the analog inputs is a series of transient spikes.

Lower reference voltages will decrease the current pulses at the reference input and will slightly decrease the average input current. The reference current changes only slightly with temperature. See Figure 56 and Figure 57 in Typical Performance Characteristics for additional details.

ANALOG SIGNAL INPUTS

The ADC121S705 has a differential input, and the effective input voltage that is digitized is (+IN) − (−IN). As is the case with all differential input A/D converters, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. Yet, the ADC121S705 can be presented with a single-ended input.

The current required to recharge the input sampling capacitor will cause voltage spikes at +IN and −IN. Do not try to filter out these noise spikes. Rather, ensure that the transient settles out during the acquisition period (three SCLK cycles after the fall of $\overline{CS}$).

Differential Input Operation

With a fully differential input voltage or signal, a positive full scale output code (0111 1111 1111b or 7FFh) will be obtained when (+IN) − (−IN) ≥ V_{REF} − 1.5 LSB. A negative full scale code (1000 0000 0000b or 800h) will be obtained when (+IN) − (−IN) ≤ $-V_{REF}$ + 0.5 LSB. This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code.

Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC121S705 should be driven with a signal or voltages that have a maximum to minimum value range that is equal to or less than twice the reference voltage. The inverting input (−IN) should be biased at a stable voltage that is halfway between these maximum and minimum values.

Since the design of the ADC121S705 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrades by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

Input Common Mode Voltage

The allowable input common mode voltage (V_{CM}) range depends upon the supply and reference voltages used for the ADC121S705. The ranges of V_{CM} are depicted in Figure 59 and Figure 60. The minimum and maximum common mode voltages for differential and single-ended operation are shown in Table 1.

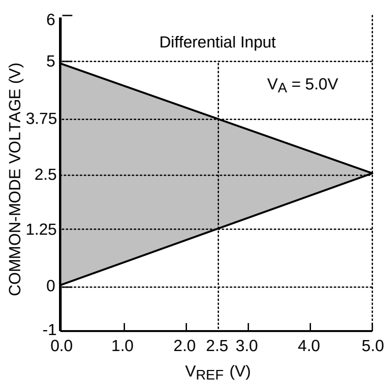

Figure 59. V_{CM} range for Differential Input operation

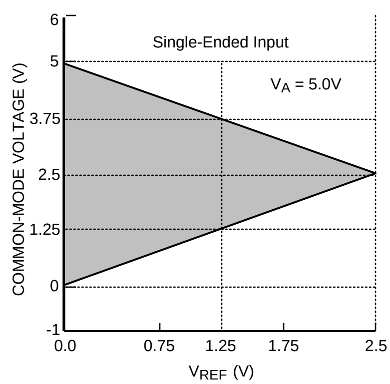

Figure 60. V_{CM} range for single-ended operation

Table 1. Allowable V_{CM} Range

Input Signal	Minimum V_{CM}	Maximum V_{CM}
Differential	V_{REF} / 2	$V_A - V_{REF}$ / 2
Single-Ended	V_{REF}	$V_A - V_{REF}$

SERIAL DIGITAL INTERFACE

The ADC121S705 communicates via a synchronous 3-wire serial interface as shown in Timing Diagrams. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. The ADC121S705's DOUT pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low; thus $\overline{CS}$ acts as an output enable.

During the first three cycles of SCLK, the ADC121S705 is in acquisition mode (t_{ACQ}), acquiring the input voltage. For the next thirteen SCLK cycles (t_{CONV}), the conversion is accomplished and the data is clocked out. SCLK falling edges one through four clock out leading zeros while falling edges five through sixteen clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC121S705 will re-enter acquisition mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the conversion mode on the N*16+4th falling edge of SCLK as shown in Figure 2. "N" is an integer value.

The ADC121S705 can enter acquisition mode under three different conditions. The first condition involves $\overline{CS}$ going low (asserted) with SCLK high. In this case, the ADC121S705 enters acquisition mode on the first falling edge of SCLK after $\overline{CS}$ is asserted. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC121S705 automatically enters acquisition mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC121S705 enters acquisition mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, see Figure 6 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

$\overline{CS}$ Input

The $\overline{CS}$ (chip select bar) input is CMOS compatible and is active low. The ADC121S705 is in normal mode when $\overline{CS}$ is low and power-down mode when $\overline{CS}$ is high. $\overline{CS}$ frames the conversion window. The falling edge of $\overline{CS}$ marks the beginning of a conversion and the rising of $\overline{CS}$ marks the end of a conversion window. Multiple conversions can occur within a given conversion frame with each conversion requiring sixteen SCLK cycles.

SCLK Input

The SCLK (serial clock) is used as the conversion clock and to clock out the conversion results. This input is CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC121S705 offers ensured performance with the clock rates indicated in the electrical table.

Data Output

The output data format of the ADC121S705 is two's complement, as shown in Table 2. This table indicates the ideal output code for the given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is sent on the falling edge of SCLK.

While most receiving systems will capture the digital output bits on the rising edge of SCLK, the falling edge of SCLK may be used to capture each bit if the minimum hold time (t_{DH}) for D_{OUT} is acceptable. See Figure 5 for DOUT hold and access times.

D_{OUT} is enabled on the falling edge of $\overline{CS}$ and disabled on the rising edge of $\overline{CS}$. If $\overline{CS}$ is raised prior to the 16th falling edge of SCLK, the current conversion is aborted and D_{OUT} will go into its high impedance state. A new conversion will begin when $\overline{CS}$ is taken LOW.

Table 2. Ideal Output Code vs. Input Voltage

Description	Analog Input, (+IN) − (−IN)	2's Complement Binary Output	2's Comp. Hex Code
+ Full Scale	V_{REF} − 1.5 LSB	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
Midscale − 1 LSB	0V − 1 LSB	1111 1111 1111	FFF
− Full Scale	−V_{REF} − 0.5 LSB	1000 0000 0000	800

APPLICATIONS INFORMATION

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC121S705:

$-40°C \le T_A \le +105°C$

$+4.5V \le V_A \le +5.5V$

$1V \le V_{REF} \le V_A$

$8\ MHz \le f_{CLK} \le 16\ MHz$

V_{CM}: See Input Common Mode Voltage

POWER CONSUMPTION

The architecture, design, and fabrication process allow the ADC121S705 to operate at conversion rates up to 1 MSPS while consuming very little power. The ADC121S705 consumes the least amount of power while operating in power down mode. For applications where power consumption is critical, the ADC121S705 should be operated in power down mode as often as the application will tolerate. To further reduce power consumption, stop the SCLK while $\overline{CS}$ is high.

Short Cycling

Another way of saving power is to short cycle the conversion process. This is done by pulling $\overline{CS}$ high after the last required bit is received from the ADC121S705 output. This is possible because the ADC121S705 places the latest converted data bit on D_{OUT} as it is generated. If only 8-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ high after the 8th bit has been clocked out. Halting the conversion after the last needed bit is outputted is called short cycling.

Short cycling can be used to lower the power consumption in those applications that do not need a full 12-bit resolution, or where an analog signal is being monitored until some condition occurs. For example, it may not be necessary to use the full 12-bit resolution of the ADC121S705 as long as the signal being monitored is within certain limits. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC121S705 spends more time in power down mode and less time in the conversion mode.

Burst Mode Operation

Normal operation of the ADC121S705 requires the SCLK frequency to be sixteen times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 500 kSPS, the ADC121S705 should be run with an SCLK frequency of 16 MHz and a $\overline{CS}$ rate as slow as the system requires. When this is accomplished, the ADC121S705 is operating in burst mode. The ADC121S705 enters into power down mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in power down mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

TIMING CONSIDERATIONS

Proper operation requires that the fall of $\overline{CS}$ not occur simultaneously with a rising edge of SCLK. If the fall of $\overline{CS}$ occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and characteristics of the individual device. To ensure that the data is always clocked out at a given time (the 5th falling edge of SCLK), it is essential that the fall of $\overline{CS}$ always meet the timing requirement specified in the Timing Specifications.

PCB LAYOUT AND CIRCUIT CONSIDERATIONS

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low reference voltage or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

Power Supply

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC121S705 should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF to 10 µF capacitor should be used to bypass the ADC121S705 supply, with the 0.1 µF capacitor placed as close to the ADC121S705 package as possible.

Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1 µF is preferred. While the ADC121S705 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference input that must settle out while SCLK is high. Since these transient spikes can be as high as 20 mA, it is important that the reference circuit be capable of providing this much current and settle out during the first three clock periods (acquisition time).

The reference input of the ADC121S705, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if the reference voltage is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4132 and LM4140 series reference families are excellent choices for a reference source.

Power and Ground Planes

A single ground plane and the use of two or more power planes is recommended. The power planes should all be in the same board layer and will define the analog, digital, and high power board areas. Lines associated with these areas should always be routed within their respective areas.

The GND pin on the ADC121S705 should be connected to the ground plane at a quiet point. Avoid connecting the GND pin too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

APPLICATION CIRCUITS

The following figures are examples of the ADC121S705 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

Data Acquisition

Figure 61 shows a basic low cost, low power data acquisition circuit. Maximum clock rate with a minimum sample rate can reduce the power consumption further.

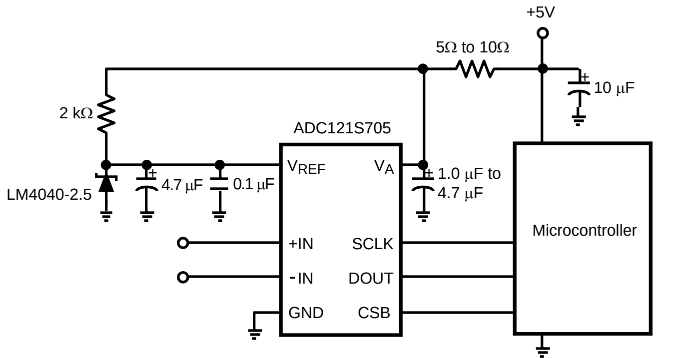

Figure 61. Low cost, low power Data Acquisition System

Pressure Sensor

Figure 62 shows an example of interfacing a pressure sensor to the ADC121S705. A digital-to-analog converter (DAC) is used to bias the pressure sensor. The DAC081S101 provides a means for dynamically adjusting the sensitivity of the sensor. A shunt reference voltage of 2.5V is used as the reference for the ADC121S705. The ADC121S705, DAC081S101, and the LM4040 are all powered from the same voltage source.

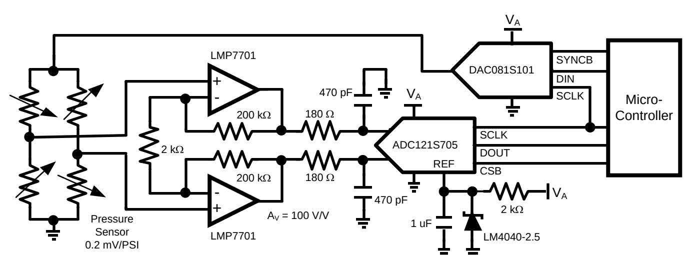

Figure 62. Interfacing the ADC121S705 for a Pressure Sensor

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC121S705CIMM/NOPB	NRND	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 0	X1AC	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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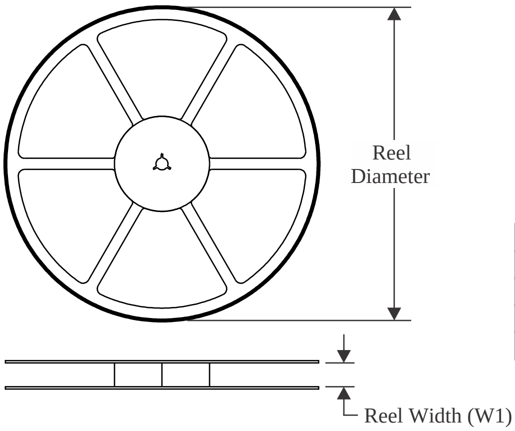
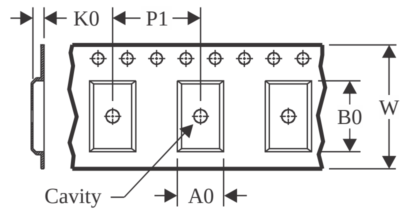
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

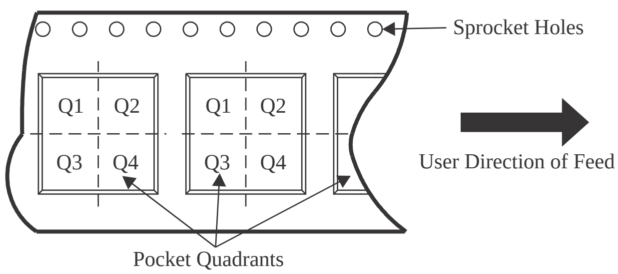


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

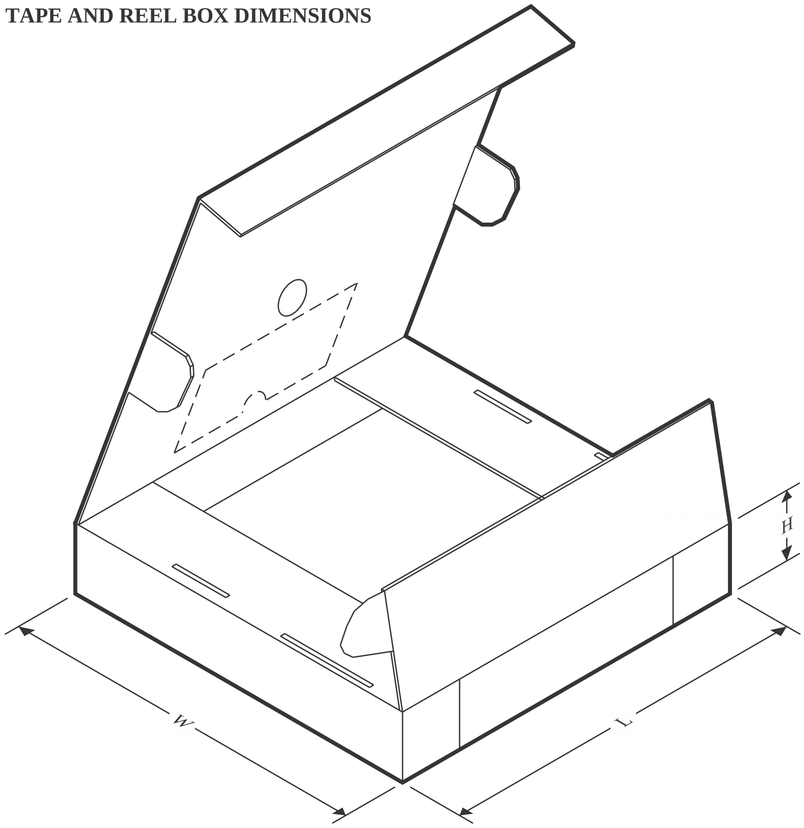
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

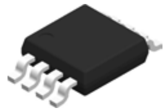
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC121S705CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

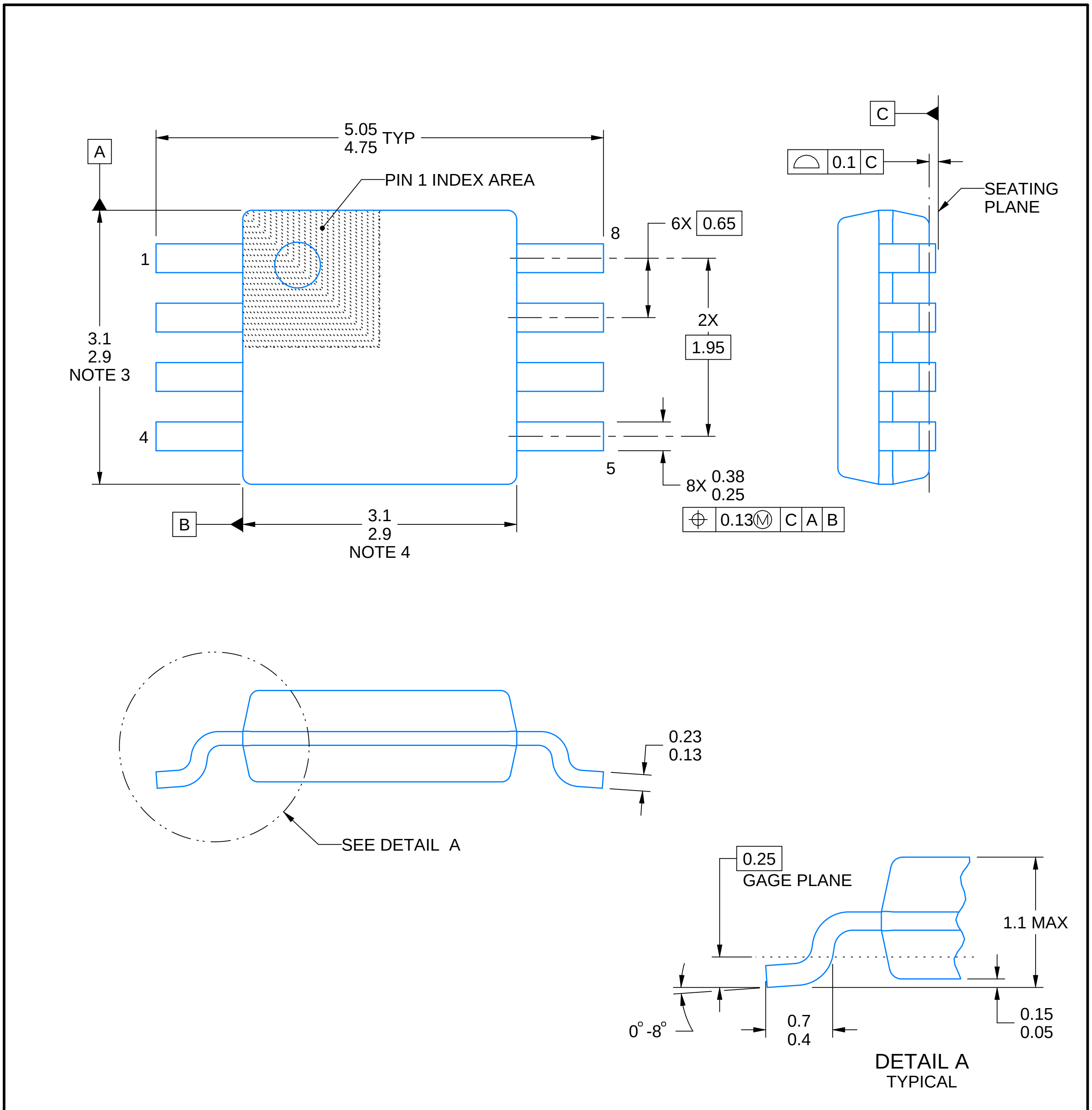
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC121S705CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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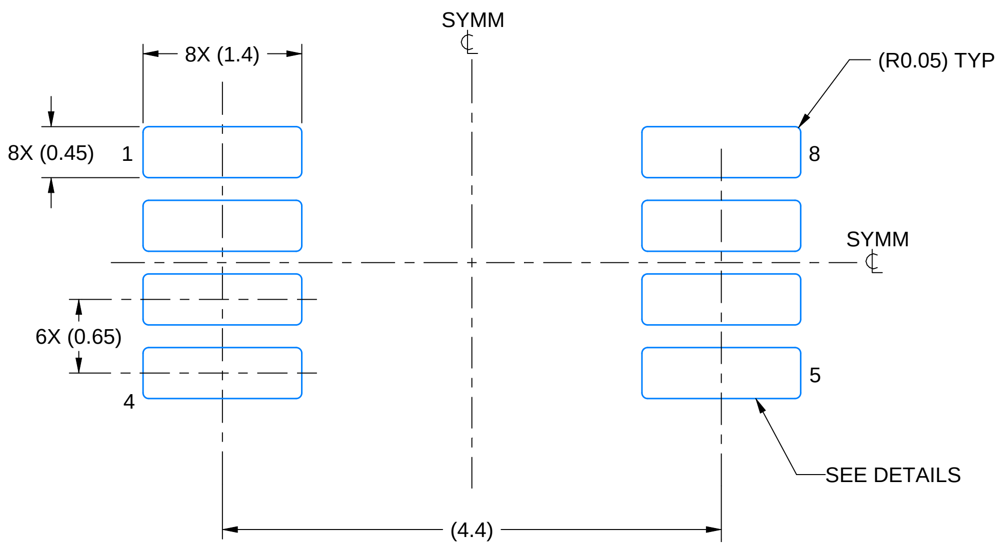
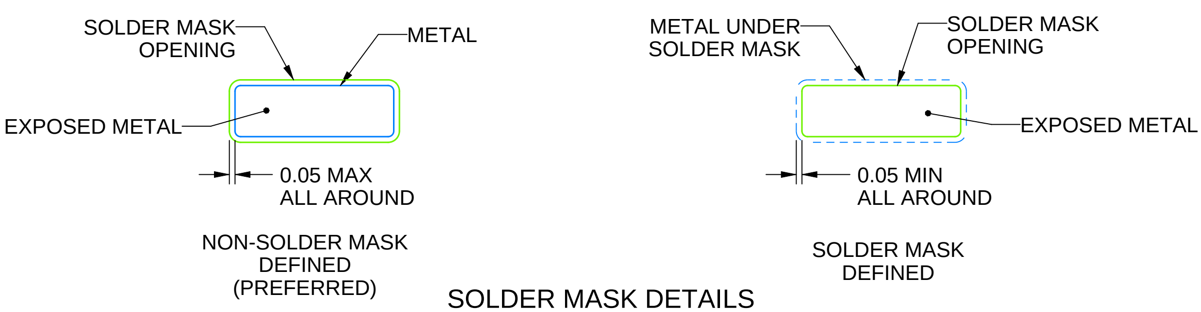
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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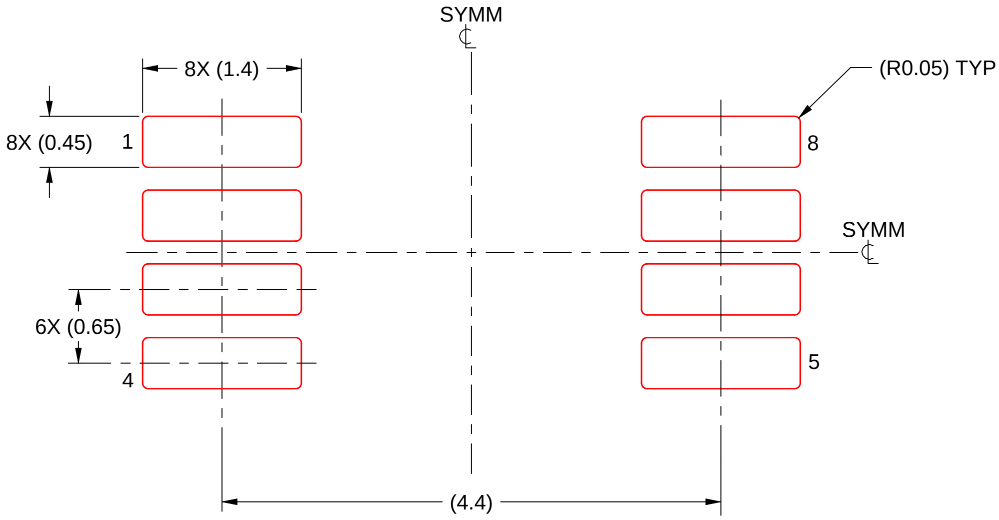
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.