

54AC16245, 74AC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS235A – MARCH 1990 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) Package, 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings

description

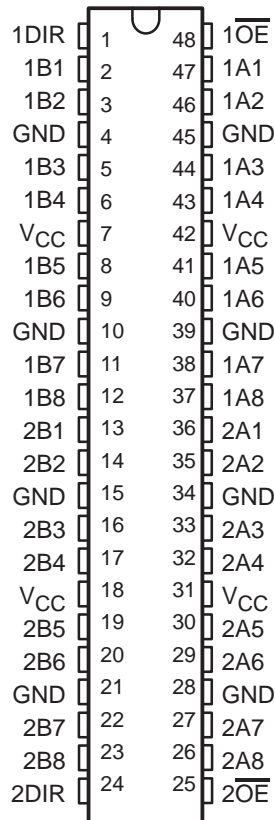
The 'AC16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The output-enable input (\overline{OE}) can be used to disable the devices so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16245 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74AC16245 is characterized for operation from -40°C to 85°C.

54AC16245 . . . WD PACKAGE
74AC16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

| CONTROL INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to bus |
| H | X | Isolation |



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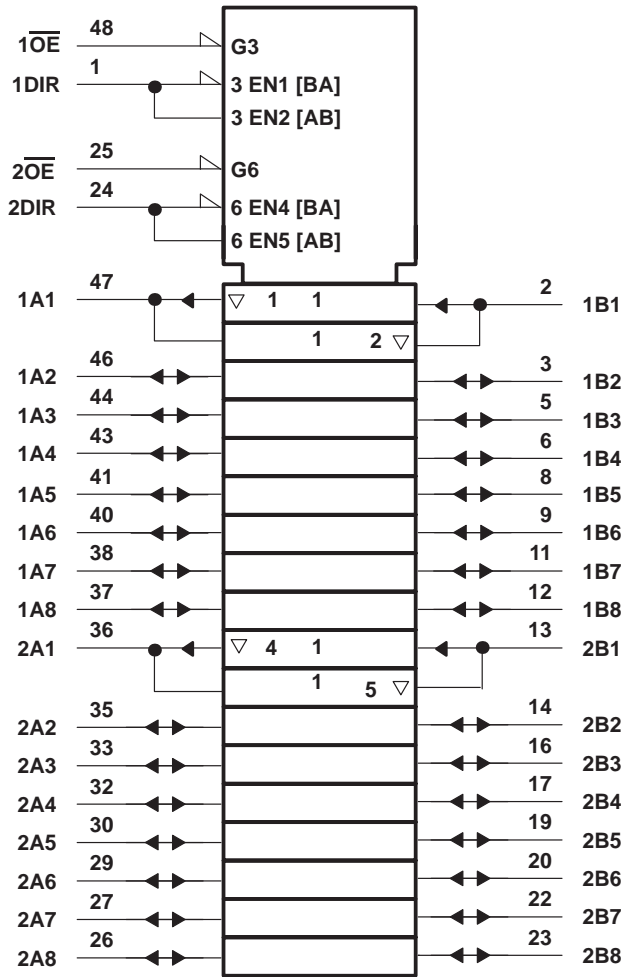
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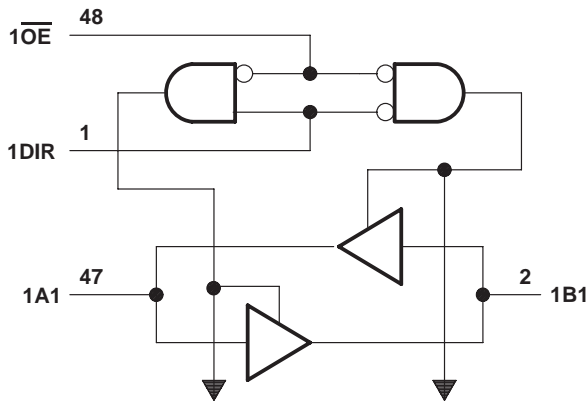
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logic symbol†

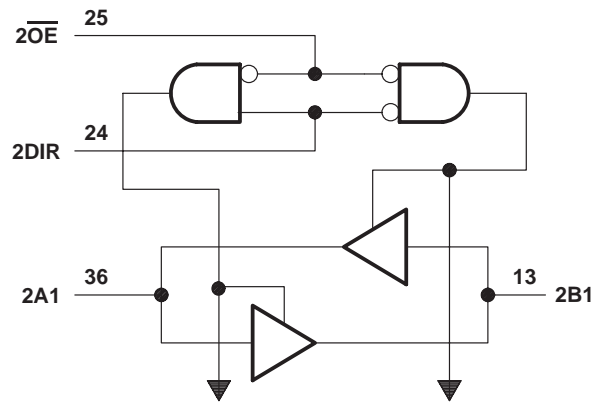


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Transceivers



To Seven Other Transceivers



54AC16245, 74AC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±400 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package | 0.85 W |
| DL package | 1.2 W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

| | | 54AC16245 | | | 74AC16245 | | | UNIT |
|---------------------|------------------------------------|------------------|-----|----------|------------------|------------------|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage (see Note 4) | 3 | 5 | 5.5 | 3 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 3$ V | | 2.1 | $V_{CC} = 3$ V | | 2.1 | V |
| | | $V_{CC} = 4.5$ V | | 3.15 | $V_{CC} = 4.5$ V | | 3.15 | |
| | | $V_{CC} = 5.5$ V | | 3.85 | $V_{CC} = 5.5$ V | | 3.85 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 3$ V | | | 0.9 | $V_{CC} = 3$ V | | 0.9 |
| | | $V_{CC} = 4.5$ V | | | 1.35 | $V_{CC} = 4.5$ V | | 1.35 |
| | | $V_{CC} = 5.5$ V | | | 1.65 | $V_{CC} = 5.5$ V | | 1.65 |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 3$ V | | | –4 | $V_{CC} = 3$ V | | –4 |
| | | $V_{CC} = 4.5$ V | | | –24 | $V_{CC} = 4.5$ V | | –24 |
| | | $V_{CC} = 5.5$ V | | | –24 | $V_{CC} = 5.5$ V | | –24 |
| I_{OL} | Low-level output current | $V_{CC} = 3$ V | | | 12 | $V_{CC} = 3$ V | | 12 |
| | | $V_{CC} = 4.5$ V | | | 24 | $V_{CC} = 4.5$ V | | 24 |
| | | $V_{CC} = 5.5$ V | | | 24 | $V_{CC} = 5.5$ V | | 24 |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| T_A | Operating free-air temperature | –55 | | 125 | –40 | | 85 | °C |

- NOTES: 3. All unused pins (input and I/O) must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage power supply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | 54AC16245 | | 74AC16245 | | UNIT |
|---------------------------|---|-----------------|-----------------------|-----|------|-----------|------|-----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | V | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | 4.8 | | |
| I _{OH} = -75 mA† | 5.5 V | | | | 3.85 | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 3 V | | | 0.1 | | | 0.1 | V | |
| | | 4.5 V | | | 0.1 | | | 0.1 | | |
| | | 5.5 V | | | 0.1 | | | 0.1 | | |
| | I _{OL} = 12 mA | 3 V | | | 0.36 | | | 0.44 | | |
| | | 4.5 V | | | 0.36 | | | 0.44 | | |
| | | 5.5 V | | | 0.36 | | | 0.44 | | |
| I _{OL} = 75 mA† | 5.5 V | | | | | 1.65 | 1.65 | | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{OZ} | V _I = V _{CC} or GND | 5.5 V | | | ±0.5 | | ±5 | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 8 | | 80 | 80 | μA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 4.5 | | | | pF | |
| C _o | V _I = V _{CC} or GND | 5 V | | | 16 | | | | | |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | 54AC16245 | | 74AC16245 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|------|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | B or A | 2.5 | 7.6 | 10.4 | 2.5 | 11.9 | 2.5 | 11.9 | ns |
| t _{PHL} | | | 3.1 | 9 | 12.3 | 3.1 | 13.5 | 3.1 | 13.5 | |
| t _{PZH} | OE | A or B | 2.8 | 8.6 | 11.8 | 2.8 | 13.2 | 2.8 | 13.2 | ns |
| t _{PZL} | | | 3.9 | 12 | 16.2 | 3.9 | 18 | 3.9 | 18 | |
| t _{PHZ} | OE | A or B | 5.3 | 8.4 | 10.4 | 5.3 | 11.2 | 5.3 | 11.2 | ns |
| t _{PLZ} | | | 4.4 | 7.7 | 9.7 | 4.4 | 10.3 | 4.4 | 10.3 | |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | 54AC16245 | | 74AC16245 | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|-----|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | B or A | 2 | 4.6 | 6.9 | 2 | 7.9 | 2 | 7.9 | ns |
| t _{PHL} | | | 2.5 | 5.2 | 7.9 | 2.5 | 8.9 | 2.5 | 8.9 | |
| t _{PZH} | OE | A or B | 2.3 | 4.9 | 7.5 | 2.3 | 8.6 | 2.3 | 8.6 | ns |
| t _{PZL} | | | 3 | 6.2 | 9.5 | 3 | 10.7 | 3 | 10.7 | |
| t _{PHZ} | OE | A or B | 5 | 7.2 | 9.1 | 5 | 9.8 | 5 | 9.8 | ns |
| t _{PLZ} | | | 4.2 | 6.2 | 8.1 | 4.2 | 8.7 | 4.2 | 8.7 | |

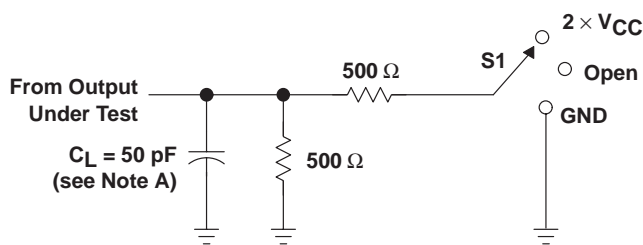
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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

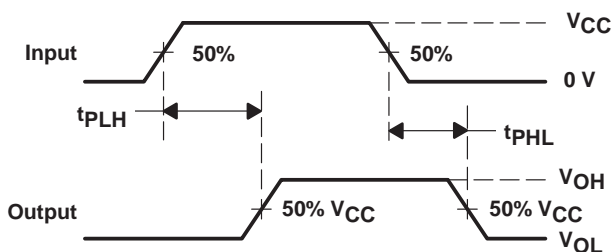
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|---|-----|------|
| C_{pd} | Power dissipation capacitance per latch | $C_L = 50\text{ pF}$, $f = 1\text{ MHz}$ | 43 | pF |
| | | | 8 | |

PARAMETER MEASUREMENT INFORMATION

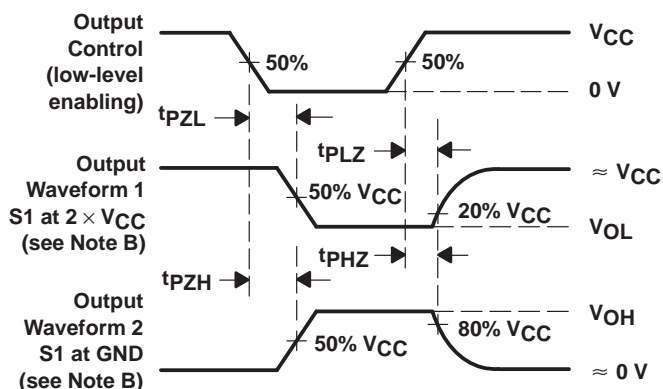


| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74AC16245DL | Obsolete | Production | SSOP (DL) 48 | - | - | Call TI | Call TI | -40 to 85 | AC16245 |
| 74AC16245DLR | Active | Production | SSOP (DL) 48 | 1000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC16245 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74AC16245DLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74AC16245DLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

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