
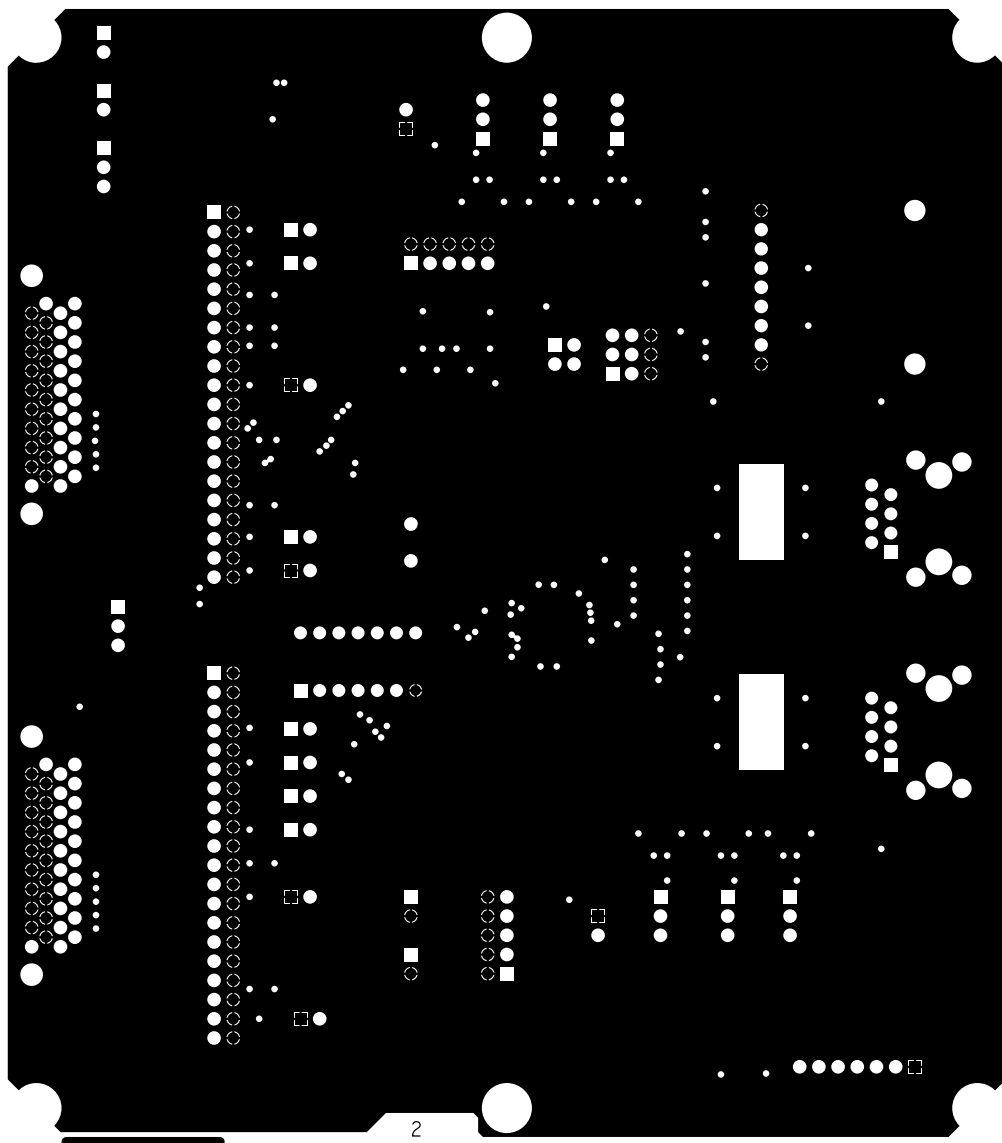



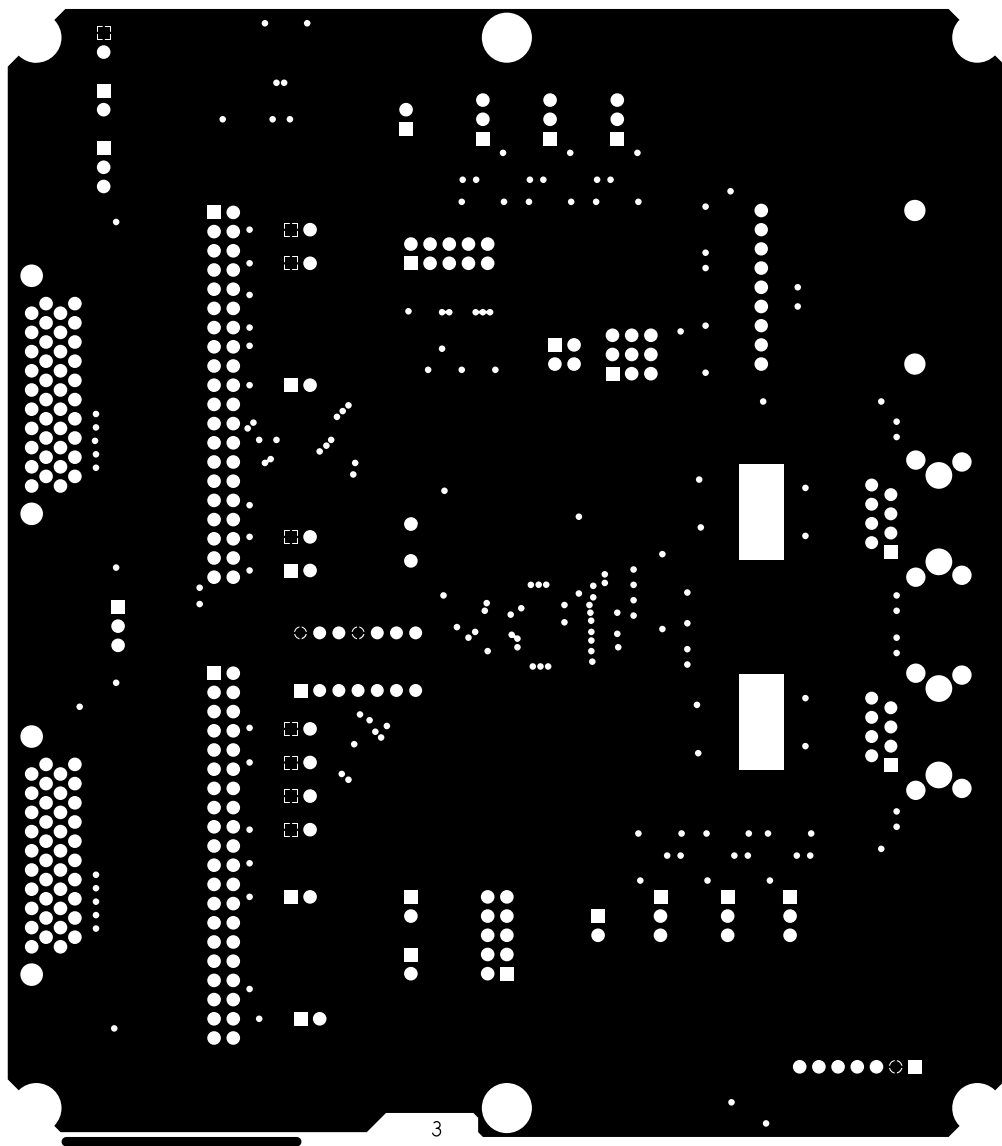
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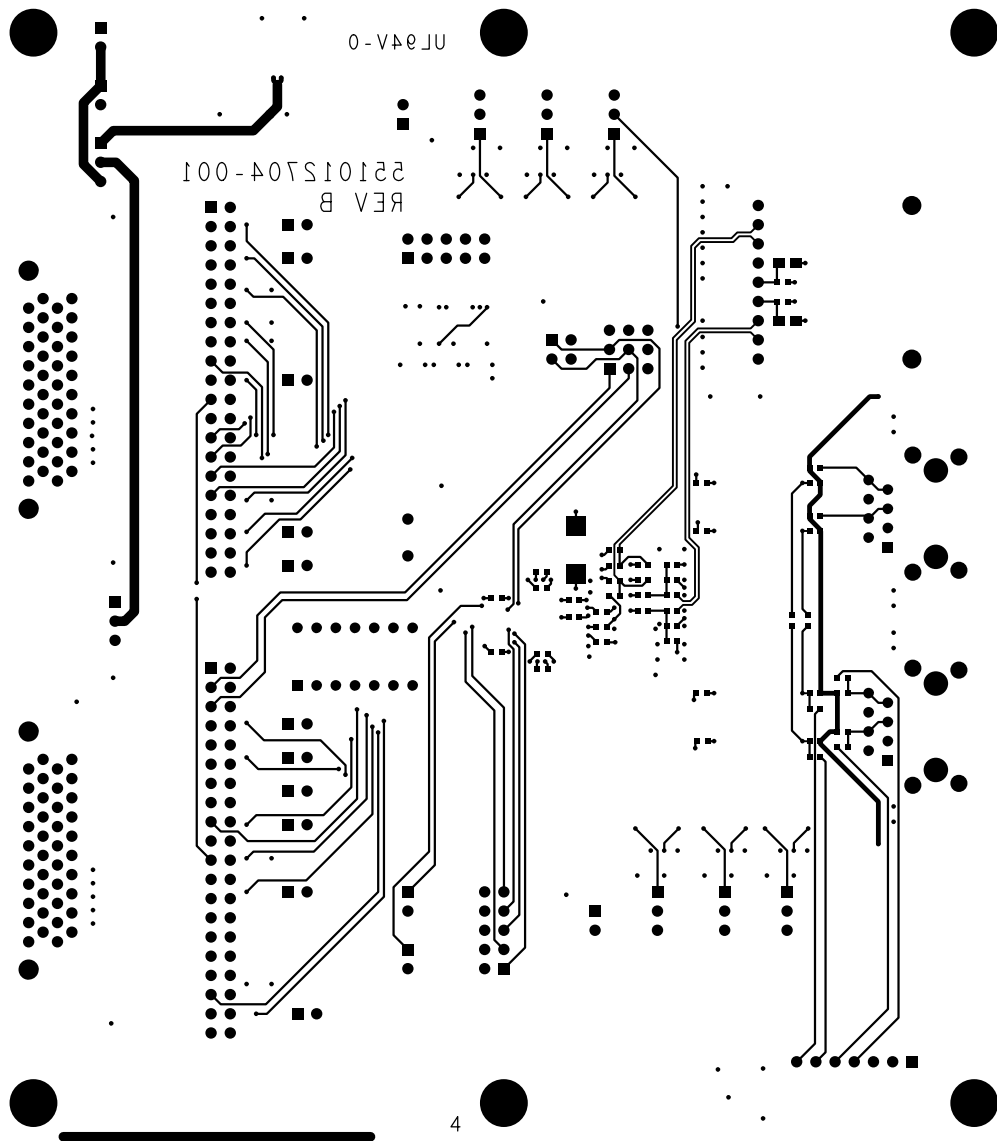
 National Semiconductor™ INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE		DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II		BOARD NO: 880012704-001	REV B
	LAYER NAME: TOP ETCH		LAYER NO: 1	SHEET 1 of 8




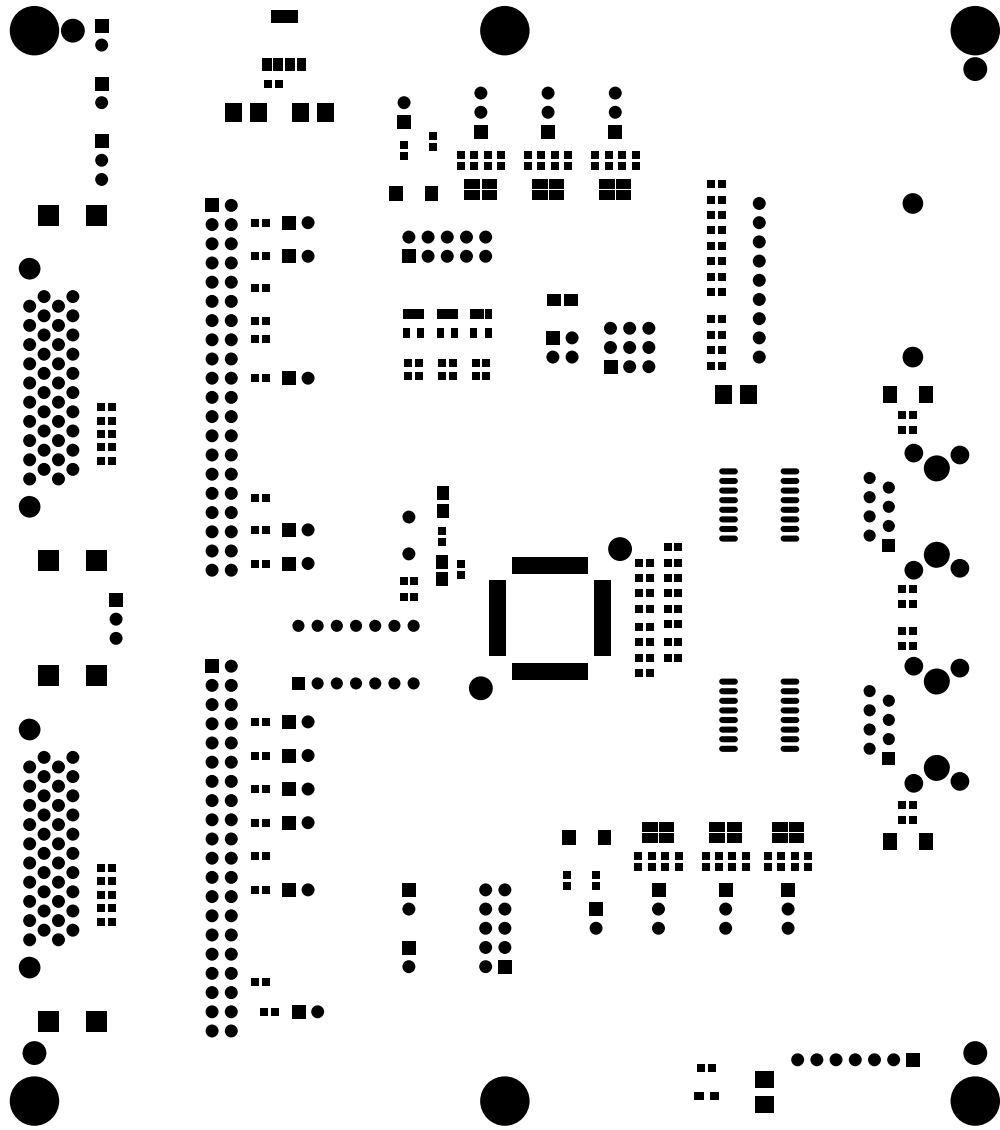
 National Semiconductor™ INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE	DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II	BOARD NO: 880012704-001	REV B
	LAYER NAME: GND	LAYER NO: 2	SHEET 2 of 8




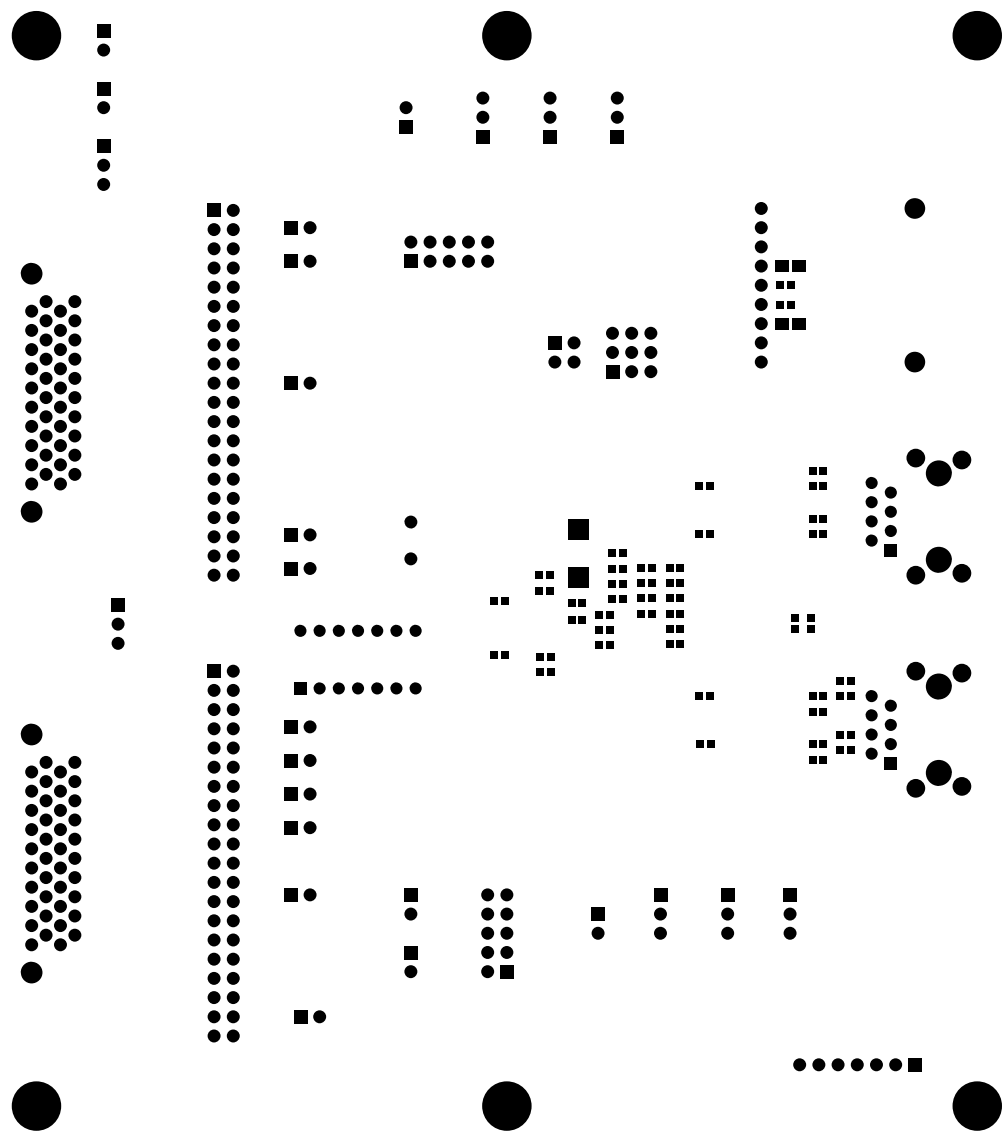
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	BOARD NAME: DP83849 DUAL PHYTER DEMO II		BOARD NO: 880012704-001	REV B
	LAYER NAME: 3V3	LAYER NO: 3	SHEET	3 of 8




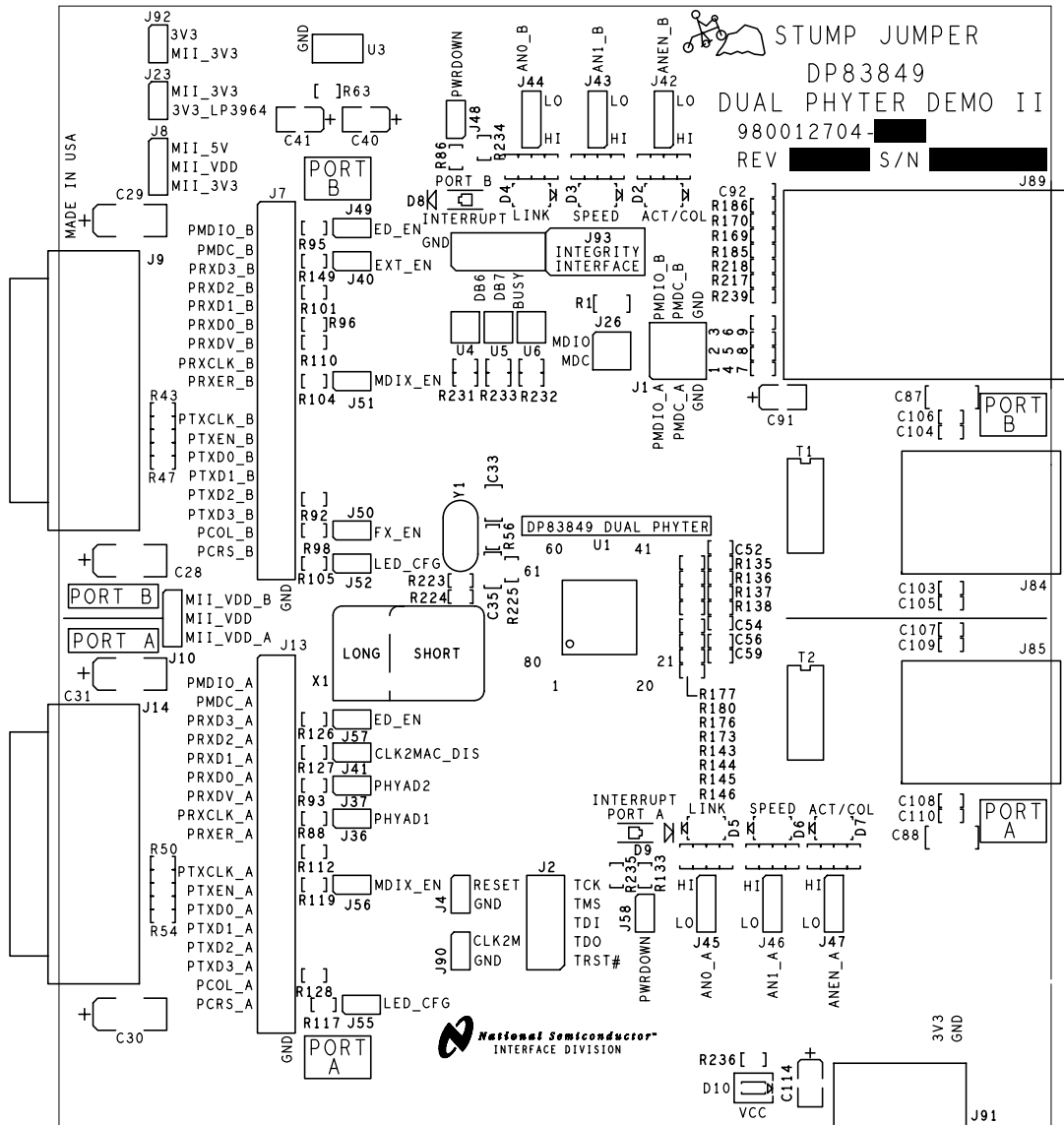
 National Semiconductor™ INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE	DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II	BOARD NO: 880012704-001	REV B
	LAYER NAME: BOTTOM ETCH	LAYER NO: 4	SHEET 4 of 8




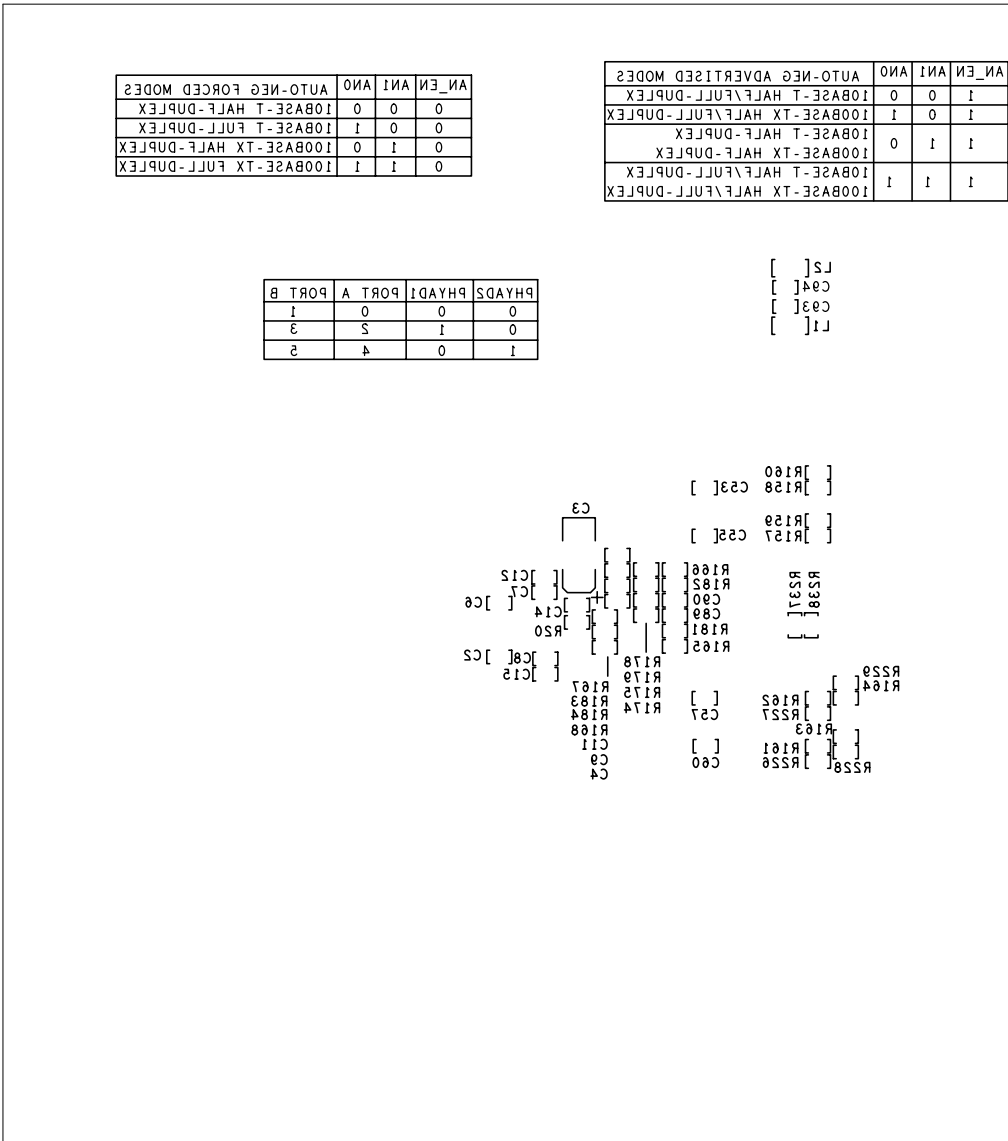
 National Semiconductor INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE	DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II	BOARD NO: 880012704-001	REV B
	LAYER NAME: TOP SOLDER MASK	LAYER NO:	SHEET 5 of 8



 National Semiconductor INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE	DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II	BOARD NO: 880012704-001	REV B
	LAYER NAME: BOTTOM SOLDER MASK	LAYER NO:	SHEET 6 of 8



 National Semiconductor INTERFACE DIVISION	ALL ARTWORK VIEWED FROM TOP SIDE	DATE: DECEMBER 16, 2005	
	BOARD NAME: DP83849 DUAL PHYTER DEMO II	BOARD NO: 880012704-001	REV B
	LAYER NAME: TOP SILKSCREEN	LAYER NO:	SHEET 7 of 8

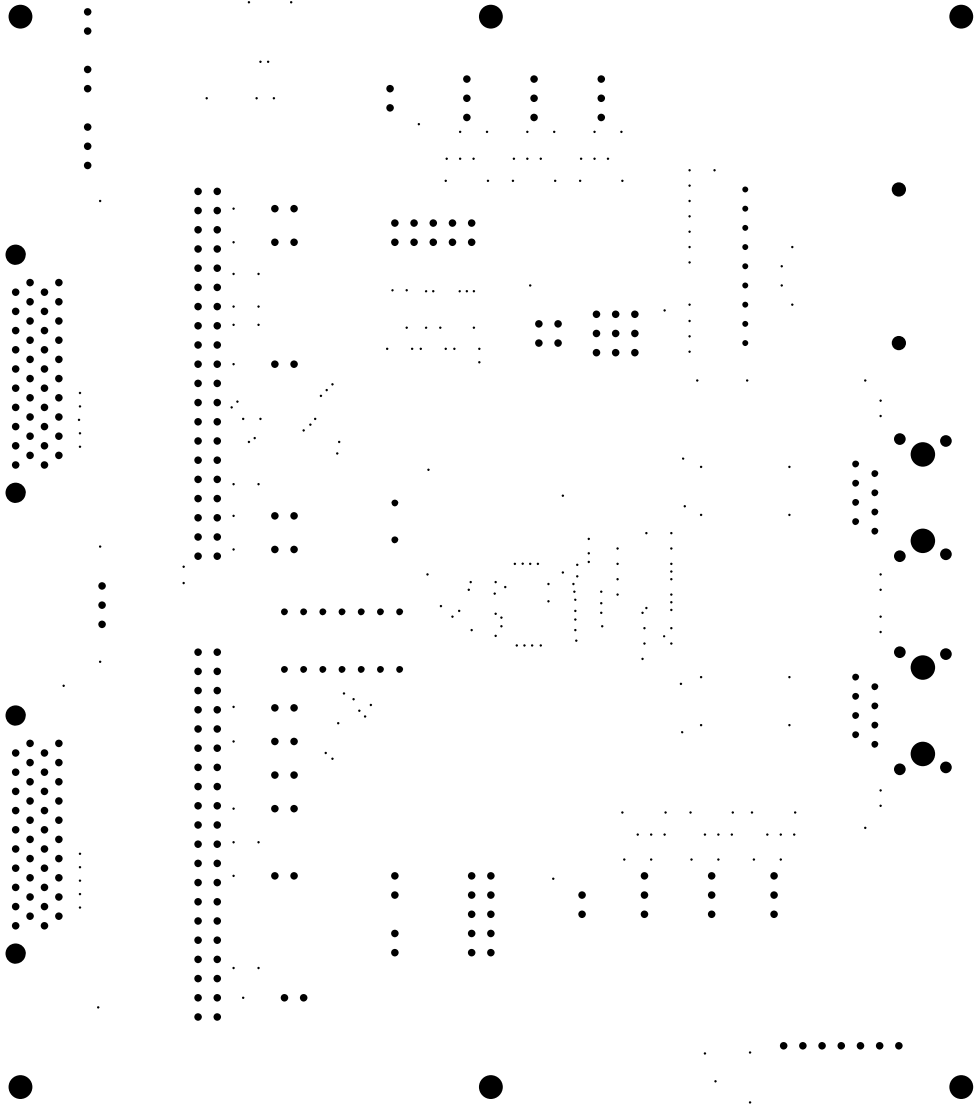


AN_EN	ANI	ANO	AUTO-NEG	FORCED MODES
0	1	1	1	100BASE-TX FULL-DUPLEX
0	1	0	1	100BASE-TX HALF-DUPLEX
0	0	1	1	100BASE-T FULL-DUPLEX
0	0	0	1	100BASE-T HALF-DUPLEX

AN_EN	ANI	ANO	AUTO-NEG	ADVERTISED MODES
1	1	1	1	100BASE-TX HALF-DUPLEX
1	1	0	1	100BASE-TX HALF-DUPLEX
1	0	1	1	100BASE-TX HALF-DUPLEX
1	0	0	1	100BASE-T HALF-DUPLEX

PHYADS	PHYADI	PORT A	PORT B
0	0	0	1
0	1	2	3
1	0	4	5

LS]
C04]
C03]
R1]



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