LM1770,LM2734,LM3370,LP5550

FPGA????????????

Literature Number: ZHCA400

POWER *designer*

Expert tips, tricks, and techniques for powerful designs

Advanced Topics in Powering FPGAs

— By Tushar Dhayagude, Marketing Manager, Power Management Products

Application	Input Voltage/ Source	Space Constraint	Operational and Light Load Efficiency
Battery Operated/ Portable	1.8V to 5.5V AA batteries, Lithium Ion cells	Severe	High efficiency, low quiescent current
Consumer (DVD, Set-top Boxes, DVR)	4.5V to 36V Wall-plug	Moderate	Low operating efficiency acceptable
Automotive	7V to 45V Battery	Minimal	Low quiescent current
Networking (Routers, Switchers)	3.3V to 12V Brick output	Moderate	Moderately high efficiency
Industrial (Automation, Process Control)	12V to 36V	Minimal	Low

Table 1. Power Requirements for Popular FPGA Applications

FPGAs have established themselves as the most flexible and reconfigurable intelligence in applications from networking and telecommunications equipment to industrial and automotive segments. More recently FPGAs have proliferated into consumer devices such as set-top boxes, DVD recorders, and video games. But future growth in FPGA usage will come from their adoption into portable devices such as GPS, medical, instrumentation, and consumer devices.

Why are the designers of portable and handheld devices turning to FPGAs now? It is because, as process technology has improved, manufacturers have made huge strides in reducing the power consumption, cost, and footprint of FPGAs. But as FPGAs proliferate into portable devices, power management becomes an increasingly challenging issue from a system perspective.

Power supply requirements are important because issues such as input voltage source, complex start-up conditions, transient response, sequencing, have to be addressed. Multiple voltages are required to power an FPGA: "Core" voltage (0.9V to 2.5V), I/O voltage (2.5V to 3.3V) and another low-noise, low-ripple voltage for auxiliary circuits (2.5V or 3.3V typ.). Furthermore, when FPGAs operate from batteries, system efficiency and battery life become crucial.

NEXT ISSUE:

RF Power Efficiency Optimization

National Semiconductor

Dual 600 mA Step-Down DC-DC Converter with I²C Interface

Highest Efficiency LM3370 Maximizes Processor Performance through Dynamic Voltage Scaling
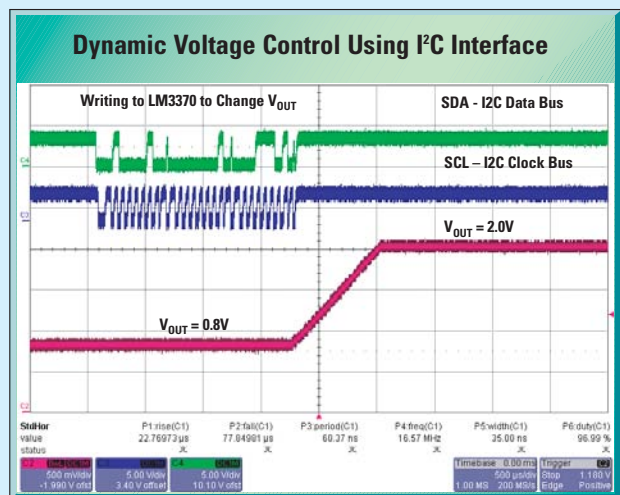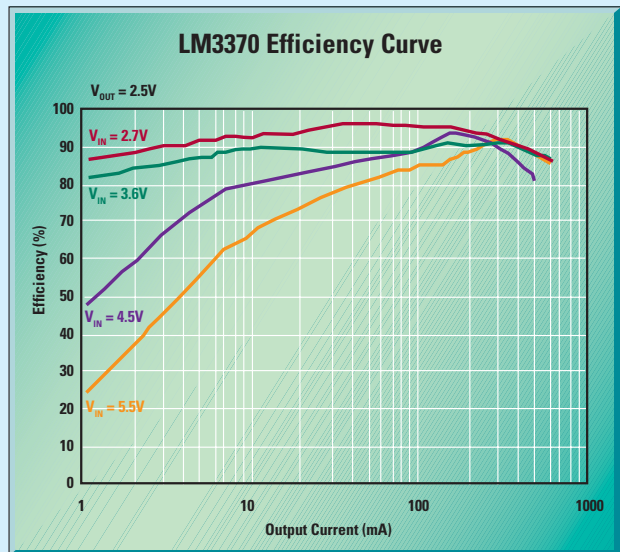
Features

- Highest efficiency: PFM-PWM mode control, 85% at 500 µA, >90% at 200 mA
- I²C interface for dynamic voltage scaling, mode control, on/off functions
- Lowest Iq in the industry (<20 µA) enables longer standby times
- Independent mode switching between auto and forced PWM mode
- Two enable pins for power sequencing
- Spread spectrum function to reduce switcher noise — ideal for RF systems
- Power-on-reset to protect the end application from sudden power losses
- V_{IN}: 2.7V to 5.5V, V_{OUT}: I²C programmable
- Integrated solution for optimal solution size

Applications

Ideal for low-power FPGAs, CPLDs, and applications processors

Product Highlight:

Highest efficiency maximizes battery life and I²C voltage control enhances processor performance

LM3370 Efficiency Curve

V_{OUT} = 2.5V
V_{IN} = 2.7V
V_{IN} = 3.6V
V_{IN} = 4.5V
V_{IN} = 5.5V

Efficiency (%)

Output Current (mA)

Dynamic Voltage Control Using I²C Interface

Writing to LM3370 to Change V_{OUT} SDA - I2C Data Bus

SCL – I2C Clock Bus

V_{OUT} = 2.0V

V_{OUT} = 0.8V

National Semiconductor LM3370

AVAILABLE LEAD-FREE

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Advanced Topics in Powering FPGAs

We discussed some of the basics of powering FPGAs in Power Designer #102[1]. Now we will examine some advanced topics in FPGA power management with a special focus on portable systems, including:

- System-level challenges in powering FPGAs in portable devices
- Monotonic rise of core voltage
- Voltage scaling and back body biasing of FPGAs to improve efficiency

System-Level Challenges

Irrespective of the FPGA being used, the end system dictates the power supply challenges. For example, in a DVD recorder with satellite broadcast, dozens of power rails may be required in addition to powering the FPGA. In such a system, power supply size and efficiency may not be a premium, but very low cost is. Conversely, in battery-operated systems, efficiency overrides all other requirements. *Table 1* shows some popular end applications for FPGAs and their power challenges.

In portable devices, efficiency during both active and stand-by modes of operation is of paramount importance. Efficiency directly affects battery life and the duration of usable operation. The input voltages for battery-powered systems range anywhere from 1.8V to 5.5V. The most common sources of power are either 2 AA or single Li-Ion cell batteries whose voltage ranges from 3V to 4.2V. Operating currents are typically less than 1.5A, with most applications requiring less than 600 mA. Although there are general guidelines for using the right step-down solution for powering FPGAs (See Power Designer #102[1]), portable devices mandate that high efficiency be maintained even during standby to extend battery life.

For portable systems, the synchronous buck DC-DC converter is the ideal solution for powering the FPGAs even at lower load currents. But in an ordinary DC-DC converter the efficiency at light loads suffers greatly. This is not important if the load is either "full power" or completely off, since

the converter can be disabled. But when powering an FPGA which has power-on standby states, the converter needlessly dissipates power by continuing to switch at the same high frequency required to produce maximum power. In portable systems, it is important to use a converter that transitions to a pulse-skipping or Pulse Frequency Modulation (PFM) scheme.

A typical fixed frequency synchronous step-down converter always runs at a fixed frequency in a continuous conduction mode, whereas a converter in PFM mode transitions to a variable frequency, fixed on-time operation as the load current decreases, and operates in a discontinuous mode to reduce switching losses.

Internal to such a converter is a comparator that samples the output voltage V_O at a fixed frequency f_{PFM} and compares it to a reference voltage V_{REF}. When V_O is less than V_{REF}, the converter generates a fixed on-time pulse through the PWM to charge the output capacitor.
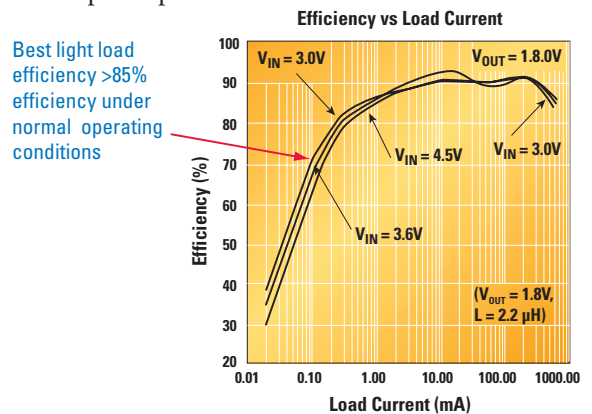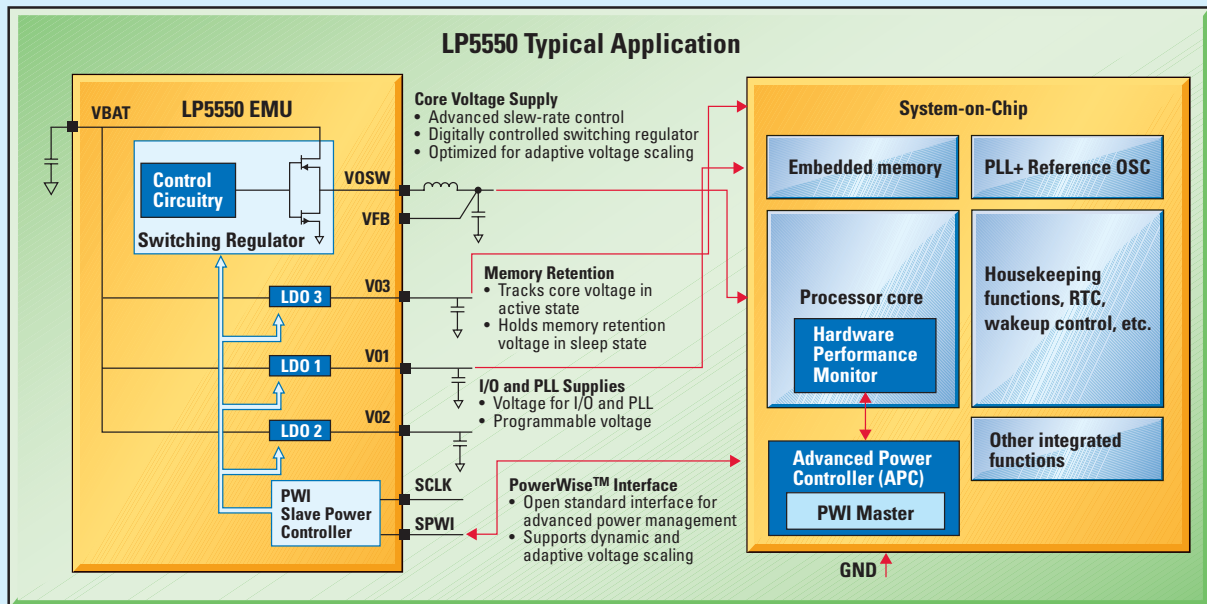

Efficiency vs Load Current

Best light load efficiency >85% efficiency under normal operating conditions

Figure 1. Plot from Device with PFM Shows High Efficiency Across All Loads

PFM operation continues until the output current rises above a certain threshold, at which point normal PWM operation is resumed. There are two main advantages of PFM operation at light loads. One is that the supply current of the DC-DC converter is greatly reduced as much of the internal circuitry is turned off during PFM. Another is that the switching losses of the output stage are minimized because it switches only when required. *(see Figure 1)*

[1] See Power Designer #102 at power.national.com/designer

PWI 1.0-Compliant Energy Management Unit for PowerWise™ Adaptive Voltage Scaling

LP5550 Digitally Controlled PowerWise™ Energy Management Unit for Reducing Processor Power Consumption

LP5550 Typical Application

LP5550 EMU

VBAT

Control Circuitry

Switching Regulator

VOSW
VFB

LDO 3 — V03
LDO 1 — V01
LDO 2 — V02

PWI Slave Power Controller

SCLK
SPWI

Core Voltage Supply
• Advanced slew-rate control
• Digitally controlled switching regulator
• Optimized for adaptive voltage scaling

Memory Retention
• Tracks core voltage in active state
• Holds memory retention voltage in sleep state

I/O and PLL Supplies
• Voltage for I/O and PLL
• Programmable voltage

PowerWise™ Interface
• Open standard interface for advanced power management
• Supports dynamic and adaptive voltage scaling

System-on-Chip

Embedded memory

PLL+ Reference OSC

Processor core

Hardware Performance Monitor

Housekeeping functions, RTC, wakeup control, etc.

Advanced Power Controller (APC)

PWI Master

Other integrated functions

GND

LP5550 Features

- High-efficiency PowerWise™ energy management unit (EMU) for adaptive voltage scaling (AVS)
- Compatible with National's PowerWise advanced power controller technology for minimizing processor power consumption
- PWI 1.0 open standard interface compatible
- Reduces power consumption of digital processors by up to 70%
- 3 Programmable LDOs for I/O, PLL, and memory retention supply generation
- Available in an LLP-16 package

AVAILABLE LEAD-FREE

Ideal for use in cellular handsets, handheld radios, cameras, PDAs, battery-powered devices, and portable instruments supplies

Product Highlight:

Digitally-controlled LP5550 reduces power consumption of processors and extends battery life of handheld consumer products

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Advanced Topics in Powering FPGAs

The FPGA power designer should choose the power management IC that allows efficient operation in both full load and light load operation. In addition to this, a part with a low quiescent current should be chosen to minimize power loss during standby modes.

Monotonic Rise of Core Voltage

Several FPGAs, ASIC cores, and even processors retain some voltage potential in shutdown. This gives rise to a pre-biased condition where the power converter starts up into this voltage. Pre-biasing can cause initial undesirable changes in the voltage of a converter that is not designed to handle such a load. In particular, it is undesirable for the pre-existing voltage to cause the output voltage of the converter to droop during turn on. The power supply voltage must rise steadily and gradually until eventually stabilizing at its nominal value. This is called a monotonic voltage rise and is necessary for the internal elements in the FPGA to turn on properly. As these elements are turning on during the ramp-up period, the "load" to the power supply will not be constant, so it is important that the converter chosen regulates its output voltage not only during the steady state but also during ramp up. There are two approaches to ensuring a monotonic rise of the voltage.

• One is to increase the bulk capacitance of the converter sufficiently to hold enough charge on the output so that the voltage does not droop during turn on. The additional bulk capacitors in this approach increase both the cost and the footprint.
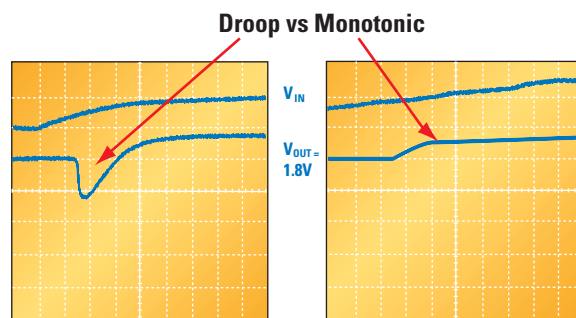
Figure 2.
Comparing Non-Monotonic Rise vs Monotonic Rise

• Another approach is to disable the low-side MOSFET of the synchronous converter and monitor the switching node voltage during the off-time of the high-side MOSFET. The IC remains in pre-biased mode until it detects that the switch node (the point at which the output inductor is connected to the two MOSFETs) stays below 0V during the entire high-side MOSFET's off-time. Once this condition is detected, the low-side MOSFET is allowed to start switching.

Figure 3 shows the switch node as well as the high-side and low-side gate signals during pre-biased startup in a typical synchronous converter. The pre-biased output voltage should not exceed the sum of the supply and gate threshold voltages of the high-side MOSFET to ensure that this device is able to switch during startup.
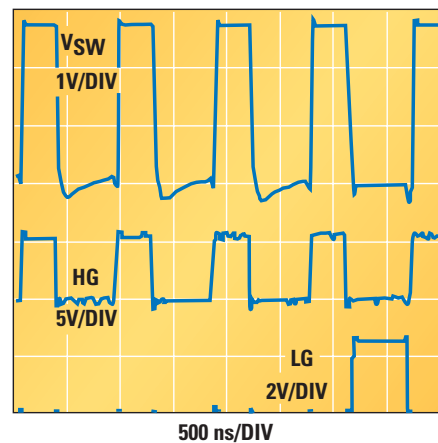

Figure 3.
Switching Waveforms During Monotonic Rise of Outputs

Voltage Scaling to Improve Efficiency

FPGAs are essentially CMOS devices, which scale with advances in process technology. As device geometries scale below 90 nm and operating frequencies increase, both dynamic and static power consumption become more important. Current approaches to FPGA design do not allow for easy reduction of dynamic or static power, although possible theoretically.

SOT-23 Synchronous Constant-on-Time Switching Controller

High-Efficiency LM1770 Synchronous Controller for Low-Voltage DC-DC Conversion
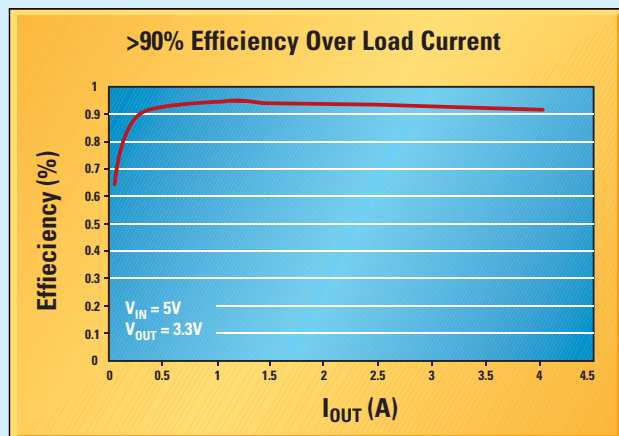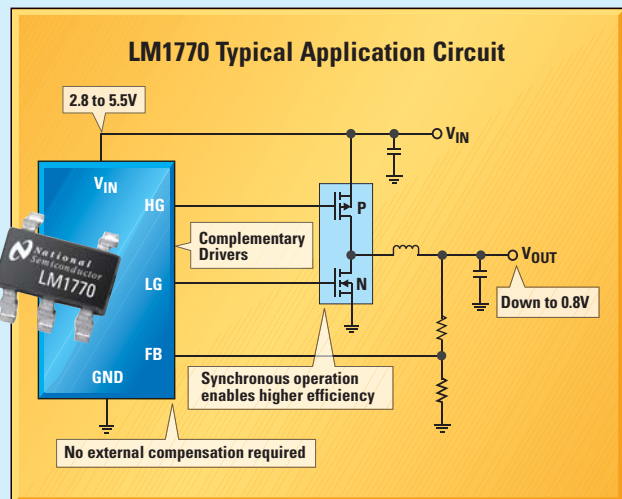
LM1770 Features

- Adaptive On-Time Control topology requires no compensation components

- Synchronous operation: High-side PFET and low-side NFET enables higher-efficiency and reduced power-dissipation

- Fast-transient response allows for lower values of capacitors

- Low input voltage of 2.8V to 5.5V; Ideal for point-of-load applications

- Three versions of adaptive on-time allows for selection of operating frequency

- Available in SOT23-5 packaging for space-constrained applications

AVAILABLE LEAD-FREE

Ideal for point of load regulation in consumer applications, set-top boxes, cable modems, digital video recorders, printers, servers, and point-of-sale terminals

Product Highlight:

Simplest synchronous controller for up to 5A digital loads

LM1770 Typical Application Circuit

2.8 to 5.5V

V_{IN}

V_{IN}

HG

LG

FB

GND

Complementary Drivers

P

N

V_{OUT}

Down to 0.8V

Synchronous operation enables higher efficiency

No external compensation required

>90% Efficiency Over Load Current

Effieciency (%)

1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

V_{IN} = 5V
V_{OUT} = 3.3V

0   0.5   1   1.5   2   2.5   3   3.5   4   4.5

I_{OUT} (A)

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Advanced Topics in Powering FPGAs

Dynamic power can be expressed in terms of switching FPGA activity N, capacitance C, frequency f and supply voltage V_{DD}

$$P_{DYNAMIC} = \frac{1}{2} \; N.C.f.V_{DD}^2$$

The static or leakage power consumption is due to sub-threshold leakage current I_{sub}, drain-body junction leakage current I_j, and source-body junction leakage current I_b, and is given by

$$P_{STATIC} = V_{DD}I_{sub} + |V_{bs}|(I_j + I_b)$$

where V_{bs} is the body bias voltage.

Manufacturers of portable power systems have realized that the desired small size and long run time requirements of their equipment cannot be met by increasing the energy density of batteries or improving the power delivery efficiency. For such advanced systems, "Dynamic or Adaptive Voltage Scaling" and "Back Biasing" are essential to reduce processor power. The core concept is derived from the equations presented above. The way to reduce dynamic power consumption in a processor is not only to lower the clock frequency as much as possible, but to also reduce the core supply voltage to the minimum value for a given clock frequency. This open-loop technique is called Dynamic Voltage Scaling (DVS). Adaptive Voltage Scaling (AVS) is a closed-loop control technique, which provides substantial improvement to Dynamic Voltage Scaling (DVS). AVS simplifies voltage scaling by inherently compensating for process and temperature variations and eliminating the need for a frequency vs supply voltage table used in DVS. The FPGA or digital processor uses a hardware performance monitor that communicates with the power controller through an open-industry standard PowerWise™ Interface (PWI) and operates at an absolute minimum supply voltage over all operating frequencies. *Figure 4* shows an implementation of advanced voltage scaling.

Back biasing a circuit such as one in *Figure 5* applies -0.8V to -1.5V to the body of the devices, increasing the threshold of the devices and reducing the sub-threshold leakage, thus lowering static power consumption.
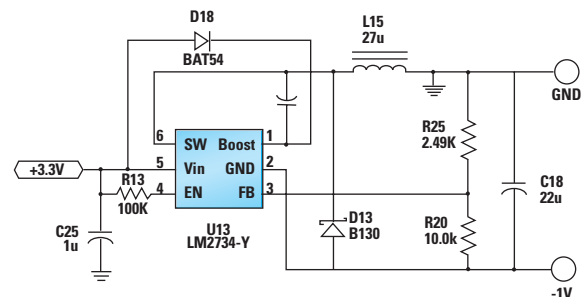
Figure 5. Circuit that Generates a Negative Voltage to Back Bias FPGAs

Conclusion

FPGAs are proliferating rapidly into portable devices. Beyond the basic issues of correctly powering FPGAs, efficiency and battery life also need to be considered. Typically, step-down regulators with provision for high light-load efficiency are best for powering these FPGAs in portable systems. To further improve efficiency significantly, techniques such as adaptive voltage scaling should be implemented. As devices scale downward of 90 nm, managing static power becomes equally important due to the rise in leakage currents in the ICs. The use of innovative back-biasing power management ICs is suggested to reduce sub-threshold leakage and static power. Furthermore, pre-biased loads may exist on the FPGAs during start-up. To ensure monotonic rise of the core voltage is important for their proper functioning, power management ICs that start-up properly into pre-biased loads should be used. ∎

**Figure 4. Implementing Advanced Voltage Scaling**

Power Design Tools
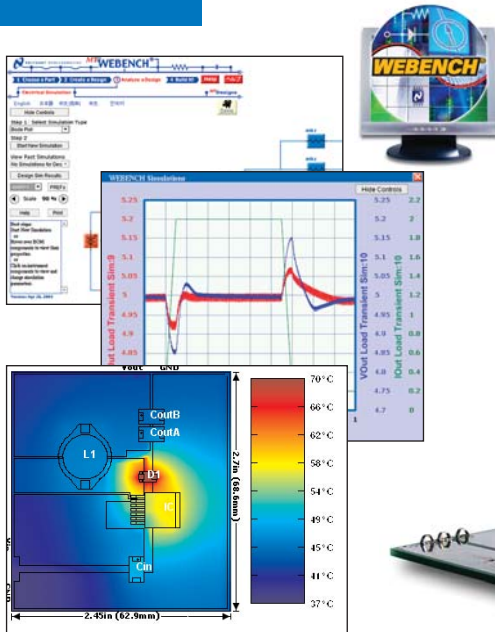
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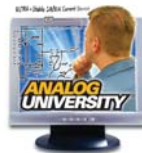
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