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Application Report
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Thermal Comparison of FR-4 and Insulated Metal Substrate PCB for GaN Inverter

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ABSTRACT

Thermal performance or the ability to efficiently transfer heat from the heat sources like power semiconductor devices to the ambient plays a critical role in determining the size and reliability of power electronic systems. Conventional heat dissipation systems rarely involve PCBs in the major heat dissipation path. However, technological changes like SMD packages for power devices to enable size reduction in power electronic systems have resulted in PCBs being increasingly used in the major heat dissipation path. Therefore the selection of an appropriate PCB material is no longer trivial and involves detailed thermal analysis. This application report compares the thermal performance between FR-4 (NEMA grade designation for glass-reinforced epoxy laminate material) and Insulated Metal Substrate (IMS) PCB in a three-phase GaN inverter for motor drives and helps engineers make an informed choice on the most suitable PCB design for a given application.

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1 Introduction

Semiconductor device packages continue to develop and evolve over time – the major driving factors behind package choices are cost, footprint, height, thermal performance, lead inductance, ease of assembly, and so forth. Increasingly, power semiconductor devices are manufactured in surface-mount packages like D2PAK, QFN to benefit from smaller footprint and lower parasitic inductance. Surface mount devices (SMD) can be either top or bottom cooled – bottom-cooled devices are predominant due to ease of manufacturing. Heat generated due to losses in bottom-cooled SMDs is typically conducted to the ambient via a heat sink mounted under the PCB as Figure 1 shows. Figure 1 also shows that the PCB is in the major heat transfer path from device to ambient and plays a critical role in the power capability and reliability of the system.

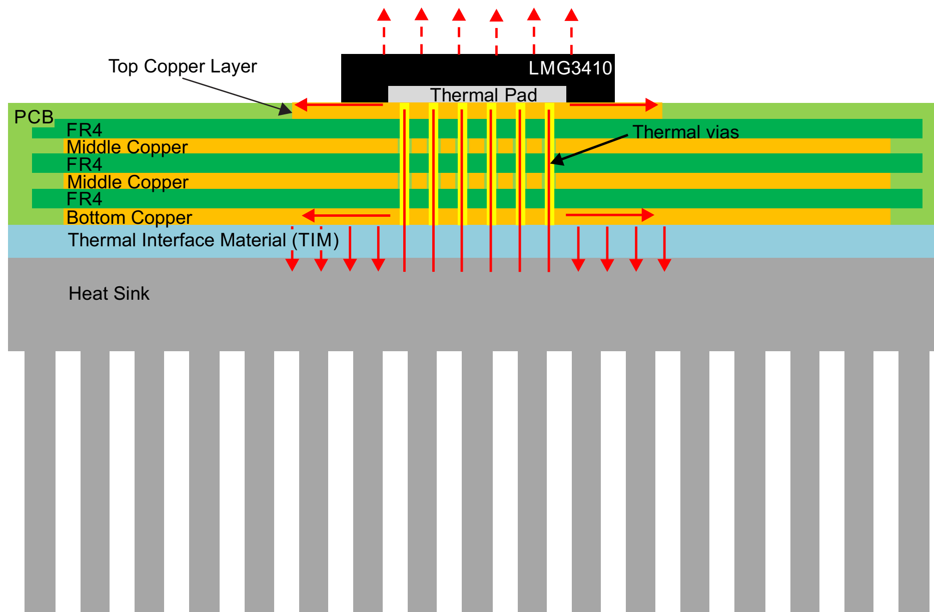

Figure 1. Bottom-Cooled SMD Package With Heat Sink Mounted Under PCB

The device junction-to-ambient thermal resistance ($R_{\theta JA}$) is given by Equation 1,

$$R_{\theta JA} = R_{\theta JC(bottom)} + R_{PCB} + R_{TIM} + R_{Heat\ Sink} \tag{1}$$

where

- $R_{\theta JC(bottom)}$ is the thermal resistance between the junction and the bottom of the case
- R_{PCB} is the thermal resistance of the PCB
- R_{TIM} is the thermal resistance of the Thermal Interface Material (TIM)
- $R_{Heat\ Sink}$ is the thermal resistance of the heat sink

Note that in Equation 1, the thermal resistance from junction-to-ambient via the top of the case is ignored since it is much higher than thermal resistance from the junction-to-ambient via the bottom of the case.

The thermal resistance of the PCB, R_{PCB}, depends on a multitude of factors including number of layers, copper pour thickness, number and size of thermal vias, dielectric material and its layer thickness, use of metal substrate, and so forth. Thus, the thermal design of the PCB is an involved process with many options available to designers at varied cost and performance. This application report documents the thermal performance of two different PCB designs – FR-4 PCB and IMS PCB, for a three-phase GaN inverter deploying the LMG3410R050 GaN device from TI.

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2 Three-Phase GaN Inverter

For the purposes of this study, a three-phase GaN inverter, driving a motor, was used to evaluate the thermal performance of FR-4 and IMS PCBs. Figure 2 shows the schematic of the test set-up used.

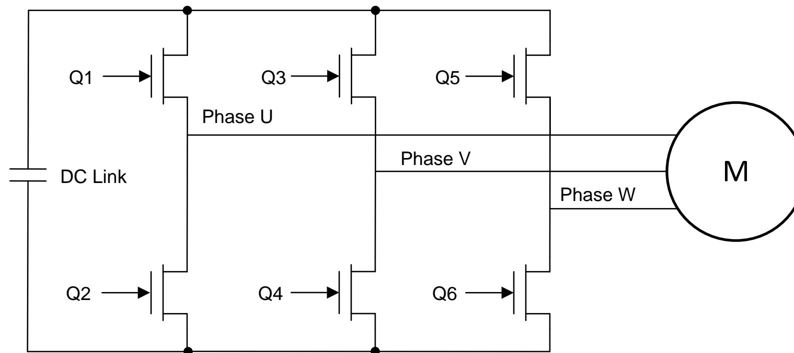

Figure 2. Test Setup

The power semiconductor devices (Q1–Q6 in Figure 2) used in this study are the LMG3410R050 TI GaN devices. These devices use a flat 32-pin QFN package in a compact 8-mm × 8-mm form factor. The bottom side of the device has a large thermal pad (highlighted in yellow in Figure 3) for heat dissipation through the PCB. The thermal pad is tied to the source pin of the device. Bottom-cooled SMD packages such as the one in the LMG3410R050 devices use the PCB in the major heat dissipation path and therefore need a detailed thermal PCB design for optimal performance. In this report, Q1, Q3, and Q5 are referred to as top-side FETs while Q2, Q4, and Q6 are referred to as bottom-side FETs (as in Figure 2).

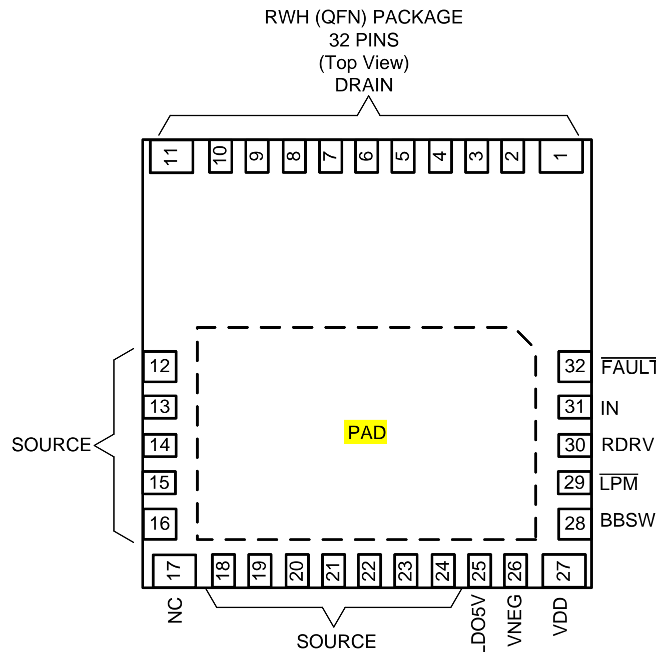

Figure 3. LMG3410R050 QFN Package

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3 PCB Structure and Thermal System Overview

PCB Layer Stack-up

An FR-4 PCB and an IMS PCB were fabricated for this study. Both the boards consist of 2 layers and there are minor variations in the PCB layout as described in the following sections. Figure 4 shows the layer stack-up of the 2 PCBs.

As Figure 4 illustrates, the total thickness of FR-4 PCB is 0.84 mm and that of IMS PCB is 1.95 mm. The thickness of FR-4 PCBs, generally, is 1.6 mm – in this study, a thinner 0.84-mm FR-4 PCB is used to reduce the PCB thermal resistance at the cost of lower mechanical strength. Thermal conductivity of the dielectric layers in IMS PCB is 3 W / m-K.

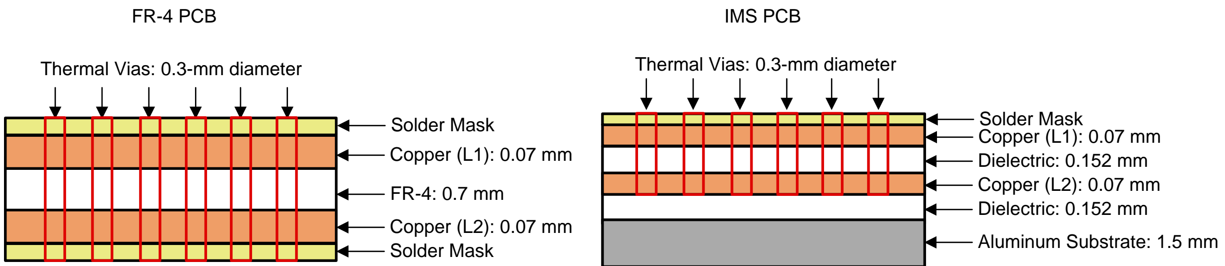

Figure 4. Layer Stack-Up Cross Section of FR-4 and IMS PCBs

Thermal Vias

Figure 5 illustrates how thermal vias are provided in thermal pad of GaN FETs to reduce PCB thermal resistance. Top-side FETs (Q1 in Figure 5) in both the boards have 33 thermal vias. Bottom-side FETs (Q2 in Figure 5) in the IMS PCB have 36 thermal vias and in FR-4 PCB have 61 thermal vias.

In top-side FETs (Q1 in Figure 5), electrical net clearance and loop inductance restrictions resulted in reduced vias - DC Bus Return net in the bottom layer needs clearance from the Phase Node net vias and hence the entire thermal pad could not be used for thermal vias. Thermal vias in top-side FETs can be increased by shifting the DC Bus Return plane to the left but this increases the loop inductance and subsequently the voltage ringing during turnoff. So, an optimal layout must be designed to balance between loop inductance and thermal performance. Thermal vias in bottom-side FETs in IMS PCBs were reduced for manufacturability.

The hole diameter of all the thermal vias is 0.3 mm. The plating thickness is 0.02 mm in FR-4 PCB and 0.033 mm in IMS PCB.

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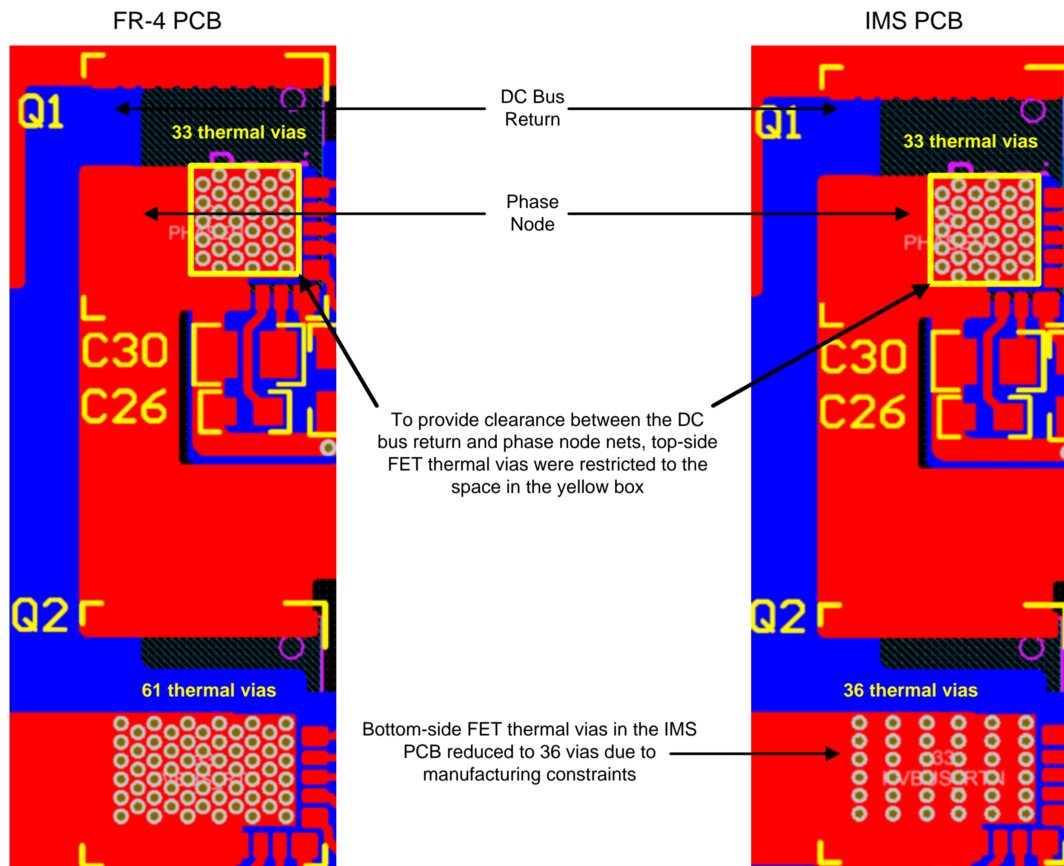

Figure 5. Thermal Vias

Mounting Holes

As Figure 6 illustrates, nine mounting holes (circled in red) are available in both PCBs to mount on to a heat sink through a Thermal Interface Material (TIM). Due to high voltage nets and form factor constraints, mounting holes are not spread symmetrically across the PCB. Bottom-side FETs have more mounting holes in the vicinity than top-side FETs. This reduces the mounting screw downforce and therefore increases the thermal resistance of top-side FETs to the ambient in comparison with thermal resistance of bottom-side FETs to the ambient. This effect is more pronounced in the thin FR-4 PCB than the IMS PCB.

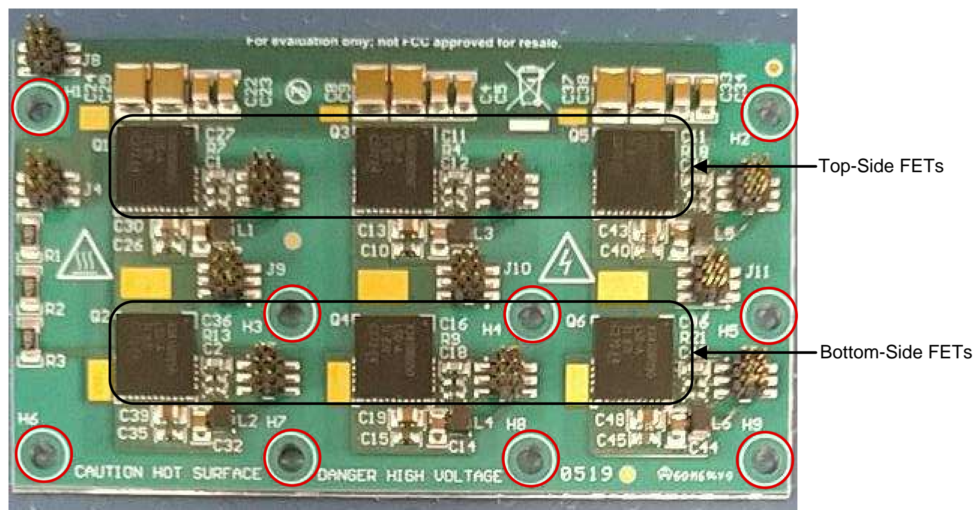

Figure 6. Mounting Holes

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Thermal Interface Material (TIM) and Heat Sink

TIM is used between the PCB and heat sink to ensure uniform contact for better heat transfer. In the absence of TIM, surface roughness results in poor contact and air gaps leading to inefficient heat transfer. Thus, TIM plays a critical role in the efficiency of heat transfer. In this study, a phase change material with a thickness of 0.1 mm and thermal conductivity of 1.6 W / m-K was used as TIM for FR-4 and IMS PCBs. Phase-change materials have higher thermal conductivity but need sufficient clamping downforce for proper operation. However, in the case of the FR-4 PCB, the asymmetric distribution of mounting holes and lower mechanical strength due to lesser thickness (0.84 mm) resulted in the top side of the FR-4 PCB making poor contact with the heat sink, as Figure 7 shows.

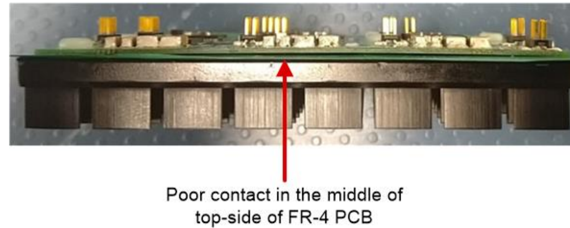

Figure 7. FR-4 PCB Poor Contact With Phase Change TIM

Hence, instead of phase change TIM, an adhesive based TIM with a thickness of 0.25 mm and thermal conductivity of 0.6 W / m-K was used with the FR-4 PCB. Adhesive-based TIMs have lower thermal conductivity but ensure better contact than phase-change TIMs in such cases without sufficient clamping downforce. IMS PCB was tested with phase change material – the 1.5-mm aluminum substrate layer provides sufficient mechanical strength for firm, uniform contact even with asymmetric mounting holes as Figure 8 shows.

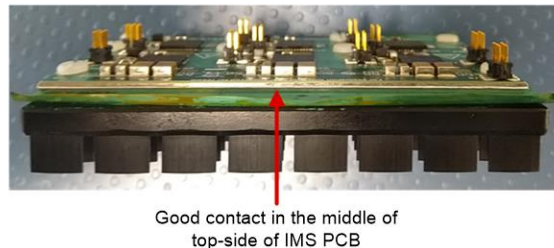

Figure 8. IMS PCB Good Contact With Phase Change TIM

An anodized aluminum heat sink with a natural convection (fan-less) thermal resistance of 5.3°C / W was used with FR-4 and IMS PCBs.

Junction-to-Ambient Thermal Resistance Estimation

Figure 9 shows the cross-section of major heat dissipation path in this study. Note that the study was conducted without any fan or forced air flow – heat transfer to ambient was only through natural convection.

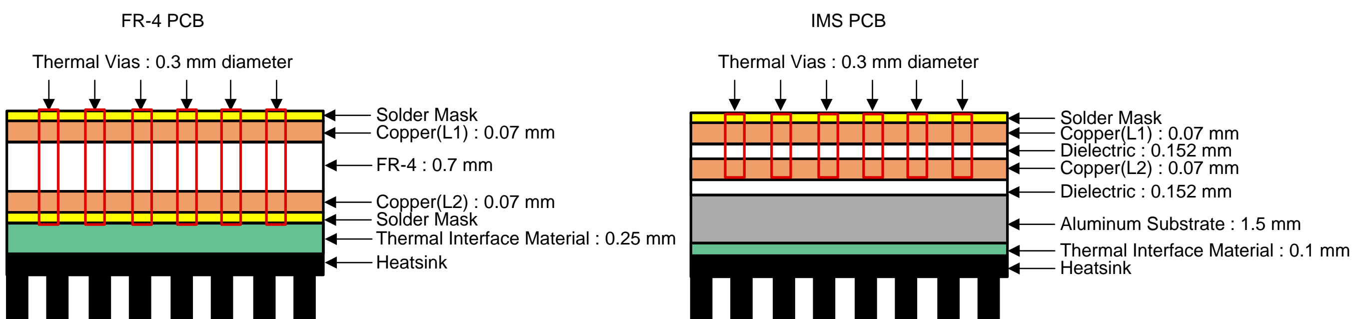

Figure 9. Cross-Section of Major Heat-Dissipation Path

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Table 1 lists the major thermal resistance components in the heat-dissipation path.

Table 1. Thermal Resistance Estimation

Thermal Resistance(°C/W)	FR-4 PCB		IMS PCB	
	Top- Side FET	Bottom-Side FET	Top-Side FET	Bottom-Side FET
Junction to case ($R_{\theta JC}$)	0.5	0.5	0.5	0.5
PCB thermal vias (R_{VIAS})	3.76	2.03	0.83	0.76
Dielectric ($R_{dielectric}$)	N/A	N/A	3.1	2.08
Aluminum (R_{AL})	N/A	N/A	0.3	0.3
TIM (R_{TIM})	25.5	17.13	2.57	2.57
Heat Sink ($R_{Heat\ Sink}$)	31.8	31.8	31.8	31.8
Junction to ambient ($R_{\theta JA}$)	**61.56**	**51.46**	**39.1**	**38.01**

Observe the following important details:

- Thermal vias play a critical role in reducing the thermal resistance of PCBs, especially FR-4. FR-4 has a poor thermal conductivity of 0.25 W / m-K; the thermal insulance factor of a 0.7-mm FR-4 layer is 2040°C-mm^2 / W. In the IMS PCB, the thermal insulance factor of a 0.152-mm dielectric layer of thermal conductivity 3 W / m-K is 50°C-mm^2 / W. Reducing the FR-4 layer thickness below a certain level is not possible due to the reduction in mechanical strength. Therefore, vias are critical for reducing PCB thermal resistance by providing a lower thermal resistance path that largely bypasses the high thermal-resistance dielectric materials like FR-4 as Figure 9 shows. R_{VIAS} is higher in the FR-4 PCB than IMS PCB due to the longer length and smaller plating thickness of the vias.
- The thermal resistance of the PCB (R_{PCB}) is R_{VIAS} + $R_{dielectric}$+ R_{AL}. The IMS PCB has a slightly higher thermal resistance (4.23°C / W for top-side FET) than FR-4 PCB (3.76°C / W for top-side FET). This counterintuitive result is due to the thin FR-4 PCB and the thicker-than-necessary bottom layer dielectric in the IMS PCB. The bottom-layer dielectric thickness can be as low as 0.075 mm for the electrical isolation required. In this case – 0.152 mm was used due to ease of availability. If 0.075 mm is used, R_{PCB} reduces to 2.65°C / W for top-side FET in IMS PCB. Also, the thermal resistance of the first dielectric layer is neglected to simplify calculations – this further reduces R_{PCB} in IMS in parallel with R_{VIAS}.
- R_{TIM} is different for top- and bottom-side FETs in FR-4 PCB due to the difference in the bottom-layer pad area - see Figure 10. In the IMS PCB, the aluminum layer acts as a good heat spreader and therefore R_{TIM} is the same for top- and bottom-side FETs. Also, note that in the IMS PCB, thermal grease can be used as TIM instead of phase-change material – grease has even better thermal properties than phase-change TIM and the isolated aluminum layer enables the use of grease which is not possible in the FR-4 PCB.

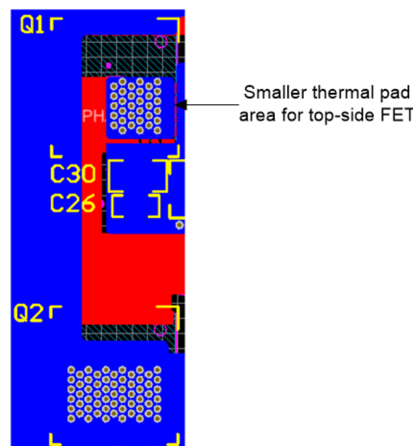

Figure 10. Bottom Layer Pad Area in FR-4 PCB

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- $R_{Heat\ Sink}$ is the equivalent thermal resistance of heat sink per FET – natural convection thermal resistance from the heat sink data sheet is multiplied by 6 (the number of FETs) to obtain $R_{Heat\ Sink}$. Clearly, $R_{Heat\ Sink}$ dominates the overall $R_{\theta JA}$ – in natural convection cooling, the heat sink plays a more critical role than R_{PCB} in deciding power capability. Also, note that this is a pessimistic estimate since the data sheet thermal resistance value is based on the point source of heat while in this study, heat sources (FETs) are distributed.
- $R_{\theta JA}$ is much higher in the FR-4 PCB (61.56°C / W for top-side FET) than in the IMS PCB (39.1°C / W for top-side FET). The key difference is in the TIM - it is to be noted that the adhesive TIM is used for the FR-4 PCB due to the lower mechanical strength. A different adhesive TIM with lower thickness and higher thermal conductivity can help reduce R_{TIM} in the case of this thin FR-4 PCB.
- Also, a thicker FR-4 PCB helps reduce $R_{\theta JA}$ by ensuring firm, uniform contact with the heat sink. This comes at the cost of higher R_{VIAS} due to thicker PCB – this increase in R_{VIAS} can be offset by a reduction in R_{TIM} by using phase change TIM instead of adhesive TIM.

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4 Test Results

The FR-4 and IMS PCBs delivered a continuous current of 3-A RMS to drive a 200-V, three-phase motor. The operating conditions were maintained until the temperatures attained steady state values. Figure 11 shows the thermal images of the top-side FETs and Figure 12 shows the bottom-side FETs.

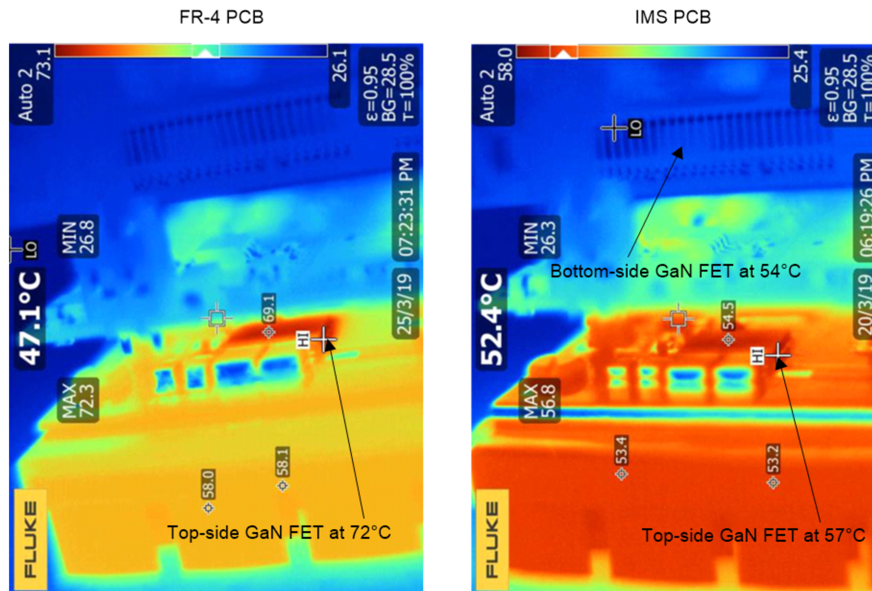

Figure 11. Thermal Images of Top-Side GaN FETs

The rise in the case temperature in the FR-4 and IMS PCBs are 47°C and 32°C, respectively, at an ambient temperature of 25°C. The ratio of these temperature rise values compares well with the ratio of $R_{\theta JA}$ for the top-side FET in the FR-4 (61.56°C/W) and the IMS (39.1°C/W) PCBs. This agrees with the fact that the GaN losses in either case are similar – switching losses are same and the increase in $R_{DS(on)}$ with temperature does not significantly increase the conduction losses in this study.

Similar observations can be made about the bottom-side FETs from Figure 12. The case temperature rise is 36°C and 29°C in the FR-4 and the IMS PCB, respectively. This matches with the ratio of $R_{\theta JA}$ for bottom-side FETs.

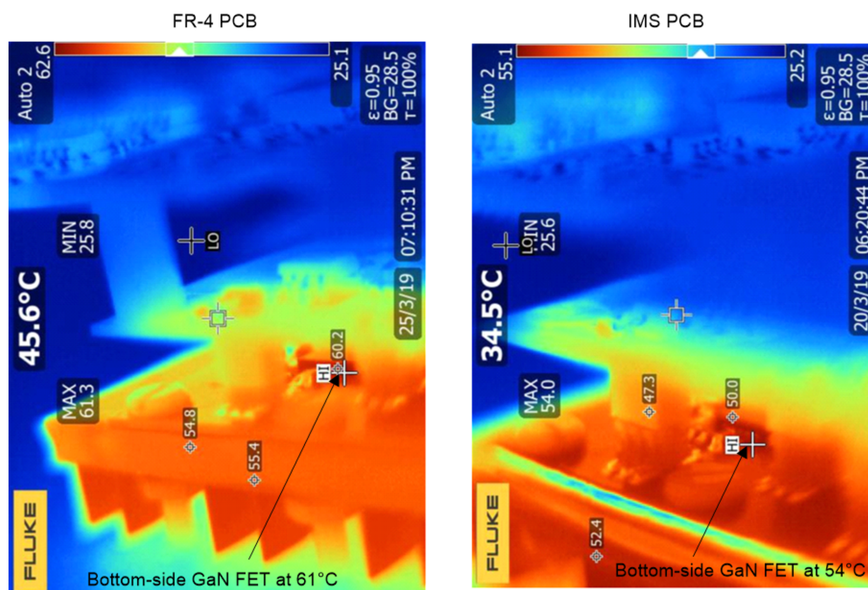

Figure 12. Thermal Images of Bottom-Side GaN FETs

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5 Conclusions

This study shows that the FR-4 PCB has a 45% higher average $R_{\theta JA}$ compared to the IMS PCB. The main difference is in the choice of the TIM that was mandated due to the lower mechanical strength of the thin FR-4 PCB. A more optimal FR-4 PCB-based solution might be a 1.6-mm PCB with a phase-change TIM to enable a lower $R_{\theta JA}$ for the FR-4 PCB than calculated in this study – such a system may have an $R_{\theta JA}$ that is only 15–20% higher than the IMS PCB instead of 45% as this study shows. Choose a suitable PCB thickness to optimize between the required mechanical strength and R_{VIAS} in the FR-4 PCBs.

Phase-change TIMs provide superior thermal performance compared to adhesive TIMs and the PCB designer should ensure sufficient clamping downforce using a suitable mounting mechanism to enable the use of phase-change TIM with the FR-4 PCBs – use of adhesive TIM can be a major roadblock to achieving necessary thermal performance. The IMS PCBs can also work with thermal grease which has better thermal performance than even phase-change TIM.

The IMS PCBs come at a higher cost but provide a significant advantage over the FR-4 PCBs in high-power, high-density applications with forced-air or liquid cooling or in applications with high ambient temperature requirements and small temperature margins. In natural-convection-cooled systems with sufficient temperature margins, FR-4 PCBs can deliver acceptable performance compared to IMS PCBs, provided the PCB designer makes optimal decisions on the FR-4 thickness, TIM material, and symmetric mounting mechanisms as explained in this study.

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