Application Report
SPRABU8–May 2014

AM335x Power Estimation Tool

ABSTRACT

The Power Estimation Tool (PET) allows you to gain insight into the power consumption of select Sitara processors. The tool includes the ability for you to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

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Trademarks

1 Introduction

PET is comprised of three modules:

1. Input Spreadsheet – Downloadable spreadsheet in which users input device parameters needed for their application. Parameters include IP activities and loadings, desired power states, and power management usages. For advanced users, multiple operating conditions can be applied along with time slots for each state.
2. Spreadsheet Upload – Upon completion of the input spreadsheet, you can then upload the spreadsheet to TI for the power consumption analysis. Registration and legal agreement acceptance is required for the upload.
3. Power Analysis Report – Contains the information on power consumption based on the spreadsheet upload. The report that includes leakage, active and total average power, as well as power management voltages, will be sent to you via email.

NOTE: The AM335x PET applies to AM3352, AM3354, AM3356, AM3357, AM3358 and AM3359 devices.

2 Input Spreadsheet

Download AM335x PET Input Spreadsheet here. There are two types of input spreadsheets: the Simplified input spreadsheet is designed for estimating the power for a single application scenario and the Advanced input spreadsheet has additional columns (slots) for multiple application scenarios. The power estimates from the Advanced spreadsheet will be an average power of the multiple application scenarios (slots) configured in the input spreadsheet.

The input spreadsheet consists of four sections: High-Level System Configuration, Processors, Peripherals, and Analog Modules. To use the input spreadsheet, modify the input fields with their appropriate usage parameters. Cells that are designed for user input are light green in color. Simply configure the light green cells to a value most closely aligned with your intended scenario.

Briefly, the purpose of each of the four sections is:

- Section A: configure the high-level system configuration such as junction temperature and power estimation mode
- Section B: configure processor subsystem components
- Section C: configure peripherals
- Section D: configure analog modules

2.1 Macro Buttons

The spreadsheet includes macros. If you can not run macros, review your excel security settings described in the following articles:

Change macro security settings in Excel (Office 2007)

Enable macros to run (Office 2003).

The input spreadsheet has command buttons to run macros as shown in Figure 1.

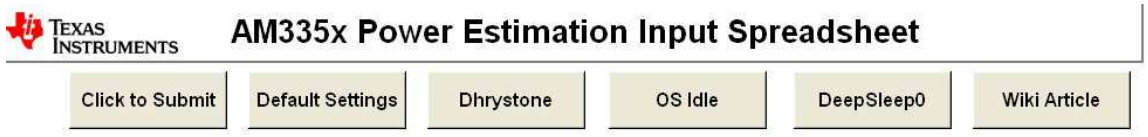

Figure 1. Macro Buttons

- "Click to Submit" - Navigate to PET spreadsheet upload page.
- "Default Settings" - Clear all settings and configure them to the default values.
- "Dhrystone" - Configure settings to the Dhrystone benchmark example application scenario. [MPU intensive, high power use case]

- "OS Idle" - Configure settings to Linux OS Idle example application scenario. [MPU idle, medium power use case]
- "DeepSleep0" - Configure settings to DS0 example application scenario. [MPU off, low power use case]
- "Wiki Article" - Navigate to this wiki article.

2.2 Section A: High-Level System Configuration

This section allows you to select the device revision, choose DDR type and loading, set a junction temperature (not ambient temperature) between 0°C and 105°C, power estimation mode, SmartReflex AVS (Adaptive Voltage Scaling) and Dual-Voltage I/O VDDSHVx voltages as shown in Table 1.

Table 1. Section A of AM335x PET Input Spreadsheet [1] [2]

Device Revision	PG2.1
DDR Type	DDR3
DDR Loading	1
Junction Temperature (°C)	25
Power Estimation Mode	Typ
Smart Reflex	off
VDDSHV1 Voltage (V)	1.8
VDDSHV2 Voltage (V)	1.8
VDDSHV3 Voltage (V)	1.8
VDDSHV4 Voltage (V)	1.8
VDDSHV5 Voltage (V)	1.8
VDDSH61 Voltage (V)	1.8
Power Mode	Active
Dynamic Power Switching	Off

(1) MAX: Worst case power consumption

(2) TYP: Typical case power consumption

- Device Revision: PG2.1, PG1.0 (evaluate PG2.1)
- DDR Type: mDDR, DDR2, DDR3, DDR3L,None
- DDR Loading: 0, 1, 2 (corresponds to the number of DDR devices in the system)
- Junction Temperature (°C): 0 ~ 105 (negative values are not supported in the tool)
- Power Estimation Mode: Max, Typ ('Max' accounts for the worst-case silicon process variation)
- SmartReflex: On, Off
- VDDSHVx Voltage [V]: 1.8 or 3.3
- Power Mode: Active, Standby, DeepSleep1, DeepSleep0, RTC Only
- Dynamic Power Switching: On, Off (currently only supported for PD_GFX)

Table 2. Typical Power Modes

Power Modes	Application State	Power Domains, Clocks, and Voltage Supply States
Active	All Features	**Power supplies**: All power supplies are ON. VDD_MPU = 1.1 V (nom) VDD_CORE = 1.1 V (nom) **Clocks**: Main Oscillator (OSC0) = ON All DPLLs are locked. **Power domains**: PD_PER = ON PD_MPU = ON PD = GFX = ON or OFF (depending on use case) PD_WKUP = ON DDR is active
Standby	DDR memory is in self-refresh and contents are preserved. Wakeup from any GPIO. Cortex™-A8 context and register contents are lost and must be saved before entering standby. On exit, context must be restored from DDR. For wakeup, boot ROM executes and branches to system resume.	**Power supplies**: All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) **Clocks**: Main Oscillator (OSC0) = ON All DPLLs are in bypass. **Power domains**: PD_PER = ON PD_MPU = OFF PD = GFX = OFF PD_WKUP = ON DDR is in self-refresh.
Deepsleep1	On-chip peripheral registers are preserved. Cortex-A8 context/registers are lost, so the application needs to save them to the L3 OCMC RAM or DDR before entering DeepSleep. DDR is in self-refresh. For wakeup, boot ROM executes and branches to system resume.	**Power supplies**: All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) **Clocks**: Main Oscillator (OSC0) = OFF All DPLLs are in bypass. **Power domains**: PD_PER = ON PD_MPU = OFF PD = GFX = OFF PD_WKUP = ON DDR is in self-refresh.
Deepsleep0	PD_PER peripheral and Cortex-A8/MPU register information will be lost. On-chip peripheral register (context) information of PD-PER domain needs to be saved by application to SDRAM before entering this mode. DDR is in self-refresh. For wakeup, boot ROM executes and branches to peripheral context restore followed by system resume.	**Power supplies**: All power supplies are ON. VDD_MPU = 0.95 V (nom) VDD_CORE = 0.95 V (nom) **Clocks**: Main Oscillator (OSC0) = OFF All DPLLs are in bypass. **Power domains**: PD_PER = ON PD_MPU = OFF PD = GFX = OFF PD_WKUP = ON DDR is in self-refresh.
RTC-Only	RTC timer remains active and all other device functionality is disabled.	**Power supplies**: All power supplies are OFF except. VDDS_RTC, VDD_MPU = 0 V VDD_CORE = 0 V **Clocks**: Main Oscillator (OSC0) = OFF **Power domains**: All power domains are OFF.

The spreadsheet presents information only for the full-featured devices in the AM335x family. However, since the spreadsheet breaks out the power consumption due to each module in the full-featured device, estimates for the other devices in the AM335x family can be obtained by setting zero for the modules not present in the device under consideration. This ensures that active power from the non-applicable modules are not included in the power tally. The device differences are summarized at the overview section in AM335x Device Evaluation Wiki.

2.3 Section B: Processors

This section allows you to set an operating performance point (OPP) for MPU domain and CORE domain, MPU utilization and SGX utilization as shown in Table 3.

Table 3. Section B of the AM335x Input Spreadsheet

CORE OPP	OPP100
MPU OPP	OPP100
MPU Frequency (Mhz)	600

ARM Subsystem	Utilization %
Cortex-A8	0
Cortex-A8 NEON	0

SGX Subsystem (for SGX-enabled devices only)	Utilization %
SGX	0

The OPP options supported for the MPU voltage domain (VDD_MPU) and the CORE voltage domain (VDD_CORE) are shown in the following tables.

Table 4. PG1.0 VDD_CORE Operating Performance Points for ZCZ Package [1]

VDD_CORE OPP Device Rev "Blank"	VDD_CORE			DDR3, DDR3L [2]	DDR2 [2]	mDDR [2]	L3 and L4
	MIN	NOM	MAX				
OPP100	1.056 V	1.100 V	1.144 V	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP50	0.912 V	0.950 V	0.988 V	—	125 MHz	90 MHz	100 MHZ and 50 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) This parameter represents the maximum memory clock frequency. Since data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 5. PG1.0 VDD_MPU Operating Performance Points for ZCZ Package [1]

VDD_CORE OPP Device Rev "Blank"	VDD_MPU			ARM (A8)
	MIN	NOM	MAX	
Turbo	1.210 V	1.260 V	1.326 V	720 MHz
OPP120	1.152 V	1.200 V	1.248 V	600 MHz
OPP100 [2]	1.056 V	1.100 V	1.144 V	500 MHz
OPP100 [3]	1.056 V	1.100 V	1.144 V	275 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) Applies to all orderable AM335_ZCZ_50 (500-MHz speed grade) or higher devices.

(3) Applies to all orderable AM335_ZCZ_27 (275-MHz speed grade) devices.

Table 6. PG1.0 VDD_CORE Operating Performance Points for ZCE Package [1]

VDD_CORE OPP Rev "A" or Newer	VDD_MPU [2]			ARM (A8)	DDR3, DDR3L [3]	DDR2 [3]	mDDR [3]	L3 and L4
	MIN	NOM	MAX					
OPP100	1.056 V	1.100 V	1.144 V	500 MHz	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP100	1.056 V	1.100 V	1.144 V	275 MHz	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) VDD_MPU is emerged with VDD_CORE on the ZCE package.

(3) This parameter represents the maximum memory clock frequency. Since data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 7. PG2.1 VDD_CORE Operating Performance Points for ZCZ Package [1]

VDD_MPP OPP Rev "A" or Newer	VDD_CORE			DDR3, DDR3L [2]	DDR2 [2]	mDDR [2]	L3 and L4
	MIN	NOM	MAX				
OPP100	1.056 V	1.100 V	1.144 V	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP50	0.912 V	0.950 V	0.988 V	—	125 MHz	90 MHz	100 MHZ and 50 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) This parameter represents the maximum memory clock frequency. Since data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Table 8. PG2.1 VDD_MPU Operating Performance Points for ZCZ Package [1]

VDD_CORE OPP Rev "A" or Newer	VDD_MPU			ARM (A8)
	MIN	NOM	MAX	
Nitro	1.272 V	1.325 V	1.378 V	1 GHz
Turbo	1.210 V	1.260 V	1.326 V	800 MHz
OPP120	1.152 V	1.200 V	1.248 V	720 MHz
OPP100 [2]	1.056 V	1.100 V	1.144 V	600 MHz
OPP100 [3]	1.056 V	1.100 V	1.144 V	300 MHz
OPP50	0.912 V	0.950 V	0.988 V	300 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) Applies to all orderable AM335_ZCZ_50 (500-MHz speed grade) or higher devices.

(3) Applies to all orderable AM335_ZCZ_27 (275-MHz speed grade) devices.

Table 9. PG2.1 VDD_CORE Operating Performance Points for ZCE Package [1]

VDD_CORE OPP Device Rev "Blank"	VDD_MPU [2]			ARM (A8)	DDR3, DDR3L [3]	DDR2 [3]	mDDR [3]	L3 and L4
	MIN	NOM	MAX					
OPP100	1.056 V	1.100 V	1.144 V	600 MHz	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP100	1.056 V	1.100 V	1.144 V	300 MHz	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP50	0.912 V	0.950 V	0.988 V	300 MHz	—	125 MHz	90 MHz	100 MHz and 50 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) VDD_MPU is emerged with VDD_CORE on the ZCE package.

(3) This parameter represents the maximum memory clock frequency. Since data is transferred on both edges of the clock, double-data rate (DDR), the maximum data rate is two times the maximum memory clock frequency defined in this table.

Module utilization is the percentage of the available MHz at the selected OPP needed to meet the scenario processing requirement.

A separate utilization entry is provided for the Cortex-A8 ARM processor and the NEON SIMD engine.

- Cortex-A8 (ARM Cortex-A8 processor core): 0 - 100 %
- Cortex-A8 NEON (General purpose SIMD engine): 0 - 100 %

For the graphics accelerator subsystem, a separate utilization entry is provided:

- SGX (2D/3D graphics accelerator engine): 0 - 100 %

2.4 Section C: Peripherals

This section is used to configure the activity on peripheral modules as shown in Table 10.

Table 10. Section C of the AM335x PET Input Spreadsheet

Module Name	Utilization %
EDMA	0
EMIF	0
GPMC	0
OCMC-RAM	0
LCDC	0
USB	0
Ethernet MAC	0
PRUSS	0
McASP1	0
McASP2	0
MMC1	0
MMC2	0
MMC3	0
Misc: Peripheral (UART, SPI, I2C, CAN, GPIO, eHRPWM, eQEP, RTC, and so forth)	0

For each of the modules, enter module utilization as a percentage (0-100). A separate utilization entry is provided for the following modules:

- Enhanced Direct Memory Access (EDMA) controller
- External Memory Interface (EMIF) controller
- General-Purpose Memory Controller (GPMC)
- On-Chip Memory Controller and RAM (OCMC-RAM)
- LCD Controller (LCDC)

- Universal Serial Bus (USB)
- Ethernet MAC
- Programmable Real-Time Unit Subsystem (PRUSS)
- MultiChannel Audio Serial Port (McASP)
- MultiMedia Card (MMC) host controller
- Misc. PERIPHERALS (other miscellaneous peripherals such as universal asynchronous receiver/transmitter (UART), serial peripheral interface (SPI), inter-integrated circuit (I2C), controller area network (CAN, general-purpose input/output (GPIO), enhanced high-resolution pulse-width modulator (eHRPWM), enhance quadrature encoder pulse (eQEP) and real-time clock (RTC) modules)

2.5 Section D: Analog Modules

Section D enables a configuration for analog modules in the AM335x as shown in Figure 2.

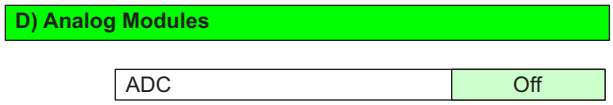

Figure 2. Section D of the AM335x PET Input Spreadsheet

- ADC (A/D converter): On, Off

3 Spreadsheet Upload

Upload your AM335x PET Input Spreadsheet here.

Upon completion of the input spreadsheet, upload the spreadsheet to TI for the power consumption analysis. Registration and legal agreement acceptance is required for the upload.

4 Power Analysis Report

4.1 Power Estimation Report Sheet

The power estimation tool generates a power analysis report in a spreadsheet format (see Table 11). The estimated values are leakage, active and total average power over the time during the entire application scenario. The report also lists per power rail groups. When SmartReflex (AVS) is enabled, MPU and CORE voltage rails show controlled voltages by SmartReflex.

Input file name: am335x_pet_input_example.xls

Junction Temperature (°C)

Device Process: nominal

ARM Clock Freq [MHz]: NITRO (1000)

Table 11. Power Estimation Report

	Voltage (V)		Current (A)		Power (W)	
	MIN	MAX	Leakage	Active	Average	Total
VDD_MPU	1.33	1.33	0.002	0.542	0.544	0.72315
VDD_CORE	1.10	1.10	0.002	0.170	0.171	0.18828
VDDS_DPLL [1]	1.80	1.80	0.000	0.007	0.007	0.01195
VDDS_SRAM [2]	1.80	1.80	0.005	0.000	0.005	0.00815
VDDS_DDR	1.50	1.50	0.000	0.003	0.003	0.00533
VDDS_1P8 [3]	1.80	1.80	0.000	0.002	0.002	0.00348
VDDS_3P3 [4]	3.30	3.30	0.000	0.000	0.000	0.00016
VDDA1P8V_USB0/1, VDDA_ADC	1.80	1.80	0.000	0.000	0.000	0.00090
VDDA3P3V_USB0/1	3.30	3.30	0.000	0.000	0.000	0.00000
Total						0.94140

1. VDDS_DPLL includes VDDS_PLL_MPU, VDDS_PLL_CORE_LCD and VDDS_PLL_DDR power supplies.
2. VDDS_SRAM includes VDDS_SRAM_CORE_BG and VDDS_SRAM_MPU_BB power supplies.
3. VDDS_1P8 includes VDDS, VDDS_RTC, VDDS_OSC and 1.8 V VDDSHVx power supplies.
4. VDDS_3P3 inclues 3.3 V VDDSHVx power supplies.

Power consumption in the AM335x device consists of:

- Leakage power – due to leakage current, and dependent on temperature and device process
- Active power – due to transistor switching, and independent of temperature

The AM335x Power Estimation Tool models temperature and device process effects on device power consumption. Active power consumption is the power that is consumed by portions of the AM335x that are performing some processing. Active power is independent of temperature, but dependent on voltage and module activity levels.

4.2 Module Utilization Sheet

The available bandwidth for each module depends on the device interconnects architecture and the selected CORE OPP. The power estimation tool calculates current module bandwidth from utilization entered by you and shows the results for each time slot with the maximum available bandwidth for the selected OPP in a separate worksheet (see Table 12).

Table 12. Maximum Module Utilization

Module	Slot 0 Max	Slot 0 Current	Unit
Cortex A8	1000	850	MHz
SGX	1600	0	MBps
EDMA	800	0	MBps
EMIF	3200	1280	MBps
GPMC	800	0	MBps
OCMC-RAM	800	0	MBps
LCDC	800	240	MBps
USB	800	0	MBps
Ethernet MAC	800	0	MBps
PRUSS	800	0	MBps
MCASP1	800	0	MBps
MCASP2	800	0	MBps
MMC1	800	0	MBps
MMC2	800	0	MBps
MMC3	800	0	MBps
Misc	6800	120	MBps

The following note and limitation applies to the AM335x Power Estimation Tool:

- **It is up to you to input reasonable utilization numbers for the MPU subsystem** for the purposes of maximum power analysis. 90-100% loading on the subsystem is not realistic for most application scenarios.

5 References

1. AM335x Power Consumption Summary
2. *AM3359, AM3358, AM3357, AM3356, AM3354, AM3352 Sitara™ AM335x ARM® Cortex™-A8 Microprocessors (MPUs) Data Manual* (SPRS717)
3. *AM335x ARM® Cortex™-A8 Microprocessors (MPUs) Technical Reference Manual* (SPRUH73)
4. AM35x Power Estimation Tool
5. AM/DM37x Power Estimation Spreadsheet

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