OMAP5910 Audio System Design

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ABSTRACT

The OMAP5910 is a true system-on-a-chip device, which consists of ARM925T MPU and C55x DSP cores. The device has a large set of peripherals that can be utilized to interface with external radio receivers and audio codecs. This document demonstrates a system audio design using the McBSP1 port of the OMAP5910 and an external audio codec running synchronously with the oversampling master clock. This document also highlights some of most common problems associated with audio designs and design techniques to solve these problems.

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1   Introduction

This document is intended to demonstrate an audio system design utilizing the OMAP5910 dual-core processor and the TLV320AIC23 audio codec, and is divided into four different parts. The first part covers the basic audio design concepts, the second covers the OMAP5910 McBSP1 and the TLV320AIC23 codec design, the third part covers the audio algorithms supported, and the fourth part shows benchmarks of the popular audio coding algorithms.

2   Design Description

2.1   System Audio Design Concepts

A typical audio system consists of many critical analog and digital sections, so good design techniques must be applied to prevent noise from propagating from the microphone or line input to the speaker output
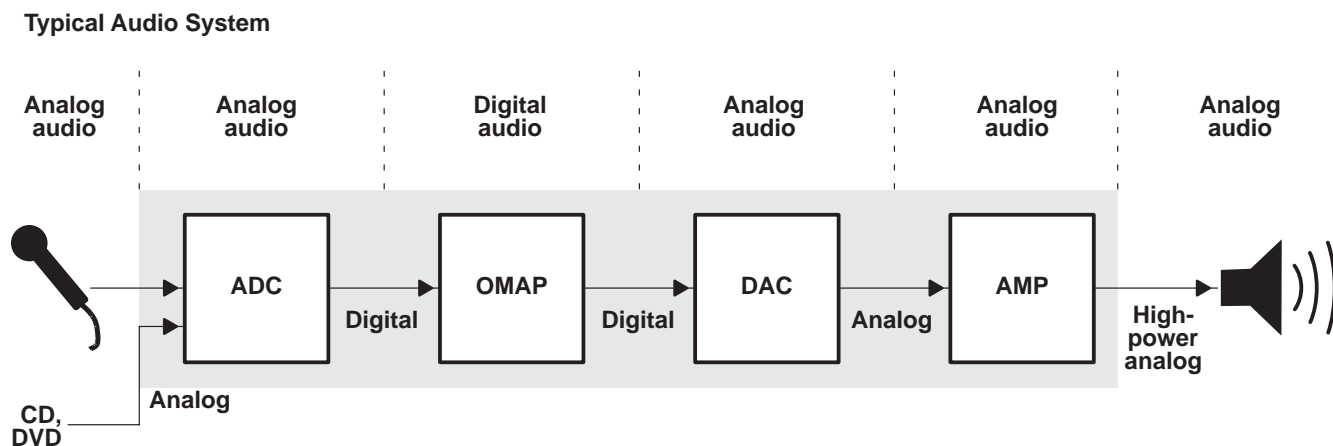
Typical Audio System

Figure 1. OMAP5910 Audio Overview

Figure 1 shows a complete signal chain of the OMAP5910 audio design. From the ADC to the Amp stage, if the design is not done properly on any of the blocks shown in the diagram, the performance will not be as what the designers are expecting. The following shows a list of common audio design problems:

- Noise coupled to the microphone input

- No anti-aliasing filter at the microphone and line inputs

- Excessive distortion due to mismatched audio amplitudes

- Excessive jitter on audio clocks, bit clock, and master clock

- Lack of good decoupling and noise isolation techniques

- Not using a linear regulator with high power supply rejection to isolate noise from the audio codec

- Not having good decoupling capacitors on the reference voltage used for ADC and DAC converters

- Switching power supply noise coupled to the audio circuits
- Printed circuit board layout, high impedance audio traces must be isolated from the noisy switching circuits

In summary, having good audio performance requires proper designs of the input stages of the codec, the OMAP interface, and the output amplifier. The OMAP5910 audio architecture is shown in Figure 2 where the interface is configured as an I^2S interface with the OMAP being a master driving the bitclock (McBSP1.CLK) and frame sync (McBSP1.FSX) signals.
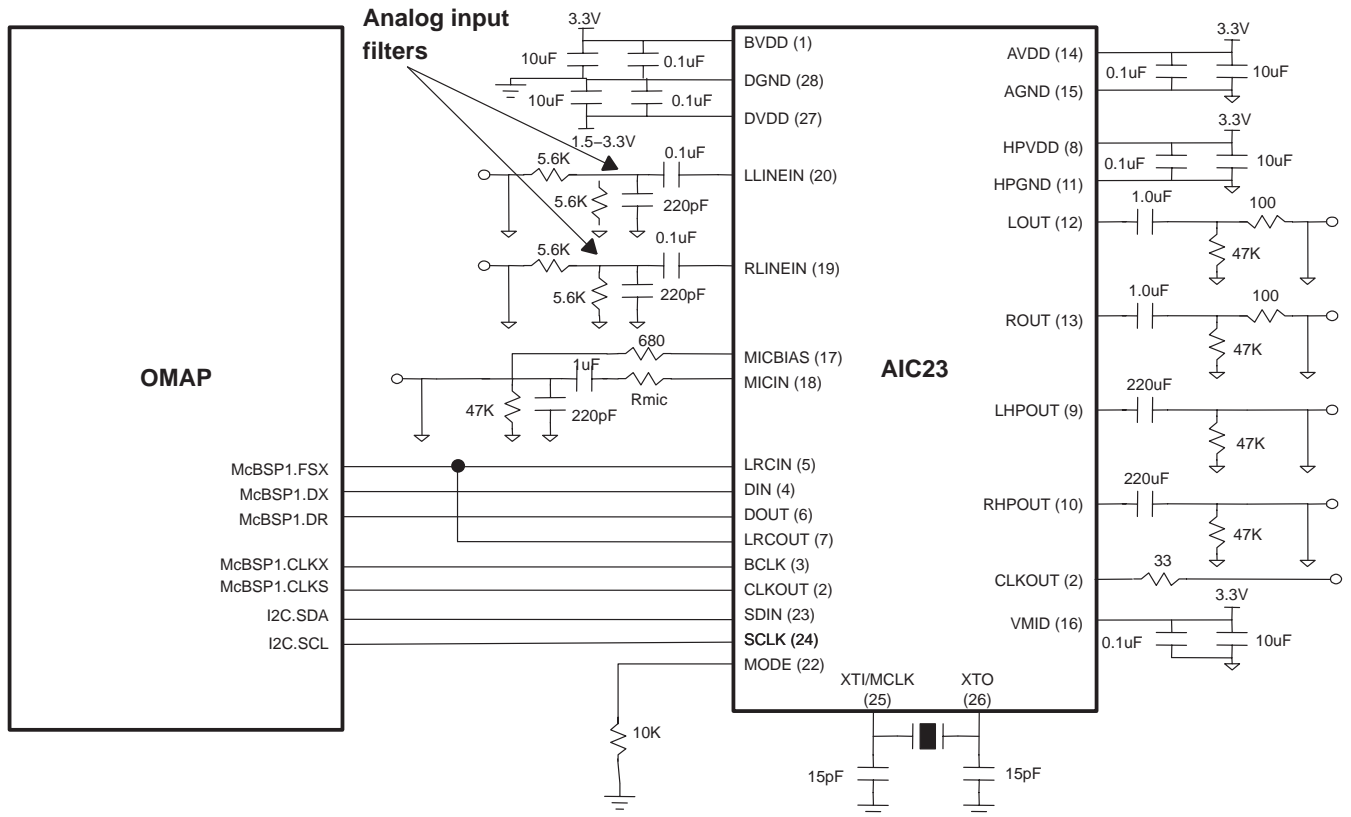

Figure 2. OMAP5910 Audio System Architecture

The audio codec, microphone, line-in, line-out, headphone-out and OMAP5910 interface circuits will be discussed and demonstrated.

2.1.1   *Audio CODEC (ADC and DAC)*

The audio codec shown in Figure 1 consists both oversampling ADC and DAC. The codec is based on the multibit sigma-delta technology with integrated oversampling digital interpolation filters. The basic architecture of the ADC is shown in Figure 3.
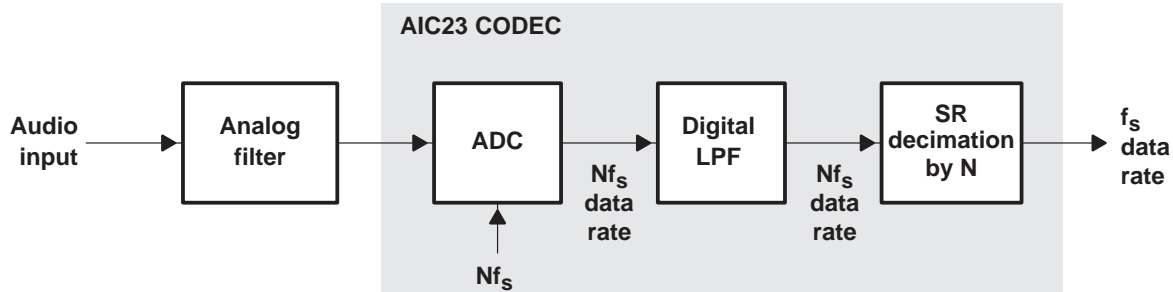
NOTES: 1. Oversample by N pushes the quantization noise way above the audio spectrum. Sampling at Nyquist rate (2 times the highest frequency component) requires higher order anti-aliasing filter.
2. Digital LPF removes the noise generated by the ADC.
3. Sample Rate (SR) decimation reduces the data rate for audio processing.

Figure 3. Simplified Oversampling ADC Architecture

The ADC architecture shown in Figure 3 is part of the TLV320AIC23, which includes a third-order multibit architecture with up to 90 dBA signal-to-noise (SNR) ratio at audio sample rate up to 96 kHz. The oversampling clock (Nf_S) supports the industry standard rates such as 256 f_S or 384 f_S as well as other unique sampling rates, 250 f_S or 272 f_S. The unique sampling rates become very useful when designers want to clock the part with a standard 12-MHz oscillator. For example:

- To generate 44.1-kHz sample rate audio, use 12 MHz/272 = 44.1 kHz

- To generate 48-kHz sample rate audio, use 12 MHz/250 = 48 kHz

This example demonstrates how to get the correct sample rates using a standard 12MHz clock input.

The DAC architecture shown in Figure 4 is part of the TLV320AIC23, which includes a second-order multibit architecture with up to 100 dBA SNR at audio sample rate up to 96 kHz. The oversampling clock is configured the same way as described in the ADC paragraph.
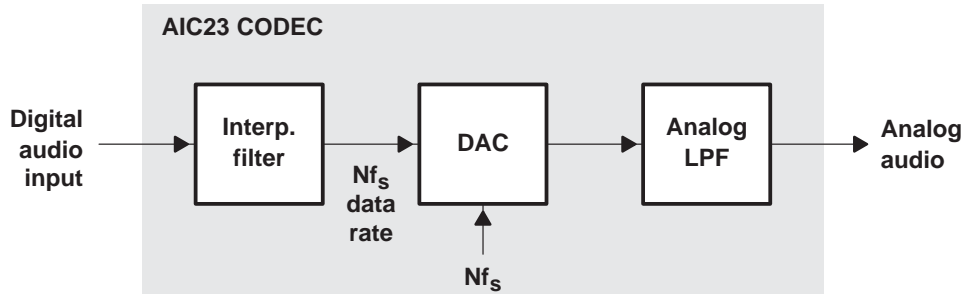
NOTES: 1. Interpolation filter increases the sample rate by N for the oversample DAC to process the data.
2. Analog low-pass filter is required to remove the sampling noise. This filter is included in the TLV320AIC23 device.

Figure 4. Simplified Oversampling DAC Architecture

2.1.2   *Microphone Circuit*

The two types of microphones commonly being used are electret (capacitive) and dynamic (inductive) condensers. The electret condenser microphone is based on the idea of sound pressure causing a movement of the capacitor plates while the dynamic condenser relies on the sound wave creating pressure to move the coil. The electret microphone is very small and low cost and has become the preferred choice for computer audio, consumer audio and cell phone applications.

In the audio system shown in Figure 1, the microphone input is very sensitive to noise because microphone output impedance driving the codec is high and the voltage amplitude is small (~100 mV). The codec typically has about 20-dB gain to increase the signal amplitude before digitizing and capturing the audio signal for processing. So, any noise coupled to the input will be increased by 10 times and this increase causes a decrease in audio performance, or lower signal-to-noise. Figure 5 shows an example of how to design a microphone circuit using TI's TLV320AIC23 audio codec. Utilizing the codec with internal mic amp such as TI TL320AIC23 reduces the circuit complexity and, therefore, improves the overall noise performance.
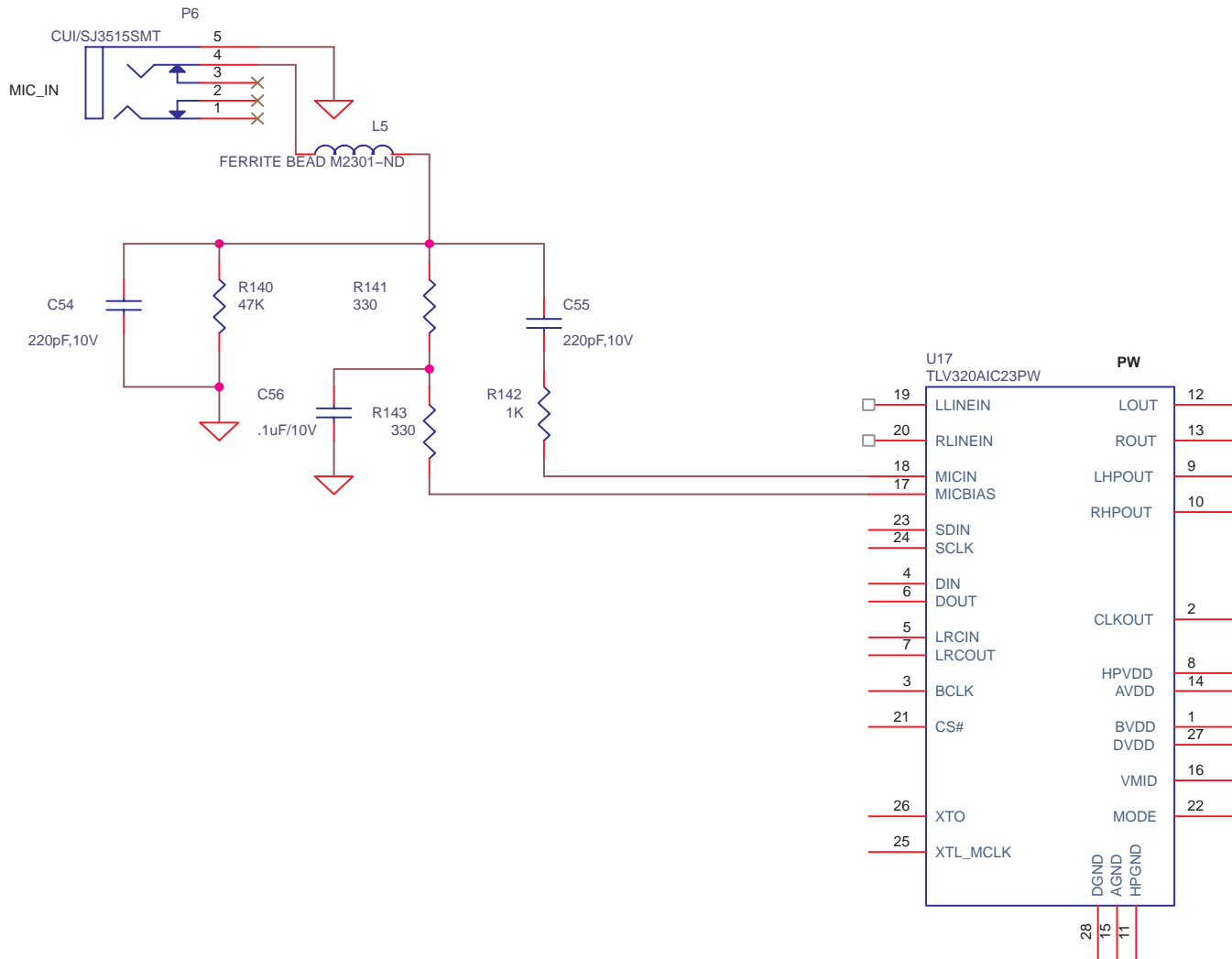
Figure 5. Microphone Circuit

2.1.3 Line-In Circuit

A line-in circuit consists of a resistor divider network to prevent input clipping and an anti-aliasing filter to limit the audio bandwidth. This is necessary to prevent the out-of-band folding back into the audio spectrum, which degrades the audio performance.

Depending on the audio source driving the line-in port, the amplitude can be as low as 0.5 V peak-to-peak to as high as 5.656 V peak-to-peak. If the codec is operating at 3.3-V supply, a signal going above the supply is not possible and is clamped or clipped at the supply voltage by the internal protection diodes. See details in Figure 6.

Input level is clipped at ~3.3 Vpp when overdriving the CODEC

Figure 6. Line-In Audio Clipping
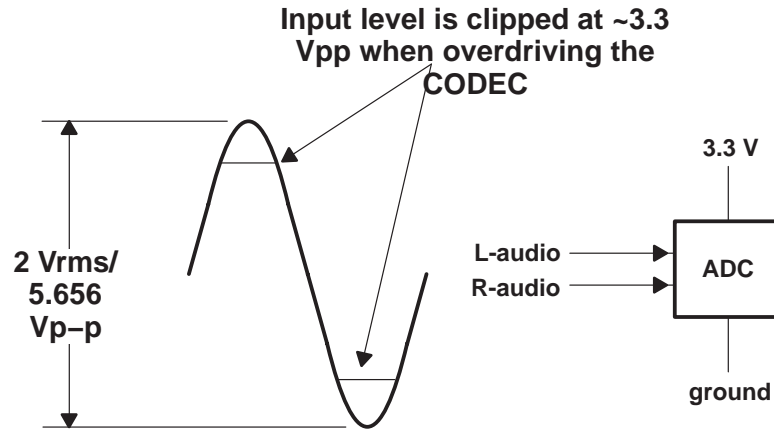
To prevent audio clipping, designers must add a resistor divider network at the input. This circuit also lowers the input amplitude when the audio source output is low. However, this can be compensated by adding more gain at the external amplifier stage or at the internal volume control circuit of the codec. See Figure 7 for detailed implementation of the divider input circuit.
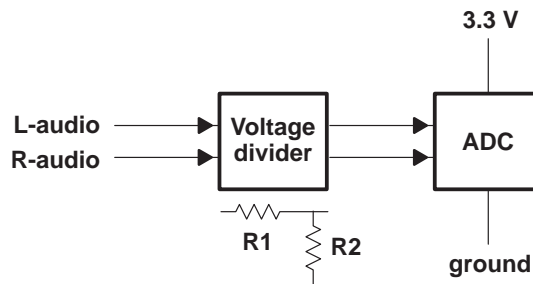
NOTE: Add a voltage divider network to limit the AC input signals to the codec with 3.3 V supply voltage. In this example, let maximum CODEC input be 2.828 V. This provides adequate margin for the 3.3-V operation.

$$2.828\ V = 5.656\ V\frac{R2}{(R1\ +\ R2)} \rightarrow R2\ =\ R1$$

Let R1 = 5.6 K → R2 = 5.6 K,
keep input impedance equal to or greater than 10 k.

Figure 7. Input Divider Circuit

A line-in circuit also needs to be bandwidth-limited to avoid an aliasing problem, which occurs when the maximum frequency of the input signal is greater than half of the sampling frequency. Since the ADC is an oversampling sigma-delta (256 or 384 oversample), the anti-aliasing filter does not have to be higher order; first order passive filter is adequate. With the TLV320AIC23 codec, the filter 3-dB corner is

$$f_{-3\ dB} = \frac{1}{2\pi RC}, \text{where R} = 5.6\ \text{K (part of the resistor divider and C} = 220\ \text{pF)}$$

$$= 129\ \text{kHz}$$

Since the ADC oversampling clock is in the MHz range, limiting the input bandwidth to 130 kHz is adequate. Figure 8 shows the complete line-in circuit using the described techniques.
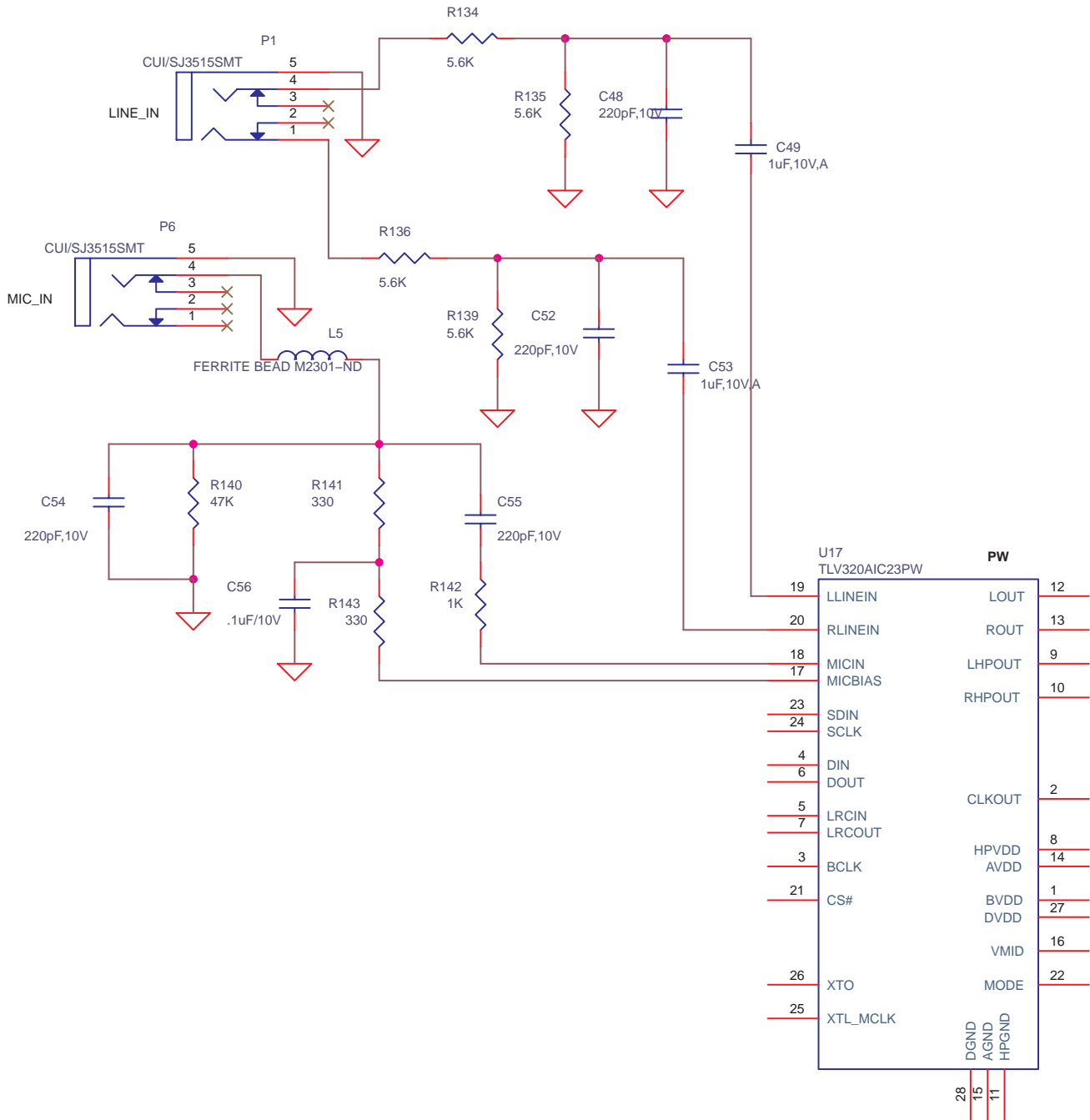

Figure 8. Line-In Circuit

2.1.4 Line-Out and Headphone-Out Circuits

The line-out circuit is very simple since the output imaging filter is internal to the codec. In some applications such as high performance entertainment and automotive audio systems, a pre-amplifier may be required to boost the codec output amplitude, which is limited by the supply voltage. A pre-amplifier can also provide high current drive capabilities for a long audio cable connected to the line-out circuit. In many other applications, taking line-out signals directly from the codec is adequate. However, these outputs must be AC-coupled using a series capacitor to remove the DC component of the signal. Also, it is a good design practice to add a series termination resistor to limit the current when the line-out is accidentally shorted to ground. See Figure 9 for detailed circuit diagram.
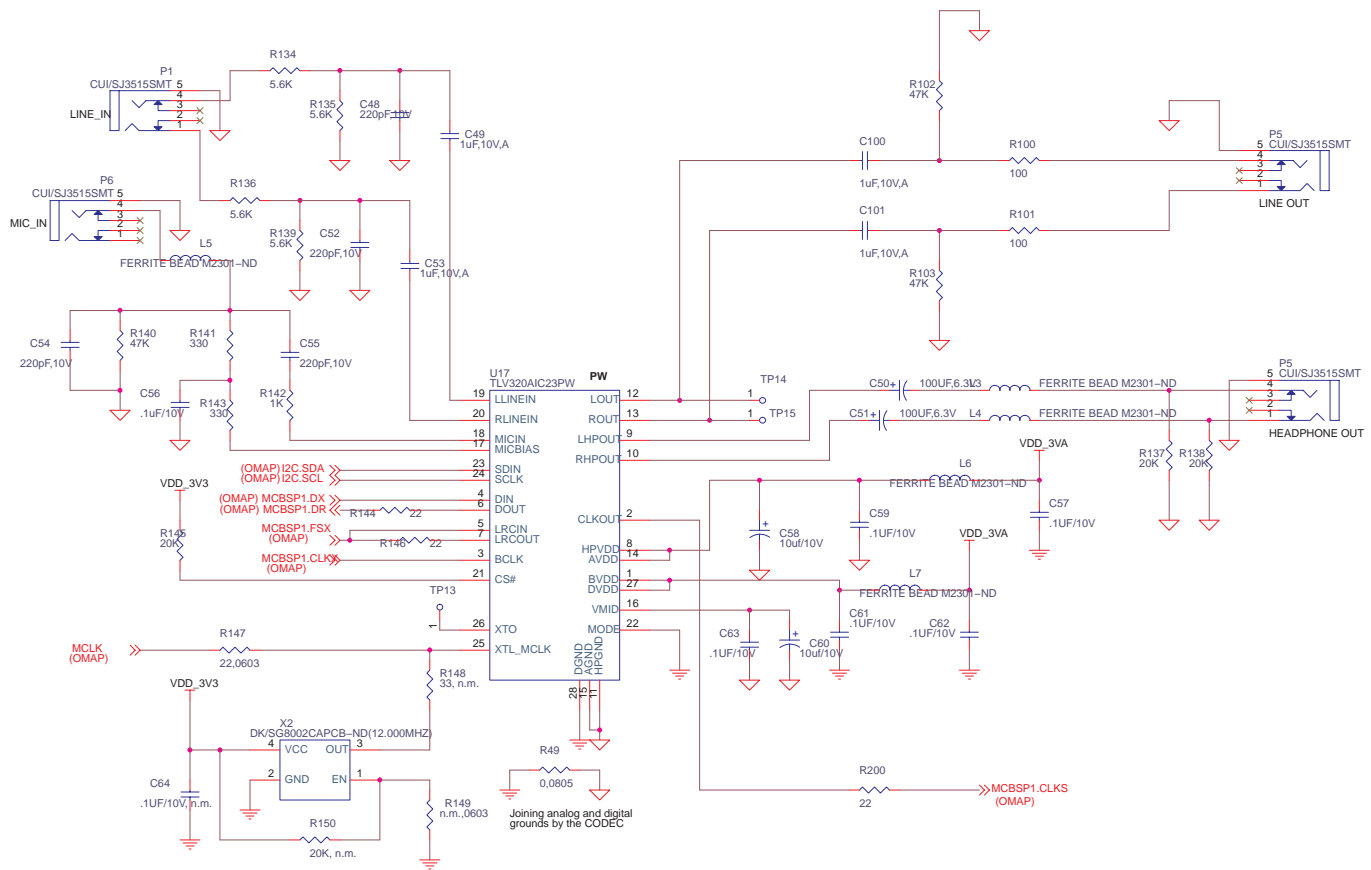
Figure 9. Line-Out and Headphone-Out Circuits

As far as headphone output shown in Figure 9, the codec has an integrated headphone amplifier capable of driving 30 mW into a 32 ohms load. Typically, a headphone has 32 ohms impedance so 30 mW is sufficient for delivering good audio to the listener. Unlike line-in, the headphone outputs only need AC-coupled capacitors to remove the DC component of the signals, not series resistors. Series resistors on headphone outputs limit the drive current needed to adequately power the headphone and, therefore, should not be included. For the AC-coupled capacitor, the minimum value is

$$f_{-3\ dB} = \frac{1}{2\pi RC},$$ where C is the coupling capacitor and R is the headphone impedance,

$$= 50\ Hz,$$ adequate low-end frequency spectrum for headphone.

Let R = 32 ohms $\rightarrow$ C = 100 uF.

2.1.5   OMAP5910 McBSP1 Interface

2.1.5.1   Multichannel Buffered Serial Ports (McBSPs)

OMAP5910 has three McBSP ports where McBSP1 and McBSP3 are on the DSP public peripheral bus and McBSP2 is on the MPU public peripheral bus. The following lists the features of all McBSPs:

- Full-duplex communication
- DMA support for both RX and TX transfers
- Double buffered data registers, allowing the continuous data stream
- Independent framing and clocking for receives and transmits
- External shift clock generation or an internal programmable frequency shift clock
- Multichannel transmits and receives of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24 or 32 bits
- μ-Law and A-Law companding
- Data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Support bit rates up to 12Mbps
- RX and TX interrupts as well as data overrun interrupt

For more information, refer to the OMAP5910 Technical Reference Manual. In this audio application, the McBSP1 is being utilized and configured as an I2S port. I2S protocol is commonly being used in the industry as the standard audio interface for ADCs, DACs, and other audio processors. One unique feature of McBSP1 is that this is the only port that has the sample rate generator, which takes an external oversampling clock to create a bitclock.

2.1.5.2   OMAP Audio Interface

As mentioned in previous sections, McBSP1 of OMAP5910 is utilized to interface with TLV320AIC23 codec, which is configured to be an I2S slave. OMAP5910 is the master, which means it drives bitclock (BCLK) and frame sync (LRCOUT) onto the I2S bus. Table 1 shows the I2S interface.

Table 1. OMAP5910 and TLV320AIC CODEC

OMAP5910	TLV320AIC23	Schematic Ref.	Description
McBSP1.FSX	LRCIN, LRCOUT	McBSP1.FSX	Frame sync transmitted by the OMAP5910
McBSP1.DX	DIN	McBSP1.DX	Data transmitted by the OMAP
McBSP1.DR	DOUT	McBSP1.DR	Data transmitted by the CODEC
McBSP1.CLKX	BCLK	McBSP1.CLKX	Bitclock transmitted by the OMAP
McBSP1.CLKS	CLKOUT	McBSP1.CLKS	Oversampling buffered clock transmitted by the CODEC
I^{2}C.SDA	SDIN	I^{2}C.SDA	OMAP I^{2}C address/data
I^{2}C.SDL	SCLK	I^{2}C.SDL	I^{2}C clock

OMAP5910 has an I^{2}C master integrated for controlling and setting external devices such as the audio codec. The two signals in I^{2}C master are I^{2}C.SDA and I^{2}C.SDL. These signals are driven by the OMAP to I^{2}C clients. For more details, refer to the OMAP5910 Technical Reference Manual.

2.2   Audio Algorithms and Benchmarks

2.2.1   Audio Algorithms

OMAP5910 consists of an ARM925 general purpose processor and a C55xx digital signal processor. Currently, there are many algorithms ported to the C55xx architecture by TI's Third Party Network partners. Here is a list of audio algorithms supported by the C55xx and OMAP architecture.

- 5-band equalizer
- Stereo sample rate converter
- Dolby AC3 decode
- MPEG-1 Layer 3 or MP3 encode and decode
- Advanced audio coding or AAC encode and decode
- Windows media audio or WMA decode
- Windows media audio with digital rights management decode
- Windows media audio encode
- Lucent enhanced perceptual audio ding or ePAC
- MPEG-1 layer I encoder and decoder
- MPEG-1 layer II encoder and decoder

2.2.2   Audio Benchmarks

Table 2 lists some of the popular audio benchmarks measured by the Third Party Networks partners. Each benchmark includes a memory usage and a DSP utilization.

Table 2. Audio Benchmarks

Algorithm	Memory	DSP Utilization	Comment
AAC Decode	21 Kwords of SARAM, 11 Kwords of DARAM	20.5 MHz peak for stereo 44.1 kHz at 128 Kbps	18.5 MHz average utilization
AAC Encode	27 Kwords DARAM, 14 Kwords data ROM, 23 Kwords program ROM	73 MHz peak for stereo 44.1 kHz at 128 Kbps	64 MHz average utilization
MP3 Decode	11 Kwords DARAM, 8 Kwords data ROM, 10 Kwords program ROM	21 MHz peak for stereo 44.1 kHz at 128 Kbps	15.4 MHz average utilization
MP3 Encode	24.2 Kwords DARAM, 8.3 Kwords data ROM, 30 Kwords program ROM	93 MHz peak for stereo 44.1 kHz at 128 Kbps	61 MHz average utilization
WMA Decode	27 Kwords DARAM, 11.5 Kwords data ROM, 16.5 Kwords program ROM	44.4 MHz peak for stereo 44.1 kHz at 128 Kbps	17.5 MHz average utilization
5-Band Equalizer	208 DARAM, 266 words data ROM, 1.427 Kwords program ROM	7.64 MHz peak and 7.58 MHz average	

3   Conclusions

This application note provides an example for systems engineers to design an audio system utilizing the OMAP5910 McBSP1 peripheral and the TLV320AIC23 audio codec. This design was prototyped and its functionalities were verified on the OMAP5910 Innovator Development Platform. The audio benchmarks running on C55xx were done by TI Third Party Networks partners. Since OMAP5910 consists of multiple serial ports, McBSP1, McBSP2, and McBSP3, it is possible to design a system with multiple codecs running synchronously with the OMAP oversampling clock frequency, McBSP1.CLKS. In this case, only one audio master is allowed. Multiple codecs architecture enables designers to capture multiple audio inputs and to do mixing and sample rate conversions digitally.

4   References

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3. Productivity Systems, Inc*, Innovator Development Kit for the Texas Instruments OMAP Platform*
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5. Texas Instruments Inc., *Audio Algorithms for C54xx/C55xx DSPs*, November 2002.

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