Migrating from TMS320VC5410 to TMS320VC5410A

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5410 to the TMS320VC5410A. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets, 5410 (SPRS075), 5410A (SPRS139), the *TMS320C54x DSP CPU and Peripherals Reference Set, Volume 1* (SPRS131) and the *TMS320C54x DSP Enhanced Peripherals, Reference Set, Volume 5* (SPRU302).

Migration issues from the 5410 to 5410A are indicated with the following symbols:

S means software modification is required

H means hardware modification is required

D means the 5410 and 5410A are different (usually due to added features on the 5410A) but no modification is necessary for migration (i.e. different but compatible).

These symbols are included at the beginning of each section.

Revision History:

Revision	Date	Description
1.0	06/19/00	Original

Contents

1 Package and Pinout Compatibility [D]

The 5410A is available in two package types:

- 144-pin ‘PGE’ thin quad flat pack (TQFP)
- 144-pin ‘GGU’ microstar™ ball grid array (BGA)

While the 5410 is available in two package types:

- 144-pin ‘PGE’ thin quad flat pack (TQFP)
- 176-pin ‘GGW’ microstar™ ball grid array(BGA)

The 5410A is pin compatible (same footprint and pinout) with the PGE 5410. Note that there is a “no connect” (NC) pin on the 5410 (PGE pin no. 80), this pin is given a new name (HPI16 pin) and used to configure the 5410A HPI to either an 8-bit HPI or a 16-bit HPI.

2 Power Supply [H]

The 5410 CVdd operates at 2.5V and DVdd operates at 3.3V while the 5410A CVdd operates at 1.5V and DVdd operates at 3.3V.

The power-up/power-down sequence on 5410A is not different from that of 5410. Both supplies may be powered up/down simultaneously. If it is impossible to power-up/down the CVdd and DVdd simultaneously, CVdd must be powered up first, DVdd second. For power-down, DVdd must be powered down first, CVdd second.

3 Clock Mode Settings at Reset [H]

The PLL programming and operation of the 5410A PLL is similar to the 5410 but the clock mode settings at device reset is different. Refer to 5410 (SPRS075) and 5410A (SPRS139) data sheets for more details. Note that the 5410A does not support the clock mode of internal oscillator with external crystal.

4 Multichannel Buffered Serial Port (McBSP) [H/S]

The 5410A McBSP slightly differs from the 5410. The 5410A McBSP has been enhanced:

- To allow all 128 channels of a 128-channel bit stream can be enabled simultaneously
- To enable the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator

Three control bits and twelve registers have been added to enable the 128 channel selection.

The CLKS pin available on the 5410 GGW package is not available on the 5410A in either PGE or GGU packages. Refer to the 5410A data sheet (SPRS139) for more details.

5 Host Port Interface (HPI) [H/S]

The 5410A HPI slightly differs from the 5410. In addition of capability to interface to an 8-bit host, the 5410A HPI has been enhanced so it can be interfaced to a 16-bit host processor. Note that unlike the 5410 HPI, the 5410A HPI does not support the host-only-mode (HOM) during reset.

6 16-bit HPI (HPI16) [H]

The 5410A host port interface can be configured as an 8-bit HPI (HPI8) or a 16-bit HPI (HPI16) via a dedicated pin, namely pin HPI16, as mentioned above in the Package and Pinout Compatibility section. This pin has an internal pull down resistor. When it is left unconnected or tied to ground, the 5410A HPI is configured as an HPI8. By tying the pin to DVdd, the 5410A HPI is configured as an HPI16 in non-multiplexed mode.

The external signals associated with the HPI16 are significantly different from those on the 5410A when HPI is configured as an 8-bit HPI. Refer to the 5410A data sheet (SPRS139) for more details.

7 HPI Memory [D]

The 5410A HPI memory map is the same as the 5410. The 5410A HPI memory type is different from the 5410. The 5410A HPI memory is composed of DARAM (dual access RAM). Refer to 5410A data sheet (SPRS139) for more details.

8 DMA External and Extended Memory Transfer [H]

The 5410A DMA has external memory access that is implemented differently from the 5410. The 5410A DMA has been enhanced to provide the ability to access to extended external data and IO memory.

Two new bits have been added to the DMA transfer mode control register (DMMCRn) to specify the space (i.e. internal or external access) of the DMA transfer, one for the source and one for the destination. Also, two new 7-bit registers are added to specify the extended data and IO pages (page 0 to page 127), one for the source and one for the destination. Refer to the 5410A data sheet (SPRS139) for more details.

9 DMA Memory [D]

In internal access mode, like HPI memory, the 5410A DMA memory is all DARAM memory. In external access mode, for data, program and IO space, the 5416 DMA memory map is expanded to 8MW (128 64K pages). Refer to the 5410A data sheet (SPRS139) for more details.

10 DMA Auto-initialization [H/S]

The 5410A has been enhanced to expand the global reload register set. Each DMA channel now has its own global reload register set. For example the DMA channel 1 has DMGSA1, DMGDA1, DMGCR1 and DMGFR1 registers as its global reload registers. Refer to the 5410A data sheet (SPRS139) for more details.

11 DMA Interrupt Generation in ABU [S]

On the 5410, the half buffer interrupt is generated when the next address (in DMSRC for transmission or DMDST for reception) is greater than the halfway point of the transmit/receiving buffer if positive index is used, or when the next address is less than the halfway point when the negative index is used. For odd and even buffers, the interrupt point differs accordingly.

On the 5410A, the half buffer interrupt is generated when the next address is equal to or greater than the halfway point if positive index is used, or when the address is less than the halfway point when the negative index is used. For odd and even buffers, the interrupt point differs accordingly. For more info, please refer to sections 3.2.3.8 and 3.2.3.9 in the TMS320C54x DSP Enhanced Peripherals, Volume 5 (SPRU302).

12 Memory Map [D]

The memory map of the 5410A is similar to the 5410 with following exceptions:

- The 5410A has a total of 64K (eight 8K blocks) DARAM while the 5410 has 8K (four 2K blocks) DARAM.
- The 5410A has 16K ROM which is program only while 5410 has 16K ROM that can be program/data.

13 Bootloader/ROM Contents [D]

The bootloader options available on the 5410A are similar but not identical to the 5410.

- HPI boot. The 5410A does not support host access during reset. In the 5410A boot loader, the Host must download code into the internal memory of the 5410A after RESET. Upon completion, the Host must write the start address of the boot loaded section to 007Eh (upper 7 bit address) and 007Fh (lower 16 bit address).

The bootloader performs an HPI boot only when the memory location at 007Fh has been changed by the host. The location 007Fh serves as a pre-initialized pointer to the start address of the boot-loaded code.

14 Data Security [D]

The ROM security of the 5410A functions similarly to the 5410 with the following exception:

- 5410 allows both HPI read/write to a 2K block on-chip RAM (1000h–17FFh)
- 5410A allows both HPI read/write to only 8K on chip RAM (4000h–5FFFh)

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