

Dual Power Supply Recommendations for the TMS320C206

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Abstract

This document describes two options used to supply power to the Texas Instruments (TI™) TMS320C206 digital signal processor (DSP). The TMS320C206 DSP requires 3.3V for the CPU and 5.0V for the I/O.

The first solution applies when a design already has a regulated 5.0V power supply and requires only a 3.3V (LDO) Low Dropout regulator. The second solution applies an unregulated voltage input to both LDO regulators to generate the 5.0V and 3.3V voltages. As voltage requirements become stricter, tighter tolerance regulators, such as the TI TPS71/72/73 families of LDOs, are required.

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Design Problem

What are some options available to supply power to the TMS320C206 DSP, which requires 3.3V for the CPU and 5.0V for the I/O?

Solution

Two scenarios are discussed to apply proper power to the TMS320C206. The first solution applies when a design already has a regulated 5.0V power supply and requires only a 3.3V (LDO) Low Dropout regulator, as shown in Figure 1.

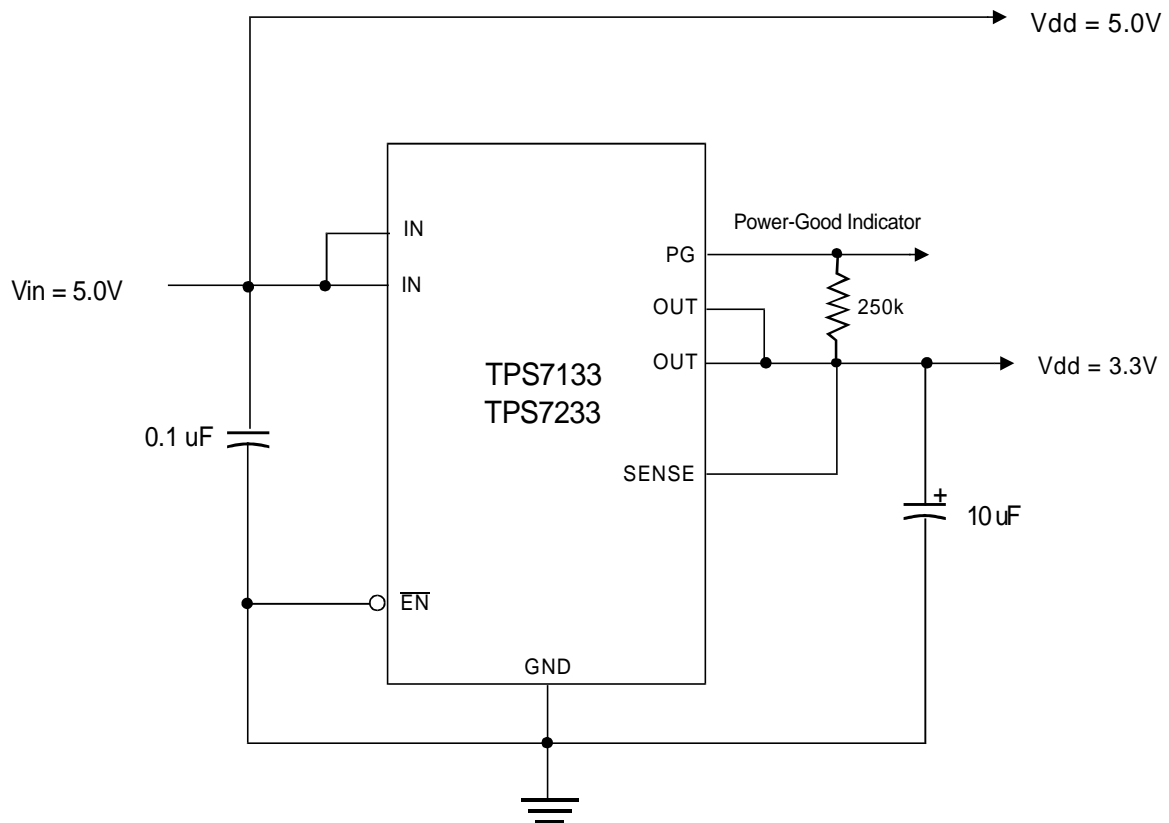
Figure 2 shows the second solution, in which an unregulated voltage input is applied to both LDO regulators to generate the 5.0V and 3.3V voltages. As voltage requirements become stricter, tighter tolerance regulators, such as the TI TPS71/72/73 families of LDOs, are required.

Texas Instruments provides a wide range of fixed and adjustable LDOs with load currents ranging from 150ma to 750ma. The examples shown in this document use fixed voltage LDOs. In a typical application maximum load currents of 250ma and 500ma are common. The maximum output load current for the TPS72xx series is 250ma and TPS71xx series is 500ma.

NOTE:

The TMS320C206 has a common ground between the 5.0V and 3.3V power. Detailed information regarding the TPS71xx (literature number SLVS092F) and TPS72xx (literature number SLVS102E) may be found at the TI web site, www.ti.com.

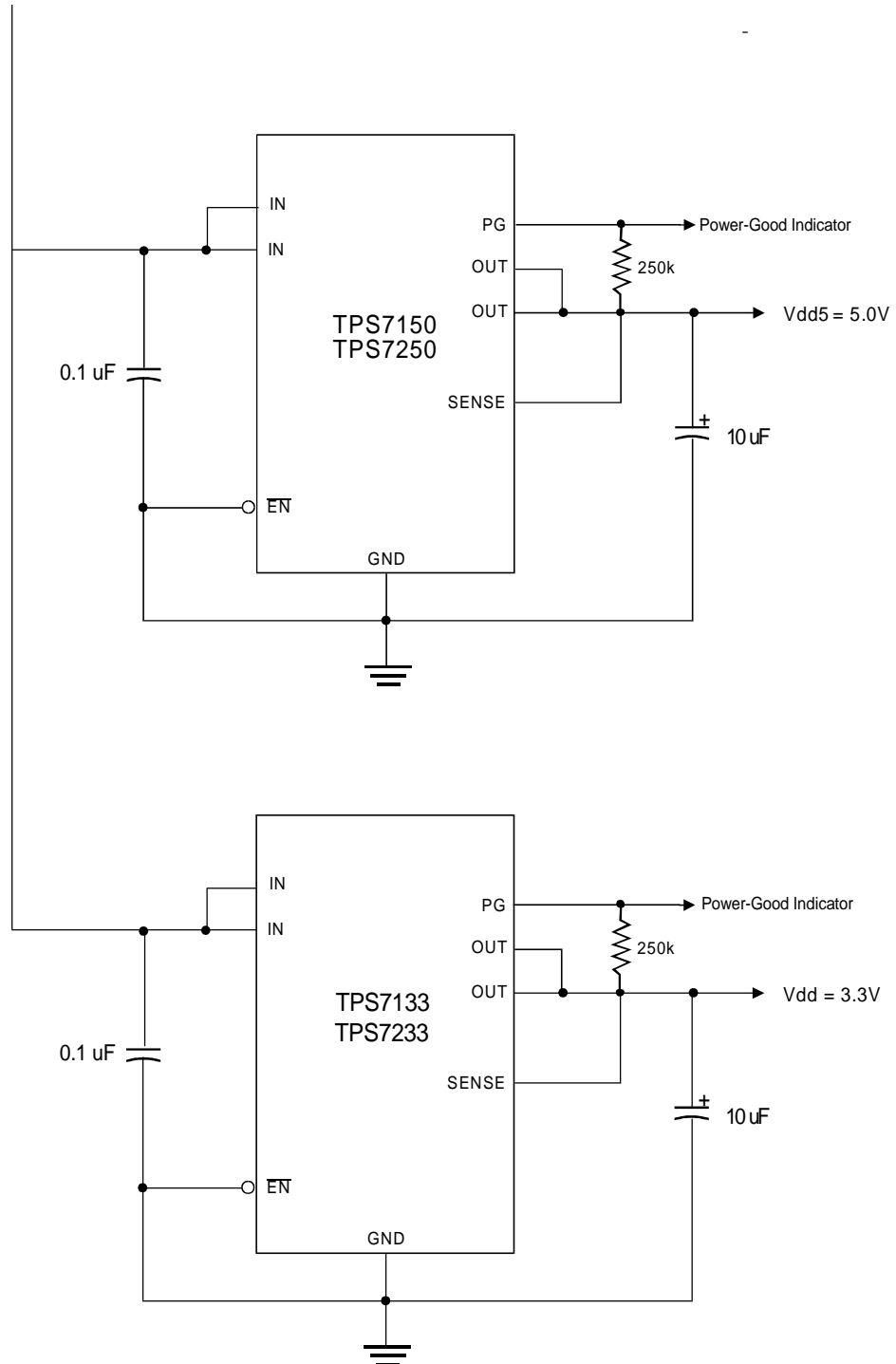
Figure 1. Supplying Power to the TMS320C206 with Existing Regulated 5.0V Supply



Note: If large line transients are expected, the input capacitance should be increased above the minimum value shown. If large load transients are expected, the output capacitance should be increased above the minimum value shown. Input and output capacitors should be located as close as possible to the LDO and the LDO should be located close to the load.

Figure 2. Supplying Power to the TMS320C206 Using 5.0V and 3.3V LDO Regulators

$5.41V < V_i < 10V$



Note: If large line transients are expected, the input capacitance should be increased above the minimum value shown. If large load transients are expected, the output capacitance should be increased above the minimum value shown. Input and output capacitors should be located as close as possible to the LDO and the LDO should be located close to the load.



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