Application Report
SPRA474

# How to Begin Development Today with the TMS320C6211 DSP

## ABSTRACT

Development may begin now for TMS320C6211 systems. Due to the compatibility between TMS320C6000 generation devices, current ‘C6000 tools may be used to develop code for the ‘C6211 and other future devices. This allows for systems to be up and running when silicon becomes available.

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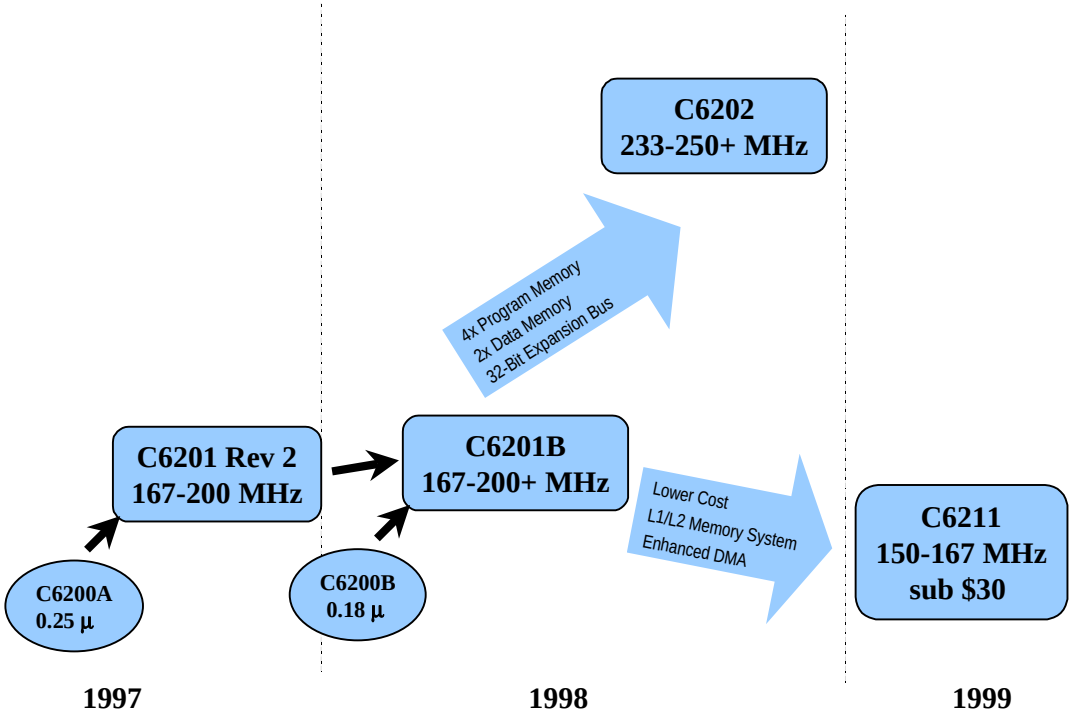
# How to Begin Development Today with the TMS320C6211 DSP

The Texas Instruments TMS320C6000 generation of high-performance digital signal processors now includes the TMS320C6211. The ‘C6211 is a low-cost version of the original ‘C6000 device, the ‘C6201. The ‘C6211 device will begin sampling in first quarter 1999, providing 1200 MIPS (million instructions per second) at 150MHz.

Introduced in February 1997, the ‘C6000 generation is based on TI’s VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Figure 1 shows the roadmap for the fixed-point generation of the ‘C6000 platform.

*Figure 1: TMS320C6200 Fixed-Point Roadmap*



# TMS320C6000 Compatibility

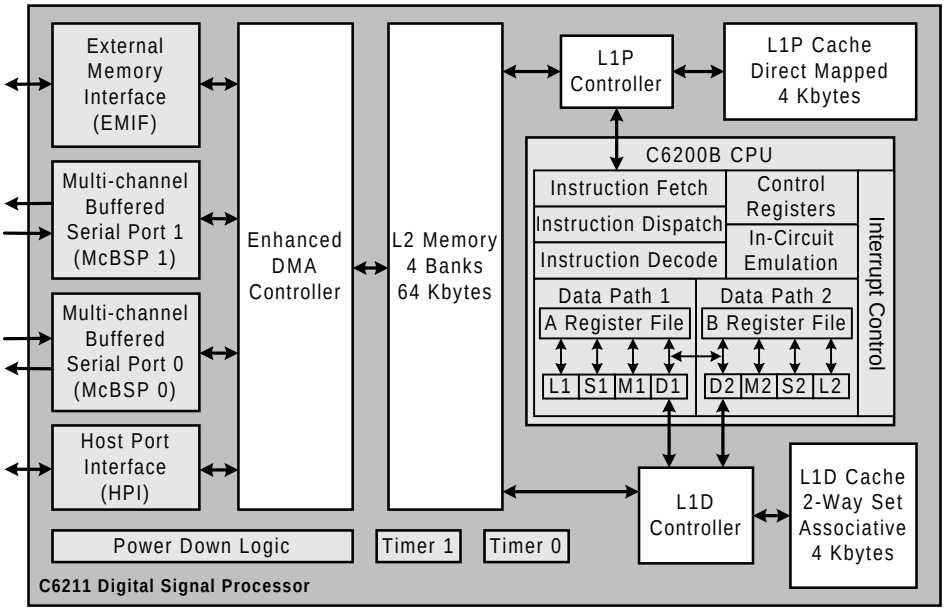
All ‘C6000 generation devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (‘C67x) members. All of the 'C6200 fixed-point devices are based on the same CPU core designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to eight instructions during a single clock cycle—up to 2000 MIPS at 250 MHz.

VelociTI's advanced features include instruction packing, conditional branching, variable-width instructions, and pre-fetched branching, all of which eliminate problems that were previously associated with VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the 'C6000 compiler.

This common architecture allows designers to begin development with existing ‘C6000 software tools for those devices currently in development. This also allows for migration from one ‘C6000 processor to another, as design requirements require.

In addition to the CPU, many of the on-chip peripherals are common between ‘C6000 devices. Figure 2 shows a block diagram of the ‘C6211. Those blocks in gray are shared between the ‘C6201 and ‘C6211.

*Figure 2: TMS320C6211 Digital Signal Processor*



## Similarities between the ’C6211 and ’C6201 DSPs

The ‘C6211 is highly-compatible with the first ‘C6000 device, the ‘C6201. The following device components are identical between the devices:

- **CPU**: The CPU of the ‘C6211 is identical to that of the ‘C6201, which means that code written for the ‘C6201 will run unmodified on the ‘C6211.
- **Multi-channel Buffered Serial Ports (McBSPs)**: The McBSPs are unchanged on the ‘C6211.
- **Host-Port Interface (HPI)**: The 16-bit asynchronous HPI is identical to that of the ‘C6201.
- **32-bit Timers**: Two timers are on the ‘C6211.
- **Interrupt Selection**: There are similar interrupt sources that may be used to interrupt the CPU or send an event to the DMA controller.

## Differences between the ’C6211 and ’C6201 DSPs

Several modifications have been made to allow the ‘C6211 to be available at a significantly lower cost than the original ‘C6201. These include:

- **Slower clock rate**: The maximum clock frequency has been decreased from 200 to 150MHz. This will still allow 1200MIPs during operation.
- **Cache memory architecture**: The ‘C6211 is a cache-based device, with separate level-one program and data caches. These small, fast memories are always active, and provide the CPU with a high (~98%) hit rate for most applications. Another internal memory block is available to use as a level-two cache, as a memory mapped SRAM space, or as a combination of the two.
- **Enhanced Direct Memory Access (EDMA) controller**: An enhanced DMA has been implemented on the ‘C6211 to provide more flexibility in programming data transfers.
- **External Memory Interface (EMIF)**: The EMIF has been enhanced to allow the device to interface to more memory types. The ‘C6211 can interface to 8-, 16-, and 32-bit SDRAM, SBSRAM, and asynchronous memories.

# Best Price/Performance

The cache architecture of the ‘C6211 allows for this device to be offered at a low cost, while keeping the high performance capabilities of the’C6000 generation. By having an efficient on-chip cache, system designers may use slower, less expensive external memory devices for data and program storage without seriously reducing the processing speed of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. The ‘C6211 has 72Kbytes of on-chip memory, with 8Kbytes serving as a level-one (L1) cache that the CPU can directly access. The L1cache is divided into 4 Kbytes of program (L1P) and 4 Kbytes of data (L1D) cache memory. The remaining 64Kbytes of on-chip memory is a unified program and data memory space. It can serve as a level-two (L2) cache, be directly mapped as internal memory, or serve as a combination of these functions.

L1P is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a wide data path to the CPU, so that the CPU may fetch eight instructions (one fetch packet) every cycle.

L1D is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both CPU data ports, so that the CPU can load or store two 32-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations.

The L2 memory is divided into four 16-Kbyte banks, each of which can be programmed as a cache or RAM space. Each bank selected as cache adds one way of associativity, allowing the L2 cache to be 1-, 2-, 3-, or 4-way associative. L2 which is selected as cache is not included in the ‘C6211 memory map. The mapability of L2 blocks as addressable locations allows critical code and data to be locked into internal memory.

The enhanced direct memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the ‘C6211 memory map, the EDMA may be used to transfer data in the background of CPU operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA offers 16 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA channel is synchronized by an event to allow minimal intervention by the CPU.

TI has run extensive tests on the 'C6211 to determine how it performs with an enhanced full-rate GSM vocoder, system-level applications in ADSL, key routines in multichannel modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent.

The high L1 hit rate, combined with the flexibility of L2 memory organization, means that the 'C6211 can operate at more than 80 percent of the cycle performance of a more costly device with an ideal memory organization where all system memory is on the chip. This high degree of efficiency allows systems such as DSL client units to rely on inexpensive external memory for program and data storage, while at the same time performing high-speed number-crunching routines in real time.

The ‘C6211 was designed with TI’s low-power high-density TSC6000 ASIC Standard Cell library for low cost, while still providing 150MHz performance.

# Begin writing code for the ’C6211 today

The identical CPUs in the ‘C6211 and ‘C6201 devices allow for code to be written for the ‘C6211 using existing ‘C6000 tools. ‘C6201 code will require no modification to use on the ‘C6211. All peripheral-specific code, with the exception of the EDMA will also be able to run unchanged on the ‘C6211.

This high level of compatibility between the two processors allows for system development to begin now. By taking advantage of the ‘C6000 software tools currently available, ‘C6211 systems can have a running start for when silicon becomes available.

The ‘C6000 compiler may be used for all members of the ‘C6000 device platform. Fixed-point devices are object code compatible, so code written for the ‘C6201 may be used by the ‘C6211.

Code development for the ‘C6211 may begin using the ‘C6000 fast simulator. The simulator provides a cycle-accurate account of device performance, assuming that all on-chip memory is used for code and data. The simulator provides a good environment to learn the ‘C6000 VLIW architecture. The fast simulator may be used to model the ‘C6211 due to the high cache hit rate and the lack of memory bank conflicts for data accesses.

The standard ‘C6000 simulator may be used to incorporate peripheral support. ‘C6211 designs may be worked out in detail on the simulator prior to purchasing actual silicon, with cycle-accurate accounts of peripherals performance. The peripherals on the ‘C6211, with the exception of the EDMA are identical to those modeled by the simulator.

A ‘C6211-specific simulator is also available to model the cache performance of the device. Using this simulator, it is possible to optimize code structure and data organization to take advantage of the ‘C6211 cache structure. This simulator provides 100% cycle accuracy for both L1 and L2 cache misses. The EDMA is simulated with cycle accuracy on the ‘C6211 simulator.

For a development start in hardware, the ‘C6201 EVM may be used to understand the ‘C6000 functionality. All of the peripherals on the ‘C6211 are identical to those of the ‘C6201, with the exception of the EDMA, so the EVM is a good tool to understand how to incorporate the peripherals into a real-time system. Applications running on the ‘C6201 EVM will not be 100% cycle accurate to a ‘C6211 system, due to the difference in the internal memory architecture, but the ‘C6211 will provide approximately the same performance as the ‘C6201 operating at 150MHz.

Using these development platforms, as well as the ‘C6000 literature currently available will enable ‘C6211 systems to be completed soon after ‘C6211 silicon is made available.

# C6000 tools support

## support

‘C6000 tools are available now for use in all ‘C6000 designs. ‘C6211 specific support will be added to the development tools in early fourth quarter 1998. The ‘C6000 development tools available today are:

- ‘C6000 Simulator Software
- ‘C6000 Optimizing C Compiler/Assembler
- TMS320C6201 Evaluation Module (EVM)
- XDS510 ‘C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable

## ‘C6000 literature available

A great deal of literature is available today for the ‘C6000 devices.

- TMS320C62x/C67x CPU and Instruction Set Reference Guide
- TMS320C6201/C6701 Peripherals Reference Guide
- TMS320C6202/C6211 Peripherals Reference Guide Addendum
- TMS320C6000 Technical Brief
- TMS320C62x/C67x Programmer’s Guide
- TMS320C6x Evaluation Module Reference Guide
- TMS320C6000 Peripheral Support Library Programmer’s Reference
- TMS320C6x Assembly Language Tools User’s Guide
- TMS320C6x Optimizing C Compiler User’s Guide
- TMS320C6x C Source Debugger User’s Guide
- TMS320C6x C Source Debugger For Sparcstations

Many application notes also exist for assistance with ‘C6000 applications.

- Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation-C6000
- Guidelines For Software Development Efficiency On the TMS320C6000 VelociTI Architecture
- Implementation Of G.726 ADPCM On TMS320C62XX DSP
- Implementing V.32BIS VITERBI Decoding on the TMS320C62XX DSP
- Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201
- TMS320C6201 (Revision 2.X) to TMS320C6201B (Revision 3.X)
- TMS320C6201 Power Supply
- TMS320C6201 System Clock Circuit Example
- TMS320C6201/6701 DSP Host Port Interface (HPI) Performance
- TMS320C6X EMIF to External SDRAM/SGRAM Interface
- TMS320C6X Manufacturing With the BGA Package
- TMS320C6X Reset Circuit
- TMS320C6X Thermal Design Considerations
- Using the TMS320C6X McBSP as a High Speed Communication Port

See http://www.ti.com/sc/docs/dsps/products/c6000/index.htm for more information.