

*Migration Document*

# ***TMS320C6201 (Revision 2.x) to TMS320C6201B (Revision 3.x)***

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*REFERENCE GUIDE: SPRA450A*

*TMS320C6000 Digital Signal Processing*

*Digital Signal Processing Solutions  
September 1998*



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## Contents

<b>Abstract</b> .....	<b>7</b>
<b>Product Support</b> .....	<b>8</b>
World Wide Web .....	8
Email.....	8
<b>Core Voltage (CVdd)</b> .....	<b>9</b>
<b>Data Memory</b> .....	<b>9</b>
<b>PLL Circuit</b> .....	<b>10</b>

## Figures

Figure 1: TMS320C6201B PLL Circuit.....	10
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## Abstract

Samples of the Texas Instruments (TI™) TMS320C6201B DSP will be available in the second half of 1998, with volume production starting at the end of the year. The TMS320C6201B revision is manufactured using a 0.18-micron process compared to the currently available revision 2 that uses a 0.25-micron process. The use of a smaller process for the TMS320C6201B DSP will lead to significantly lower power dissipation as well as lower cost. The new data memory structure will allow simultaneous word accesses by both sides of the CPU and the DMA during a single cycle.

This document is intended to enable TMS320C6201 designers to anticipate the migration of their design to the TMS320C6201B and take advantage of the benefits of this revision.

The following lists the changes implemented by the TMS320C6201B compared to the TMS320C6201:

- ❑ Core voltage changed from 2.5V to 1.8V  
The new core architecture will be run at a lower voltage to provide less power consumption by the device.
- ❑ Dual blocks of Internal Data Memory  
64k-byte Data memory now divided into two 32K-byte blocks, with four 4K-byte banks per block.
- ❑ Voltage input to PLLV changed to 3.3V

The PLL circuit will be powered by the I/O voltage supply, rather than by the core voltage supply.



## Product Support

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## Core Voltage (CVdd)

The voltage level of the 'C6201 core has been changed from 2.5V to 1.8V. A new process will be used to manufacture the revision 3 silicon, which will reduce the physical size of the architecture. This change will allow more space for additional memory and peripherals on the device, and will also allow for less power consumption.

To provide a forward-compatible design that will function correctly for both revision 2 and revision 3, the core power supply must be designed to allow for an output voltage of either 2.5V or 1.8V. This may be accomplished by providing jumpers on the board, which select biasing resistors or capacitors for a linear regulator, or by providing jumpers to select a binary input to a switching regulator.

## Data Memory

The internal data memory is now divided into two 32K-byte blocks, ranging from 0x80000000 to 0x80007FFF and from 0x80008000 to 0x80010000. With the division of the internal data memory into two blocks on revision 3 silicon, internal data may be accessed from different blocks without conflict, regardless of the banks accessed. Each block still contains four banks of 16-bit halfwords. Within a block the functionality is the same as on revision 2 silicon: both sides of the CPU (A or B) and the DMA may access different banks without conflict.

