Teaching DSP through the Practical Case Study of an FSK Modem

Authors: G. Baudoin, F. Virolleau, O. Venard, P. Jardin

ESIEE, Paris

September 1996
SPRA347

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

Contents

Figures

Teaching DSP through the Practical Case Study of an FSK Modem

Abstract

This paper describes the teaching of Digital Signal Processors (DSP) through classical lectures and a practical case study where students have to implant a real time simplified FSK modem on a TMS320C50.

Product Support

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Students level

This teaching is delivered to ESIEE (French Grande ecole) students 4 years after baccalaureat, and more precisely to students of the Digital Communications specialization. These students have already received lectures in Digital Signal Processing (130h) and in Digital Communications (50h). The same approach could be used with slight modifications to postgraduate or undergraduate students with electronic background.

Organization and evaluation of the teaching

This teaching is 26 hours long. It consists of 8 hours lectures and 18 hours laboratories.

Lectures

During the 8 hours lectures, 3 topics are developed:

- The general principles of Digital Signal Processors
- Fixed and floating point arithmetic
- Description of the TMS320C50 processor

Laboratories

The laboratories are dedicated to the study and the development of a simplified FSK modem on a fixed point DSP TMS320C50. During the laboratories, the students work in teams of 2 or 3 persons and they are supervised by two lecturers.

Evaluation

The evaluation is done by averaging 2 marks: the mark of the practical case study (report and demonstration) and the mark of a 2 hour long written examination.

Documentation

The given documentation includes the copy of the lectures slides, the TMS320C50 user's guide and the instructions for the laboratory.

Equipment used during the case study

For each student group, the equipment is consists of a PC computer with Matlab, an evaluation board for The TMS320C50 (EVMC5X) with the associated software (dspa, dspInk, evmc5x), and an oscilloscope.

The evaluation board includes a TMS320C50 DSP, memory, interface with the PC bus, and chips for digital to analog and analog to digital conversion. This chip is connected to the standard serial port of the DSP.

Description of the topic of the case study

The work consists of studying and implanting a simplified V23 FSK modem. The data interface with the PC is not required. That is to say that the modem always sends the same data sequence so it is easy to synchronize an oscilloscope on the modulated signal. The choice of the data sequence is free.

The bit rate Fb is 1200 bits per second. The Frequency Shift Keying modulation sends a frequency F1=2100Hz for a bit equal to I and F0=1300 Hz for a bit equal to 0.

The students must realize one continuous phase modulator, one band-pass emission filter, one non-coherent demodulator, and (but this is not mandatory) a clock recovery and a threshold detector.

A program for input and output of analog signals with the analog interface on the EVM board is given to the students. This program allows to test the DSP board, but only the output of the analog interface is necessary for the modem. The sampling frequency is 9600 Hz, which is sufficient for the spectrum of the modulated signal. The converter works with 14 bits.

Matlab is used to calculate a table of sine values and the filter coefficients.

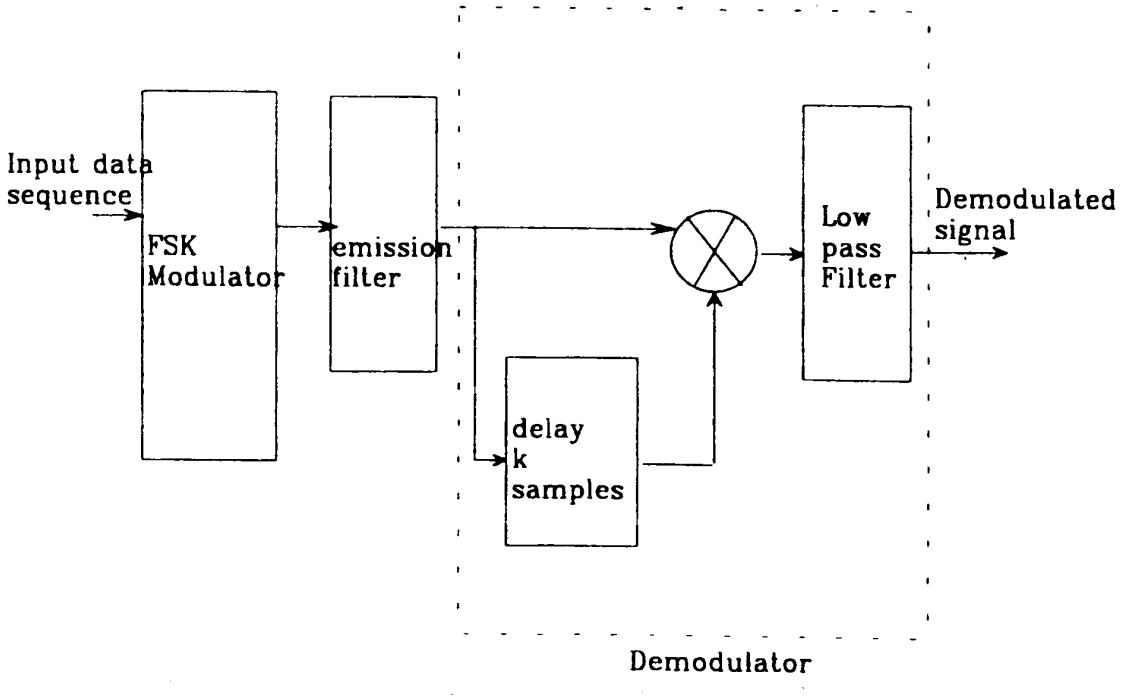
In practice, there are 4 steps in the work:

- Realization of a sinusoidal frequency generator of arbitrary frequency,
- Realization of a FSK modulator,
- Realization of the emission filter,
- Realization of a demodulator.

At each step, students can verify their work by observation of signals (pure sinusoid, modulated signal, filtered modulated signals, demodulated signal) on the oscilloscope.

Figure 1 represents the complete system.

Figure 1. FSK modem to implant on the DSP



Arbitrary frequency sinusoidal generator

Even if for the modem only 2 frequencies are necessary, the students are asked to develop a sinusoidal frequency generator of arbitrary frequency.

The required precision on the sinusoids amplitudes is 1% of the full-scale amplitude. The proposed generation method is direct lookup table method. It consists in reading the sine values in a table of N values, the phase of the signal being incremented at the adequate rate.

It is supposed that the cycle time of the DSP is perfectly fixed and equal to T_c.

The sine values in the table correspond to N phases Ψi that are uniformly distributed between 0 and 2π.

$$\Psi_i = \frac{2i\pi}{N} \qquad i \in [0, N-1]$$

If sin_deb is the first address of the sine table, sin(Ψi) is stored at address: sin_deb+i. The value I is called the index in the table.

Suppose F is the desired frequency. The signal to generate is x(t), with:

$$x(t) = A \sin(2\pi Ft) = A \sin((\Phi(t))$$

and $t = nT_e$ where T_e is the sampling period. Because of Shannon's theorem, I/T_e is chosen greater than 2F.

$$\Phi(nT_e) = \Phi_n = 2\pi FnT_e = \Phi_{n-1} + 2\pi FT_e$$
$$\Phi_n = \Phi_{n-1} + \Delta\Phi_F$$
$$\Delta\Phi_F = 2\pi FT_e$$

Generating the sinusoid at the frequency F, consists in calculating Φ_n modulo 2π, recursively by the preceding formula and then reading the sine value of the closest phase Ψ_i present in the sine table. This sine value is then sent to the digital to analog converter

As Φ_{n-1} belongs to the interval $[0,2\pi]$ and $\Delta\Phi F$ is smaller than π, the recursive calculation of the phase Φ_n modulo 2π, supposes to compare the phase Φ_n with the value 2π and when the phase becomes greater that the limit value 2π, to suppress 2π from Φ_n.

It is possible to suppress the time consuming comparison tests with 2π. This can be achieved by using the circularity of 2's complement representation of numbers. The method is described in the following lines.

Φ_n is represented in the DSP by an integer number on 16 bits, noted $I_{\Phi n}$. The minimum value of Φ_n (which is 0) is coded by -2^{15} , and the maximum value (which is $2\pi n-2^{15}\pi$) by $2^{15}-1$. For calculation, Φ_n is stored in the Most Significant Bits of the accumulator. When some positive value is added to Φ_n corresponding to a result superior to $2^{15}-1$, the circularity of the 2's complement representation gives the result modulo 2^{16}. So, the overflow test is unnecessary.

Calculations are done on $I_{\Phi n}$ that is linked to Φ_n by:

$$I_{\Phi n} = \frac{2^{15}\Phi_n}{\pi} - 2^{15}$$

For a table size equal to N, the phase increase between successive table points is $2\pi/N$ and corresponds to an increase in I-, equal to $2^{16}/N$.

For a frequency F, the phase increase between successive points of the generated sinusoid is $2\pi FT_e$, which corresponds to an increase ΔI_Φ. On $I_{\Phi n}$ equal to $2^{16}FT_e$ rounded to the closest integer.

For a given integer value $I_{\Phi n}$, the table index is equal to $i = N\, I_{\Phi n}\, 2^{-16} + N/2$. Generally N is a power of 2 and i is obtained by a simple shift of I_Φ.

The precision of the generated frequency F is given by the precision of the representation of $2^{16}\ Ft_e$, which is rounded to the closest integer. So the precision dF on F is given by:

$$|dF| < 2^{-17}\, F_e$$

The errors on the amplitudes of the generated sinusoid are introduced when a phase Φ_n is rounded to the closest Ψi. To obtain an absolute precision dx, it is sufficient that the amplitude difference between 2 successive sine values of the table be smaller than 2 dx. The precision on the amplitudes is worst for the values closed to zero where the derivative is maximal. A sufficient condition for an absolute precision dx is

$$N > \frac{A\pi}{dx} \text{ where A is the maximum amplitude.}$$

Of course, it is possible to only store in the table sine values corresponding to phases uniformly distributed between 0 and π or $\pi/2$. But this will increase the calculation time.

Special case of a limited number of frequencies

In the case of the FSK modem, there are only 2 possible values for F: F_0 and F_1, and the problem can be simplified.

The size N of the table can be calculated in order that the reading index increment is an integer for both frequencies. This condition can be written as:

$$\Delta\Phi_0 = 2\pi F_0 T_e = k_0 \frac{2\pi}{N} \quad \text{with } k_0 \text{ integer}$$

$$\Delta\Phi_1 = 2\pi F_1 T_e = k_1 \frac{2\pi}{N} \quad \text{with } k_1 \text{ integer}$$

Which is equivalent to :

$$\begin{cases} NF_0 T_e = k_0 \\ NF_1 T_e = k_1 \end{cases}$$

The smallest possible value of N satisfying this condition is N = 96, for the constant used in the case study.

In that case, the only errors on the precision of the sine values at the sampling times, are due to the limited precision of the digital to analog converter.

The precision of the generated frequency is connected to the precision of the sampling frequency.

To generate the frequency F_0 (respectively F_1), the sine table is read with an integer step index equal to k_0 (resp. k_1). In that case it is necessary to test if the reading index has reached the end of table. A circular buffer of size N = 96 is read with a step equal to k_0 or k_1.

Realization of the FSK modulator with continuous phase

When the student knows how to generate a sine signal of a given frequency it is easy to implant a FSK modulator.

At the bit rate Fb of 1200 Hz, an interruption is sent to the DSP. The DSP reads a new data in the periodical data sequence. If the bit is equal to 0, the phase increment $\Delta\Phi$ is set to $\Delta\Phi_0$, if the bit is equal to 1 the phase increment is set to $\Delta\Phi_1$, with:

$$\Delta\Phi_0 = 2\pi F_0 T_e$$

$$\Delta\Phi_1 = 2\pi F_1 T_e$$

In both cases, the samples of the modulated output signal x_n are calculated at each sampling period T_e by:

$$x_n = \sin(\Phi_n)$$

$$\Phi_n = \Phi_{n-1} + \Delta\Phi$$

$\Delta\Phi_0$ corresponds to a step $\Delta i = k_0$ in the reading index i, and $\Delta\Phi_1$ to a step $\Delta i = k_1$. Calculations are done on the reading index i_n:

$$i_n = i_{n-1} + \Delta i$$

The bit rate Fb is generated using the timer of the C50. The period register PRD of the timer is loaded with the value Tb/Tc -1 rounded to the closest integer. Here Tb is equal to 1/1200 s and Tc=50 ns, so the value of PRD is equal to 16666.

The obtained bit rate is equal to 1199,976 Hz.

The x_n output samples are sent to the digital to analog converter at the sampling rate $1/T_e$. This sampling rate is given by the clock on the serial port where the DAC is connected. At each interruption XINT (transmit interrupt from the serial port), a new sample X_n must be written to the DXR register (transmit register of the serial port).

Calculation and implantation of the emission filter

The emission filter must satisfy the following constraints:

- From 400 to 3000 Hz, attenuation smaller than 0.5 dB
- From 0 to 200 Hz and from 3400 to 4800 Hz, attenuation superior to 30 dB.

The filter is calculated using Matlab.

An FIR filter is calculated with the Parks McClelland algorithm (routine remez in Matlab). An order 63 is sufficient for coefficients coded on 16 bits.

The filter coefficients are coded on 16 bits integers with Matlab. As the maximum absolute value of coefficients is smaller than 1, the chosen format is Q15 (15 bits after the coma).

If b is the vector of the filter coefficients, the coded coefficient vector bc is obtained by the Matlab command:

bR = round(b*2∧15);

A file containing the coded coefficients written as integer is saved using the format of a COFF file with the << data >> directive.

The filter is implanted on the DSP using the MACD type instructions.

The modulated signal x_n is filtered and sent to the DAC, it can then be observed on the oscilloscope.

Realization of the demodulator

The principle of the asynchronous demodulator is drawn in figure 1.

The received signal s(n) is delayed by an integer number of sampling periods k. The delay k must be smaller than the number of samples in a bit (6 here). the received signal s(n) is multiplied by the delayed signal s(n-k), the product signal is noted v(n) = s(n) s(n-k).

The product signal v(n) is filtered by a low pass filter to eliminate the harmonic frequencies generated by the product.

To understand the method, suppose, that the time samples n and n-k belong to the same bit period corresponding to the frequency F_0, then:

$$s(n)s(n-k) = A^2 \sin(2\pi F_0 n T_e)\sin\left(2\pi F_0 (n-k) T_e\right)$$

$$s(n)s(n-k) =$$

$$\frac{A^2}{2}\left[\cos(2\pi F_0 k T_e) - \cos(4\pi F_0 n T_e - 2\pi F_0 k T_e)\right]$$

The first term is a function of k only, its does not depend on time as long as n and n-k belongs to the same bit. The second term should be eliminated by the low pass filter.

So, after the low pass filter, as long as n and n-k belongs to the same bit, the filtered signal will correspond to the constant $\cos(2\pi F_0 k T_e)$ or to the constant $\cos(2\pi F_1 k T_e)$ depending on the value of the received bit.

To maximize the efficiency of the demodulator, k must be chosen in order to maximise the difference d(k):

$$d(k) = \left|\cos(2\pi F_0 k T_e) - \cos(2\pi F_1 k T_e)\right|$$

Matlab is used to construct the above function d(k) and to find its maximum for k smaller than 8 (8 is the number of sample by bit).

The best values are k = 7, then k = 4.

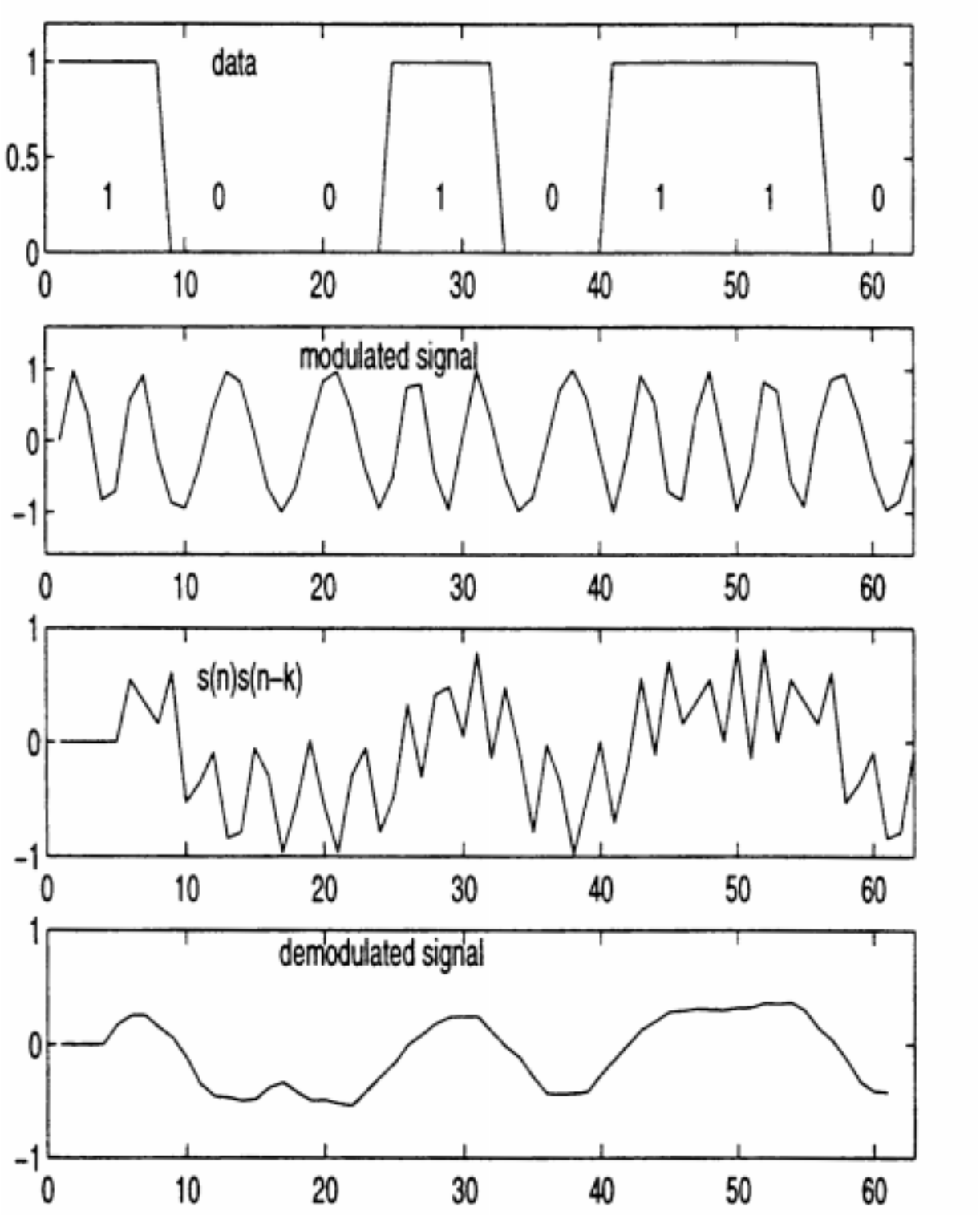
The value k = 4 is used in the demodulator, because it allows longer time intervals corresponding to n and n-k on the same bit period.

The low pass filter is a simple IIR filter (order 3 is enough) with a cutoff frequency around 1200 Hz (bit rate).

The demodulated signal is observed on the scope and the constant values are compared with the original data sequence.

Figure 2 represents the different interesting signals: the data sequence, the modulated signal, the output of the product s(n)s(n-k) and the demodulated signal.

Figure 2. Data sequence, modulated signal, output of the product s(n)s(n-k) and demodulated signal



Organigram of the complete system

Initialization

Initialization of the DSP: wait cycles,

Interrupts, serial port, timer.

Initialization of the DAC.

Transfer of data tables (sine table, filter coefficients, data sequence to transmit) from program memory to data memory.

Initialization of data to zero i_n, xn…

Initialization of pointers for table reading.

Enabling timer interrupt.

Main program

Waiting for the first timer interrupt.

Enabling the serial port interrupt.

beg:

modulation:

calculation of in the sine table index.

reading of the sine table to obtain the modulated sample xn.

filtering of xn by the emission filter -> s(n).

demodulation:

calculation of v(n)=s(n) s(n-k).

filtering of v(n) by a low pass filter.

writing of the demodulated value in memory OUTDEMOD.

waiting for the serial port interrupt.

goto beg

Timer routine (TINT)

saving context.

reading next bit in the arbitrary data sequence

to transmit, at the address given by the pointer

data_ptr.

test the bit:

if bit=0, $\Delta i=k_0$

if bit=l, $\Delta i=k_1$

test the position of the read bit in the data

sequence:

if it is not the last bit, increment

data_ptr by 1.

if it is the last bit, load data_ptr with

the address of the beginning of the

data sequence.

restoring context, enabling interrupts.

Serial port transmit routine (XINT)

saving context.

transferring the memory word OLJTDEMOD in the register DXR, to send the demodulated signal to the DAC.

restoring context, enabling interrupts.

Interest of this case study

The interests of such a case study are of 2 types: technical acquisitions and motivation of the students.

Motivation of students

In a limited amount of time, the students can realize a real-time actual system, from which they can observe different signals on an oscilloscope. This work allows them to synthesize several topics in digital signal processing and to learn new concepts on digital signal processors and real time systems.

Technical interests (acquisitions)

The students already know the theory of FSK modulator and demodulator, of digital filtering, and of general signal processing. But their only practical experience is computer simulations with SPW. Here, the technical acquisitions are:

- Training on TMS320C50 in a real environment they use the CALU, different types of addressing, they manipulate interruptions, they initialize the processor, they use the timer to generate the 1200 bits by second clock, they use the standard serial port to which the analog concerter is connected, they can use the circular buffer.
- Fixed point arithmetics: students can generate arbitrary frequency sinusoides using the circularity of the 2'complement representation of number. They also study the limited precision of calculation for digital filters with fixed point representation of coefficients and signals.
- Frequency generation techniques by table lookup.
- Continuous phase FSK modulation and demodulation implantation.
- Implantation of digital filters with fixed point DSP, comparison of FIR and IIR, using MAC instructions or circular buffers.