TMS320 DSP
DESIGNER'S NOTEBOOK

C54x Extended Addressing

APPLICATION REPORT: SPRA184

Jim Larimer
Digital Signal Processing Products
Semiconductor Group

Texas Instruments
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TEXAS INSTRUMENTS

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CONTACT INFORMATION

US TMS320 HOTLINE	(281) 274-2320
US TMS320 FAX	(281) 274-2324
US TMS320 BBS	(281) 274-2323
US TMS320 email	dsph@ti.com

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C54x Extended Addressing

Abstract

In some applications, there is a need to store and have easy access to multiple algorithms. This increases the program memory requirement beyond 64K words. The TMS320LC548 and TMS320LC549 provide direct support for an extended address capability for program memory space. This extended address capability supports a total of 4M 16-bit words if the on-chip RAM (32K words) is mapped to program space as a home page. The program space is increased to 8M words if the on-chip RAM is mapped to data space only. This document describes how to implement this and what cycle overhead will be created.

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Design Problem

In some applications, there is a need to store and have easy access to multiple algorithms. This increases the program memory requirement beyond 64K words. How can I do this and what cycle overhead will this create?

Solution

The TMS320LC548 and TMS320LC549 provide direct support for an extended address capability for program memory space. This extended address capability supports a total of 4M 16-bit words if the on-chip RAM (32K words) is mapped to program space as a home page. The program space is increased to 8M words if the on-chip RAM is mapped to data space only. Please see the TMS320LC54x technical reference guide for additional details.

All changes in program control to locations specified by the extended addressing pointer are unconditional. This program discontinuity instruction can be delayed.

Standard unconditional far branch example:

far goto	extpmad	algebraic
FB	extpmad	mnemonic

This instruction passes control to the program location specified by the extended program memory address (extpmad). This value can be any value between 0 and 7FFFFFh.

Delayed unconditional far branch example:

far dgoto	extpmad	algebraic
FBD	extpmad	mnemonic

This instruction passes control to the program location specified by the extended program memory address (extpmad). This value can be any value between 0 and 7FFFFFh. Since this is delayed, the two 1-word or one 2-word instruction following the branch is fetched from program memory and executed.

Extended program address branch/call overhead

The table below lists the associated instruction cycle count. Note that there is no overhead associated with the far branch and far call instructions. There is a one cycle delay associated with the far return.

Table 1. Associated Instruction Cycle Count

Instruction	Standard cycle count	Delayed cycle count
Branch	four	two
Far Branch	four	two
Call	four	two
Far Call	four	two
Return	five	three
Far Return	six	four