Application Report
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Interfacing the Embedded 12-Bit ADC in a TMS570LS20x/10x Series Device

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ABSTRACT

The Texas Instruments Hercules™ ARM® Safety Microcontrollers TMS570LS20x/10x series products have two 12-bit analog-to-digital converters (ADC). This document provides the device configuration and layout recommendations to achieve the best performance of the embedded ADC, including: layout requirements on power and ground, decoupling/bypass capacitor requirements on voltage reference pins and power pins, typical circuit and requirements in front of ADC input channel, recommendations on ADCLK configuration, PLL settings and trigger signal to achieve the best ENOB, how to do calibrate and compensate, and how to use over-sampling to improve resolution.

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1 Description

Two 12-bit ADC cores and 24 ADC input channels are implemented in the TMS570LS20x/10x devices. Figure 1 illustrates the connection of the two A/D converter peripherals on the TMS570LS20216 device.

- Each ADC supports 16 channels
- Each ADC has 8 dedicated channels
- Each ADC has a dedicated pin for event trigger
- Two ADC cores share 8 channels
- The references are shared between the two cores

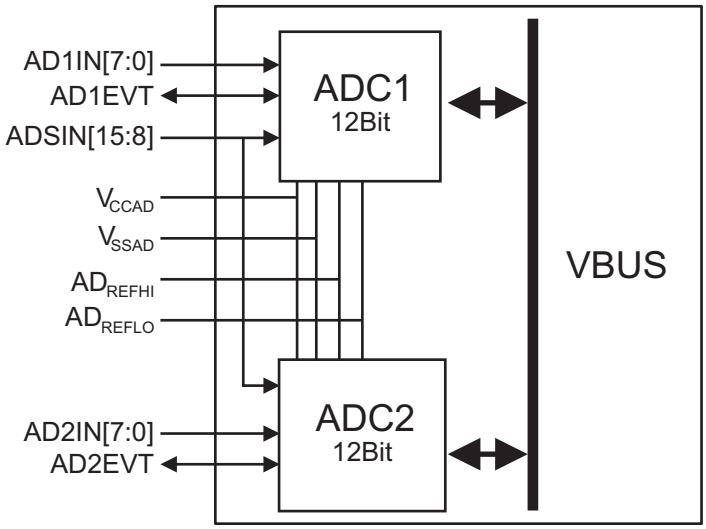

Figure 1. Channel Assignments of Two ADC Cores

2 Circuit Design and Layout Requirement

2.1 General Requirements

The most important thing of an ADC is to protect the analog part from excessive digital noise. The following section states the general recommendations to use the TMS570LS20x/10x embedded ADC.

First of all, the board should be partitioned into 'Analog Region' and 'Digital Region'. The ADC inputs, VCCAD, VSSAD, AD_{REFLO} and AD_{REFHI} are only allowed to route in the 'Analog Region'. The digital signals and the ADC Event triggers are only allowed to route in the 'Digital Region'. If the digital signals and analog signals are mixed up, the digital noise will couple to the analog signal. This may generate 'random noise', offset and gain errors on the conversion result. If you have to route a digital signal in the 'Analog Region', please try to make the analog signals and the digital signals perpendicular to each other to minimize the coupling.

Second, ground strategy is also very important. A spit ground plane can be used to prevent digital logic ground currents from contaminating the analog signals. However, it should be used only when necessary because it introduces many potential risks. If your board has some very noisy components or huge current consumption components, for example, switching power supplies and MOSFET drivers for the motor, you need to split your ground plane or use star ground connection carefully to reduce the noise coupling to AD circuit. You might also need to shield the noisy components to prevent field coupling in those cases too. However, splitting the ground plane under TMS570LS20x/10x devices is not required due to the following reasons:

Reason 1 - DC current:
In a 3.3-volt system, the least significant bit (LSB) of a 12-bit ADC represents 3.3V/4096 = 0.8mV. If the DC drop on the ground plane from external analog input to the TMS570 device is less than one LSB, it is not necessary to split the ground plane to prevent the DC current.

DC current spreads from the source to the destination evenly on the ground plane. The largest DC current for a TMS570LS device is the V_{CC} current. The worst case current is around 400mA. Look at the ground plane shown in Figure 2. This component placement is not optimized because the IC that consumes most of the power is far away from the power supply.

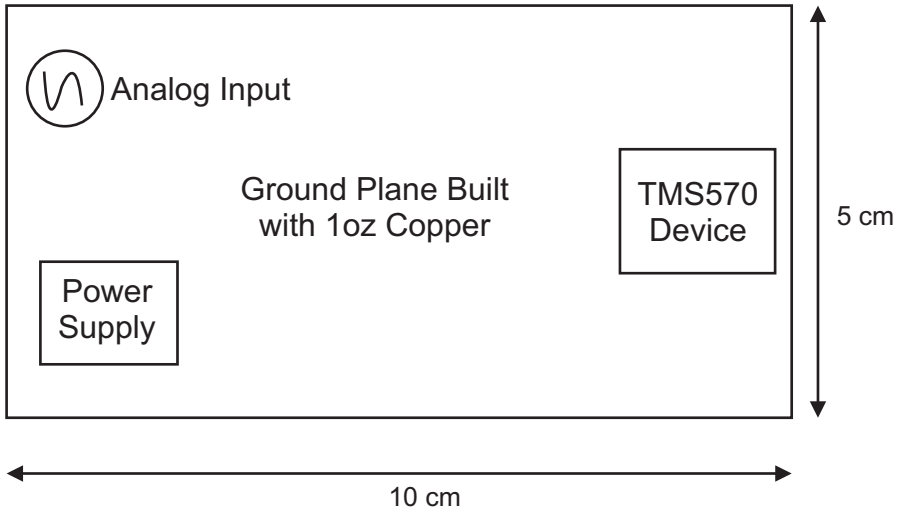

Figure 2. Ground Plane Example

The resistance of a 1oz copper ground plane is about 0.5mΩ/●, where ● represents a square area with equal length and width. The ground plane in Figure 2 looks like a 2:1 (length: width) rectangle. The worst case voltage drop on the ground plane is around 0.5mΩ/● x 2● x 400mA = 0.4mV, which is only half LSB. In a real case, after you optimize your power delivery and your component placement, running at normal voltage and room temperature, the voltage drop on the ground plane due to the TMS570LS20x/10x itself should be less than half LSB.
Here, only the power consumed by TMS570LS20216 itself is considered. If your system includes some high current device, for example, a motor driver consumes current in the order of an 'Amp', you need to split your ground plane to avoid DC voltage drop on the ground plane

Reason 2 - High frequency current:
Due to the skin effect (to minimize the impedance in the path), the high frequency return current flowing through the plane is restricted to a narrow area underneath/above the PCB trace carry the outgoing current. The equations to calculate the current distribution on an infinite and finite ground plane can be found in [1]. Figure 3 is a calculation example (Left part shows the setup while right part shows the calculated current distribution):

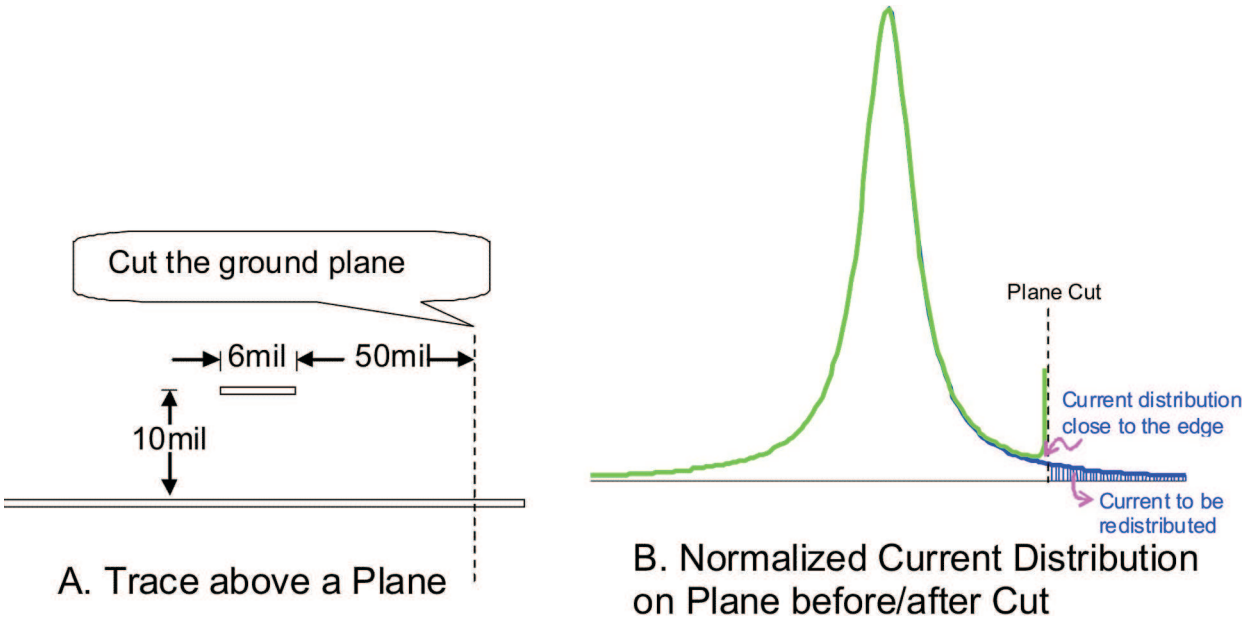

Figure 3. Current Distribution on an Infinite and a Cut Ground Plane

Since almost all the current flows underneath/above the trace, splitting the ground doesn't help much to reduce the high frequency coupling between analog and digital circuits.

Splitting the ground plane should be done only when you know where the ground current flows. If you have to split the ground plane, please follow two important rules [2]:

- Do not run any signal across the gap of a split ground plane. The analog ground and the digital ground should be connected at one point and all the traces commuting between the analog and digital region should be routed over this bridge point as shown in the left part of Figure 4. By doing this, the current returns directly underneath/above each trace and the current loop area is minimized. A high frequency signal cross the gap like the right part in Figure 4 can generate both signal integrity problems (discontinuities) and EMI problems. Even if it is low frequency or DC signal, it might also carry high frequency noise due to the on board and on-chip coupling.

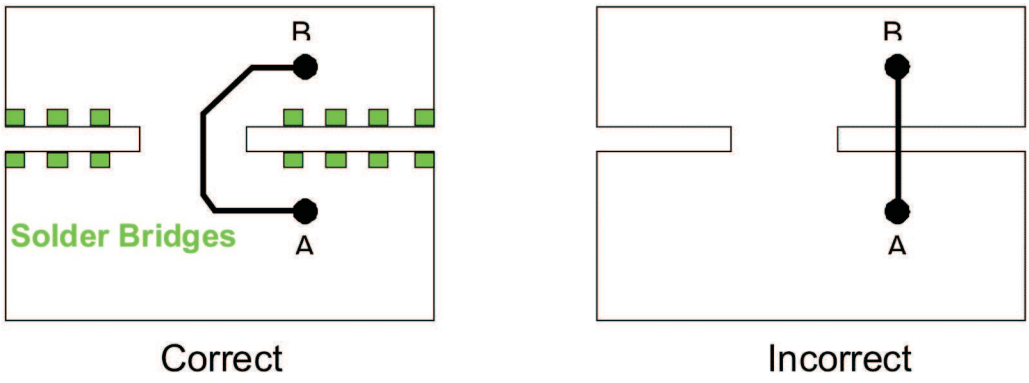

Figure 4. Signal Traces Crossing the Gap of Ground Plane

- Please reserve a few solder-bridges along the gap (every half inch) of the ground plane as shown in the left part in Figure 4. You can connect them in case the ground gap brings problems into your system.

2.2 Power and Reference Voltage

VCCAD and VSSAD are not truly analog power and grounds. They contain digital noise generated during conversion. VSSAD is also connected to V_{SS} through p-substrate inside the IC, the high frequency V_{SS} current in the digital/core area can also follow through this VSSAD pin to the board ground. A minimum 100 nF decoupling capacitor should be placed between VCCAD and VSSAD before they reach the power/ground plane as shown in Figure 5.

VREFHI and VREFLO are the reference voltages for the conversion. They should be extremely clean. Random noise on these two pins will lead to random noise on the conversion result. With synchronized (with the clock inside device) noise presenting on these two pins, the conversion result looks 'stable' but has offset and gain errors. A minimum 100nF decoupling capacitor should be placed between them before they reach the power/ground plane as shown in Figure 5. Do not share VIAs between VSSAD and VREFLO or between VCCAD and VREFHI because the self-inductance of the common VIA couples digital noise to the voltage reference pins.

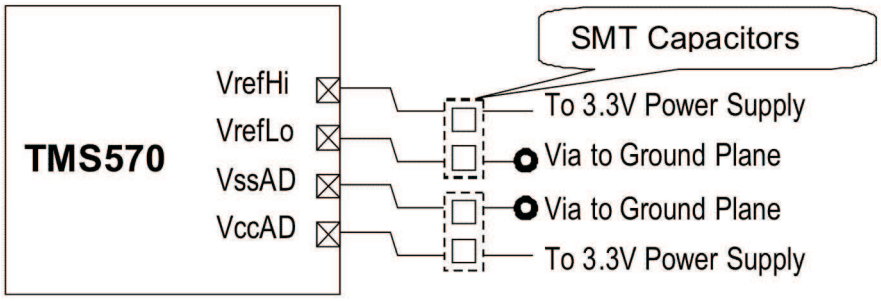

Figure 5. Power and Reference Voltage Layout Strategy

2.3 Input Channel

A typical input stage of the ADC input includes a low pass filter, and an OP-AMP as shown in Figure 6. You can combine the low pass filter and OP-AMP together.

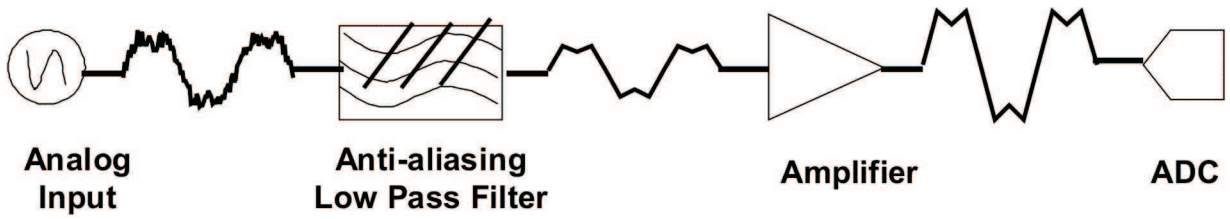

Figure 6. ADC Input Strategy

2.3.1 Anti-aliasing Low Pass Filter

Usually, the analog input carries all kinds of noise (e.g.,: FM noise, cell phone band noise and other spurious signal). The user should have some prior understanding of the nature of the input signals to be measured, for example, the minimum or maximum frequency. Then, a filter can be designed to improve the signal to noise ratio (SNR).

On the other side, the highest ADC sampling rate on TMS570LS20x/10x devices is around 1MSPS. The Nyquist frequency is half the sampling frequency. Any signal/noise beyond the Nyquist frequency can be considered as 'disturbance' to the system and should be filtered before sampling.

To protect the analog input signal integrity, the capacitor and inductor used in the filter must be screened carefully. The capacitance of the capacitor must not change across the voltage, frequency and temperature range (NPO capacitor). The inductance of the inductor must not change across the current, frequency and temperature range too. The change of capacitance or inductance will result in harmonic distortion to the system and degradation of the effective number of bits (ENOB).

2.3.2 Op-Amp

Figure 7 shows the equivalent circuit of an ADC input channel for TMS570LS20x/10x devices. The ADC loading changes before/after sample switch closes. To protect the analog input from changes in ADC loading, especially at sampling frequency greater than 100KSPS, an Op-Amp is recommended. The operational amplifier (OP-AMP) can provide the following benefits to the system:

- Isolate the analog input and ADC loading
  - High input impedance
  - Low output impedance
  - Protects the analog input from changes in ADC loading
- Charge sample and hold networks effectively
- Provides gain/offset and level shifting
- Configure as filters

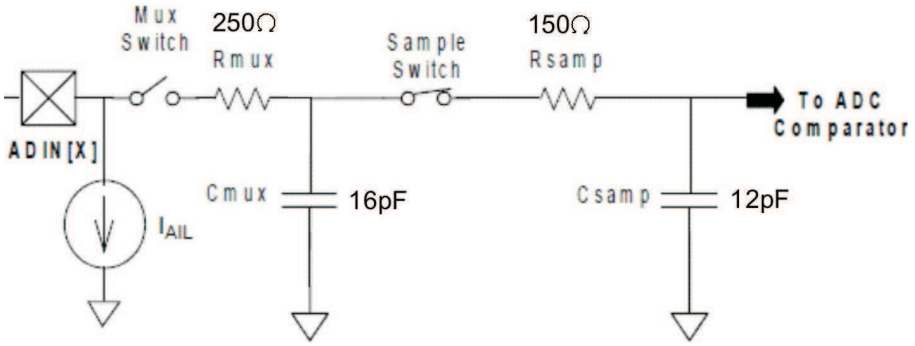

Figure 7. MibADC Input Equivalent Circuit

The OP-AMP is not a must. If the input frequency and sampling frequency is low, or the input signal driving strength is strong, the OP-AMP can be removed. Once the OP-AMP is removed, the circuit looks like Figure 8. Two offsets must be considered in this case [3]:

- Offset caused by charge sharing between C_{ext} and the ADC sampling capacitor.
- Offset caused by re-charging the C_{ext}.

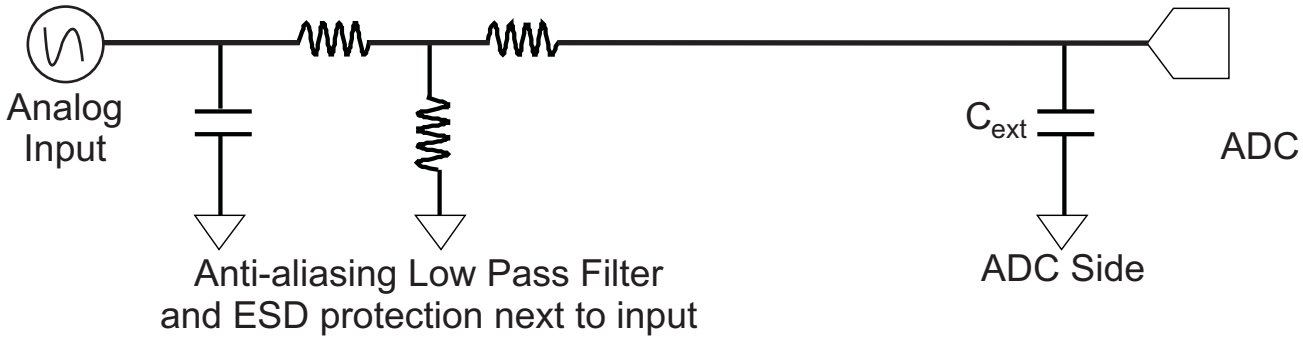

Figure 8. ADC Input Passive Circuit (No OP_AMP)

Please refer to the TMS570LS20216 Technical Reference Manual [3] about how to estimate these offsets and to know if OP-AMP is a must in your system. An alternative way is to run a test on the board:

1. Bypass the Op-Amp.
2. Provide a DC voltage to the analog input.
3. Run 10 ADC conversions with the desired sampling rate and acquisition time.
4. If the 1st conversion is more than 1LSB greater than the other 9 conversions, you might need an OP-AMP (Takes too long to charge the C_{ext}).

5. Run 10 ADC conversions with the desired sampling rate and twice the acquisition time.
6. If average value of step V is more than 1LSB greater than the average of step III, you might need an OP-AMP (C_{ext} is not big enough to share charge with the sampling capacitor).
7. If your application tolerates the uncertainty in Step 4 and Step 6, you don't need an OP-AMP.

3 Device Configuration

3.1 ADCLK and PLL Settings

According to the device datasheet, the ADCLK can run at any frequency lower than 30 MHz. The ADCLK is generated by dividing down the input clock to the ADC module, which is the VCLK. If divided by 1, the ADCLK always presents in the ADC module, running at VCLK frequency. If divided by any other value, the ADCLK only presents in the ADC module when there is on-going AD conversion or pending AD conversion. Therefore, to save the power, reduce the emission and improve the ADC accuracy, please divide down the VCLK at least by 2 to generate the ADCLK.

The sampling and conversion take place at the edge of ADCLK. The phase jitter of ADCLK leads to the sampling jitter error as shown in Figure 9, resulting in an overall degrading in SNR. This can be a serious problem, especially for high input frequency (e.g., 100 KHz). The ADCLK is generated from VCLK, which can be traced back to the PLL output. There are two PLLs in the device. To achieve a better ADC dynamic performance, the PLL setting must be chosen carefully.

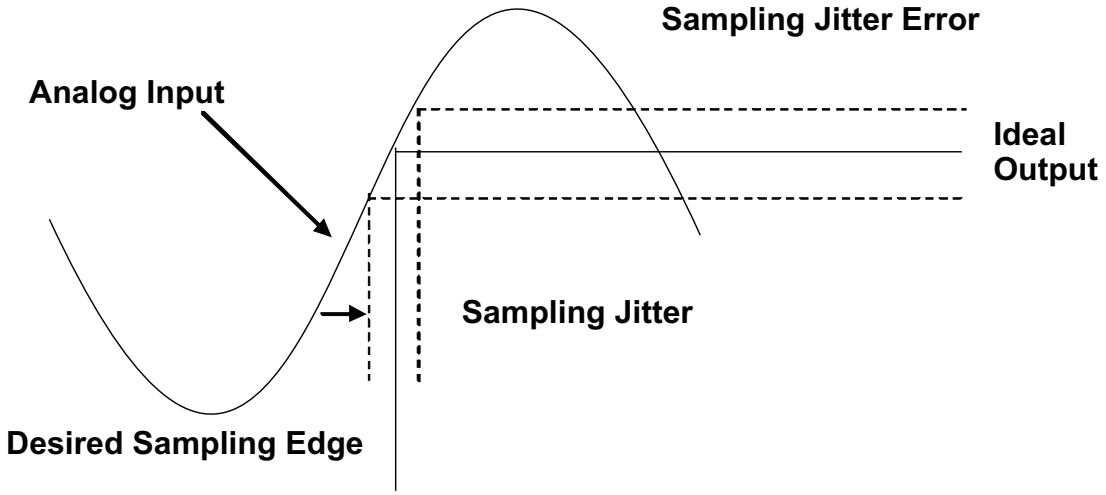

Figure 9. Effect of Sampling Jitter

Figure 10 shows the block diagram of the FMzPLL (clock source 1). **NR** is the input clock divider, which controls the frequency of the adjust pulse. A lower **NR** value means the error in PLL frequency is compensated faster, resulting in less jitter. The adjust pulse will go through a low pass filter (**LF**) before it applies to the VCO. The cut-off frequency of this low pass filter is controlled by the **BWADJ** field in PLLCTL2 register. A lower **BWADJ** value results in less jitter. During normal operation, any **BWADJ** less than 7 will be treated as 7. A Larger **NF** also generates less jitter.

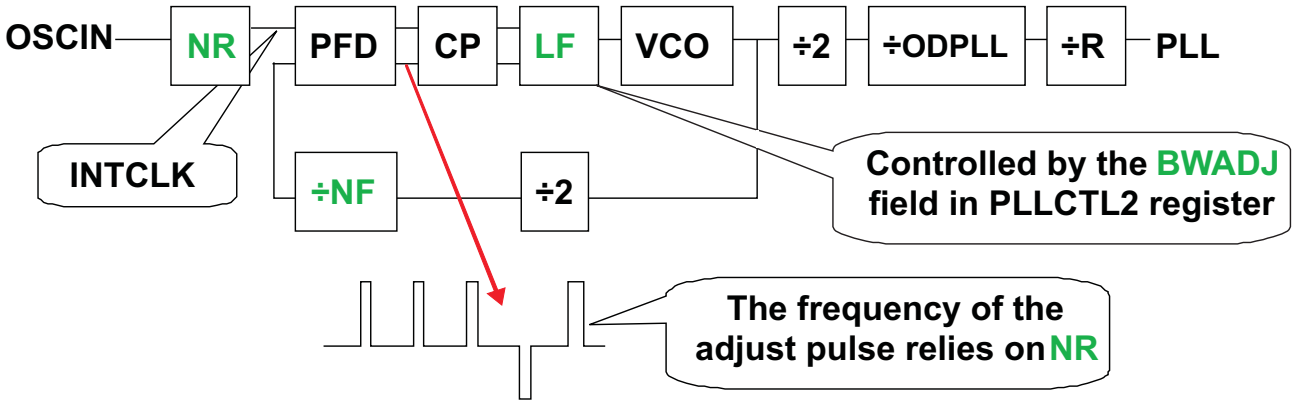

Figure 10. FMzPLL Block Diagram

The FPLL (clock source 6) block diagram is shown in Figure 11. It is similar to the FMzPLL block diagram. However, the upper frequency limit for INTCLK in the FPLL is much higher than the FMzPLL. Therefore, FPLL has less jitter than FMzPLL. To achieve the best ADC dynamic performance (SNR, ENOB etc.), the system should run on FPLL and the input divider **NR** of FPLL should be set to 1.

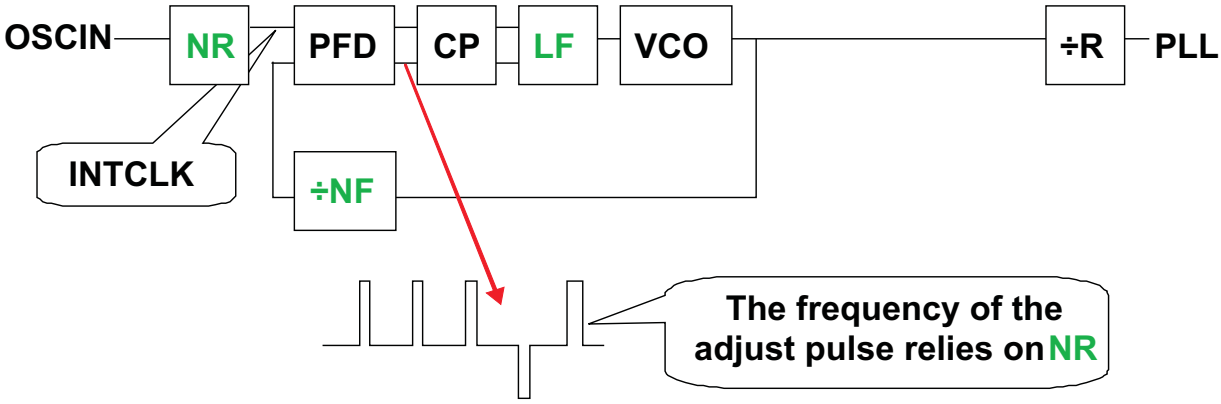

Figure 11. FPLL Block Diagram

Table 1 shows the ADC dynamic characterization on one 144-pin TMS570LS20106 sample. With100 KHz input signal, using clock source 6 (FPLL) can achieve a higher ENOB. With 10 KHz input signal, the clock source setting is not critical.

Table 1. ADC Dynamic Characterization of One Sample Using Different Clock Sources

Input Signal Frequency (KHz)	Sampling Rate (KSPS)	Clock Setting	ADCLK Frequency (MHz)	SINAD	SNR	THD	ENOB
100	500	Run on clock source 0, Input clock 80MHz	26.67	67.75	69.14	-73.37	10.96
100	500	Run on clock source 6, Input clock 10MHz, PLLCTL3=0x00000700	26.67	68.09	68.77	-76.52	11.02
100	500	Run on clock source 6, Input clock 10MHz, PLLCTL3=0x00000900	25	67.78	69.2	-73.33	10.97
100	500	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20015F00, PLLCTL2=0x3FC00A3D	26.67	65.33	66.23	-72.55	10.56
100	500	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20017F00, PLLCTL2=0x3FC00E3D	26.67	65.82	66.7	-73.14	10.64

Table 1. ADC Dynamic Characterization of One Sample Using Different Clock Sources (continued)

Input Signal Frequency (KHz)	Sampling Rate (KSPS)	Clock Setting	ADCLK Frequency (MHz)	SINAD	SNR	THD	ENOB
100	500	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20035F00, PLLCTL2=0x3FC0043D	26.67	59.97	60.19	-73.03	9.67
100	500	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20015F00, PLLCTL2=0x3FC0DA3D	26.67	62.24	62.68	-72.44	10.05
10	50	Run on clock source 0, Input clock 10MHz	10	67.83	68.83	-74.72	10.98
10	50	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20017F00, PLLCTL2=0x3FC00E3D	26.67	67.74	68.22	-77.51	10.96
10	50	Run on clock source 1, Input clock 10MHz, PLLCTL1=0x20035F00, PLLCTL2=0x3FC0043D	26.67	67.65	68.13	-77.42	10.94

3.2 Trigger Signal

The 12-bit embedded ADC has two trigger modes, software-triggered and hardware event-triggered. If the dynamic parameters (SNR, ENOB, etc.) are important to the application, user must choose the trigger mode and trigger signal carefully to avoid the sampling jitter. For example, suppose the hardware event-trigger is used and the application provides a rising edge of the ADEVT pin to start the conversion, if the triggered signal is not synchronized with the device VCLK, the sampling jitter can be as high as 1 VCLK cycle. This will degrade the ADC dynamic performance quite a bit even if the input frequency is only 10 KHz. On the bench test, the hardware event-trigger and the RTI interrupt is used as trigger source to achieve a precise time stamp to start the conversion.

3.3 Calibration

The ADC internal calibration can be used to calculate the offset error and provide a compensation value for normal ADC conversion. This internal calibration can remove the offset to achieve a lower total error and better absolute accuracy. No extra circuit is required for this calibration. Here is an example of the internal middle point calibration.

```
//Before calibration, the application code should initialize the ADC
//The ADC should use the same settings for calibration and conversion.
//Cal with MidHIGH
//Enable Calibration Mode
plat_adc->adcalcr_un.adcalcr_st.calen_b1 = 1;
//set hilo
plat_adc->adcalcr_un.adcalcr_st.hilo_b1 = 0;
//set bridge enable
plat_adc->adcalcr_un.adcalcr_st.bridgeen_b1 = 0;
Sum_Cal_Data=0;
for(k2=0;k2<8;k2++)
{
          //start calibration conversion
          plat_adc->adcalcr_un.adcalcr_st.calst_b1 = 1;
          //wait until calibration is finished
          while(plat_adc->adcalcr_un.adcalcr_st.calst_b1 != 0);
```

```
            //read back result
            Conv_Data = plat_adc->adcalr_un.adcalr_st.adcalr_b12;
            Sum_Cal_Data=Sum_Cal_Data+Conv_Data;
    }
    //Cal with MidLow
    //set hilo
    plat_adc->adcalcr_un.adcalcr_st.hilo_b1 = 1;
    {
            //start calibration conversion
            plat_adc->adcalcr_un.adcalcr_st.calst_b1 = 1;
            //wait until calibration is finished
            while(plat_adc->adcalcr_un.adcalcr_st.calst_b1 != 0);
            //read back result
                Conv_Data = plat_adc->adcalr_un.adcalr_st.adcalr_b12;
            Sum_Cal_Data=Sum_Cal_Data+Conv_Data;
    }
    //At this point, the ideal Sum_Cal_Data should = 0x8000
    //To divide 16 should be (Sum_Cal_Data+0x8)>>4,
    Sum_Cal_Data=(Sum_Cal_Data+0x8)>>4;
    Cal_ADC=0x0800-(int)Sum_Cal_Data; //Calculate the compensate offset
    plat_adc->adcalr_un.adcalr_ul=Cal_ADC; //write the offset into the Cal register
    //Disable Calibration Mode
    plat_adc->adcalcr_un.adcalcr_st.calen_b1 = 0;
    //set hilo low
    plat_adc->adcalcr_un.adcalcr_st.hilo_b1 = 0;
    //set bridge enable low
    plat_adc->adcalcr_un.adcalcr_st.bridgeen_b1 = 0;
    //set cal_st low
    plat_adc->adcalcr_un.adcalcr_st.calst_b1 = 0;
```

The ADC offset is temperature dependent. It is recommended to run periodic internal re-calibration to remove temperature dependencies. Figure 12 shows the offset calculated by internal calibration of the worst device among 100 devices we characterized. Based on this data, the internal calibration shall be executed every 10 ˚C to avoid temperature dependency greater than 1 LSB.

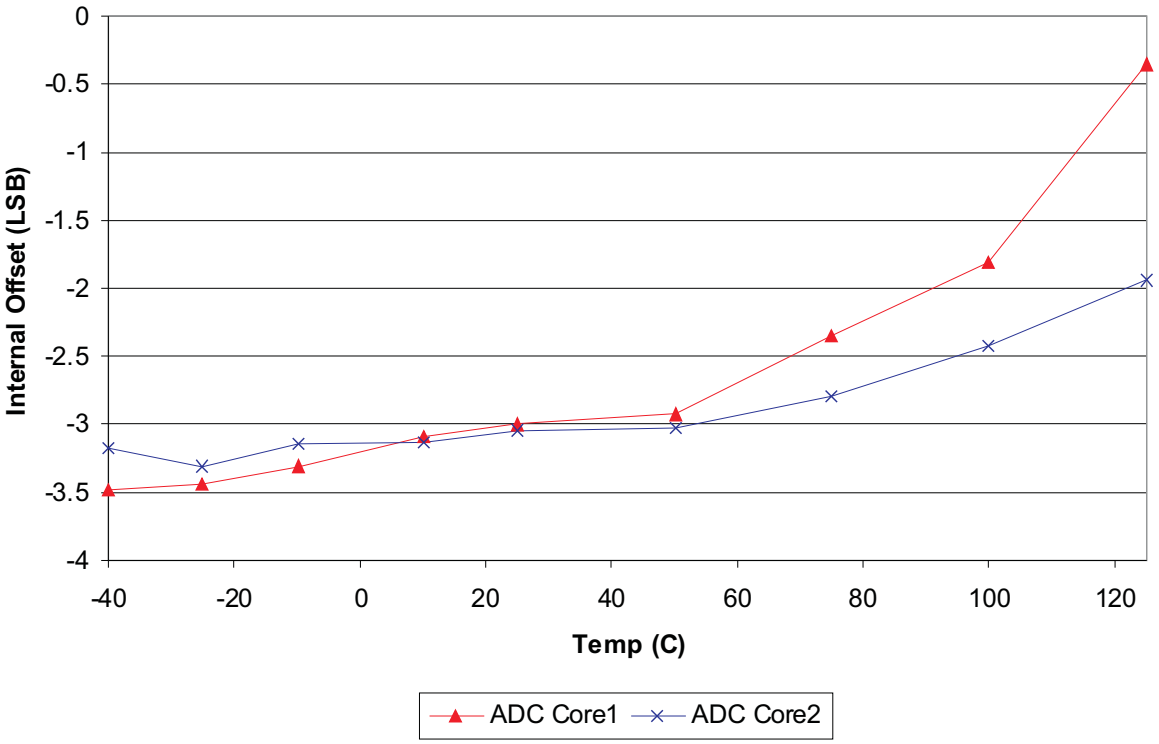

Figure 12. Internal Offset versus Temperate

3.4 Over-Sampling to Improve Resolution

Due to the quantization noise, sampling jitter, distortion and other noise sources, the ENOB of our 12 bit ADC is less than 11. However, over-sampling can be used to improve the resolution as follows:

1. Sampling an analog signal at a much higher rate than twice the input signal frequency.
   Suppose the highest frequency of the input signal is f_{in}, the ideal lowest sampling frequency should be f_s=2 f_{in}. By sampling at k·f_s, the noise band expands k times and the signal-to-noise ratio (SNR) keeps the same as shown in Figure 13.

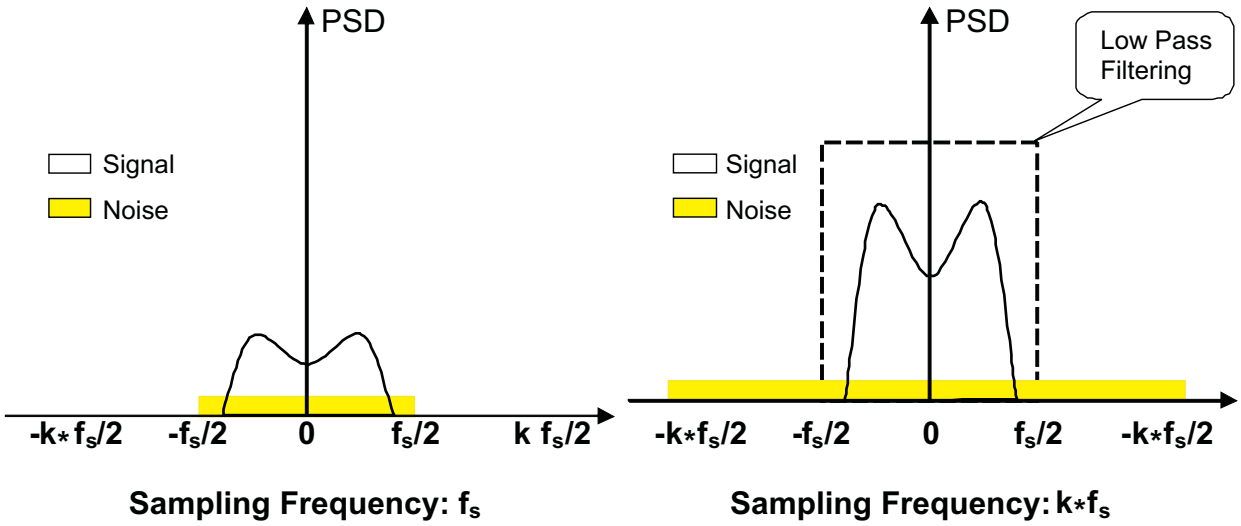

Figure 13. Power Spectral Density w/o Over-sampling

2. Filtering the samples with a digital low-pass filter
   By applying a digital low pass filter with a cut-off frequency at $f_s/2$, ideally, the SNR is improved $10\log_{10}K$ dB and the ENOB is improved $\log_4 K$ bits. However, this method doesn't mitigate the harmonic distortion introduced by the ADC as much as it mitigates the random noise (for example, if the digital filter cut-off frequency is 100KHz, it can filter the harmonic distortion of a 100KHz signal very well, but it can not filter the harmonic distortion of 10KHz well). The improvement on SINAD is less than the $10\log_{10}K$ dB.
   This device doesn't have an On-chip programmable digital filter. The CPU must handle the filtering. Therefore, the digital filter has to be chosen carefully as a trade-off between ADC performance and CPU load.
   The digital filter settling time, in other words, the delay introduced by the digital filter has to be considered by the application. Usually, a higher order digital filter means more computation time, longer delay and better noise ejection.
3. Reducing the sample rate by decimation.
   Ideally, this step does not reduce the SNR. It could be integrated into the previous step to reduce CPU load.

This method not only improves the resolution of the ADC but also relaxes the requirement on the anti-aliasing filter because the digital filter can remove the noise in the frequency range $[f_s/2\ k{\cdot}f_s/2]$.

4 References

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2. Henry W. Ott, Electromagnetic Compatibility Engineering, Chapter 17 Mixed Signal Layout, John Wiley & Sons, Inc, New Jersey, 2009.
3. *TMS570LS20x/10x Technical Reference Manual* (SPNU489)
4. *ADC Source Impedance for Hercules™ ARM® Safety MCUs* (SPNA118)

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