Application Report

SNOA420A–May 2004–Revised April 2013

AN-1235 Using Smart Charge Sharing to Reduce Power and Boost Column Driver Performance

ABSTRACT

This application report describes how Smart Charge Sharing works, how it differs from other common power saving techniques in column drivers, and how to control Smart Charge Sharing on Texas Instruments FPD33584 and FPD33620 column drivers.

Contents

List of Figures

List of Tables

1 Introduction

As flat panel displays extend to higher resolutions and refresh rates, the performance requirements of shorter line times are in direct conflict with the system designer's power budget requirements. Texas Instruments proprietary Smart Charge Sharing technology is able to reduce power consumption while improving the column driver output performance. When used properly, Smart Charge Sharing can reduce the column driver power by up to 40% and improve the settling time of the outputs.

2 How Smart Charge Sharing Works

Smart Charge Sharing works by redistributing the energy stored in the columns of the TFT liquid crystal display. The columns can be driven halfway to their final value without consuming any power. This is possible because in dot or n-line inversion schemes, half of the columns are driven to voltages above VCOM and half of the columns are driven to voltages below VCOM.

In Figure 1, Figure 2, and Figure 3 below, the basic operation of Smart Charge Sharing is described. In this example, the flat panel display column is approximated as a lumped RC load on the output amplifier of the column driver. For quantitative analysis, the columns should be modeled as a distributed load, but for the purpose of illustrating how charge sharing works, a lumped model is adequate.

Figure 1 shows the situation immediately before the start of charge sharing. Alternating columns are at voltages above and below VCOM, respectively. There are a series of switches within the column driver that are capable of shorting all the columns together. Before charge sharing begins, these switches are all open.

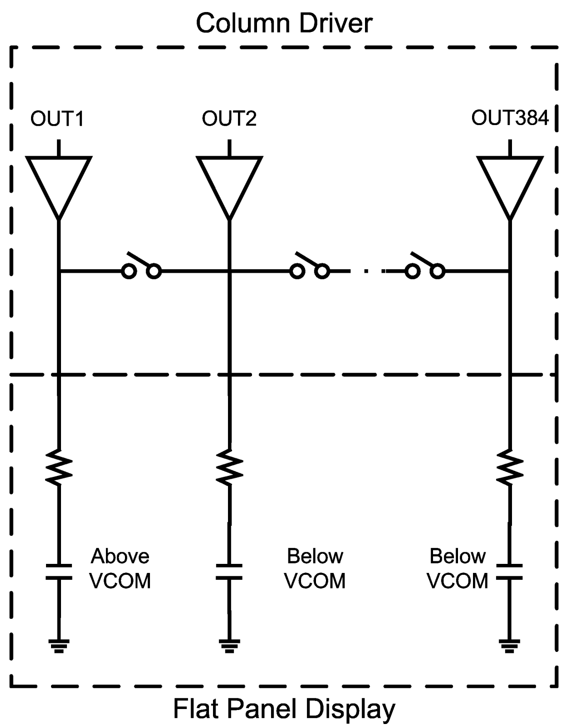

Figure 1. Column Voltages Immediately Before Charge Sharing

Figure 2 shows the situation during charge sharing. The output amplifiers are disabled (in a hi-Z mode) and the switches are now closed. Current flows from the columns above VCOM to the columns below VCOM, as shown by the arrows. During charge sharing, no power is consumed by the output amplifiers.

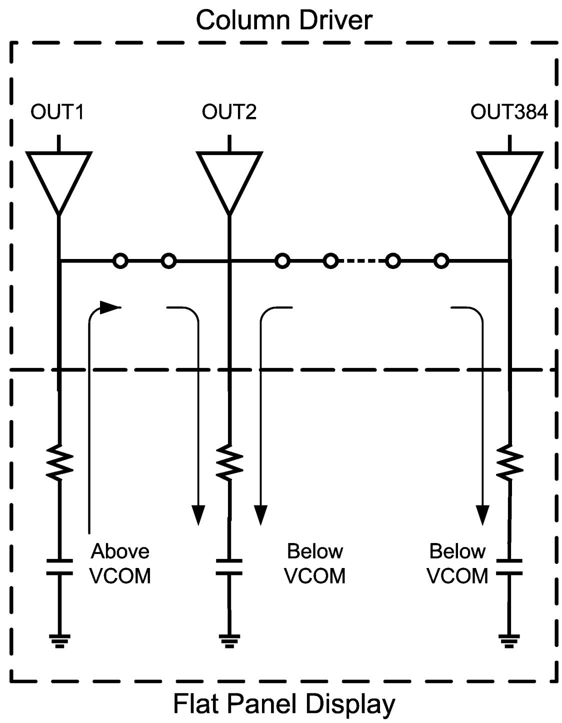

Figure 2. Column Voltages During Charge Sharing

Figure 3 shows the column voltages immediately following charge sharing. The switches are once again open, but all the columns are now at VCOM. It is at this point that the output amplifiers enter the traditional driving state. Note that the outputs only have to drive the columns from VCOM to the final voltage instead of through the entire voltage range.

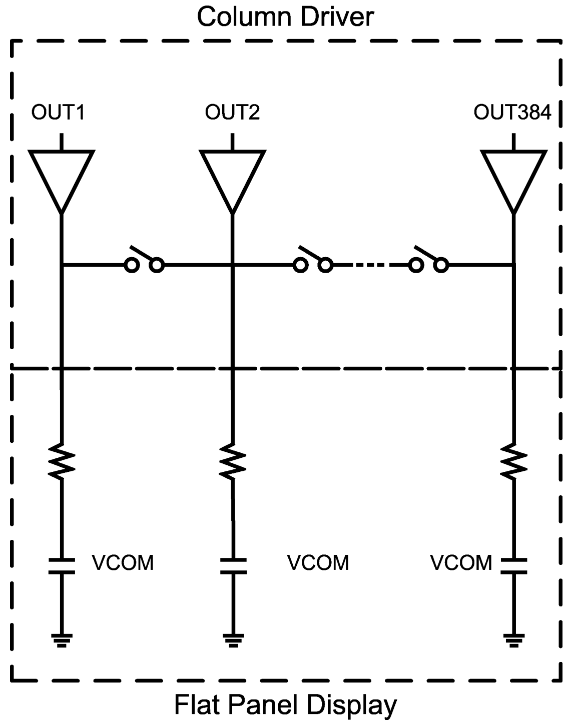

Figure 3. Column Voltages Immediately After Charge Sharing

Smart Charge Sharing also incorporates a monitor for the POL signal. The columns are only shorted together when the POL signal toggles, indicating that the column voltages are changing polarity relative to VCOM. In n-line inversion schemes, the columns do not switch voltage ranges every line. The incorporation of Smart Charge Sharing increases the efficiency of the charge share function.

3 How Smart Charge Sharing Differs from Conventional Drivers

The output waveforms of column drivers using Smart Charge Sharing look different than conventional column driver outputs. Figure 4 illustrates the difference in output waveforms. In both waveforms, VHxx is the output voltage in the upper range (above VCOM) and VLxx is the output voltage in the lower range (below VCOM). The top waveform (a) is a conventional driver output. The slew rate remains relatively constant throughout the voltage range. The bottom waveform (b) is a column driver that uses Smart Charge Sharing. There are two distinct parts to the Smart Charge Sharing waveform. The first is the charge share time. When measured at the output of the column driver, this segment has a fast slew rate before stabilizing at the VCOM voltage. At the end of charge sharing, the output amplifier enters a conventional drive mode and looks very similar to the conventional driver's waveform.

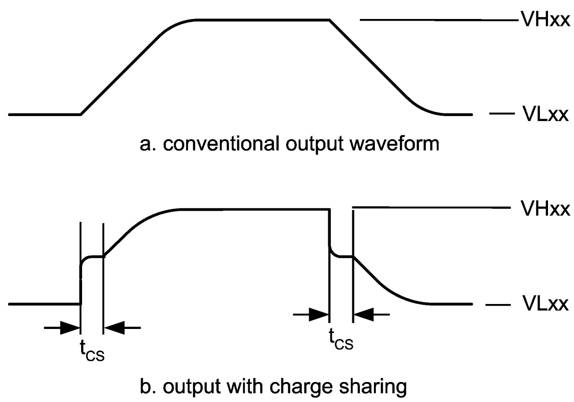

Figure 4. Output Waveforms for a. Conventional Driver and b. Driver Using Smart Charge Sharing

Smart Charge Sharing is also fundamentally different from the other common power saving technique used in column drivers today. Many column drivers available today have a low power option. In most cases, this option reduces the bias current to the output amplifiers in order to save power. The end result is that the overall slew rate of the output also decreases. This is an adequate solution for small panels with light loads and lower resolution, but the performance degradation caused by slower slew rates cannot be tolerated in today's high resolution, high load panels.

Smart Charge Sharing saves power while at the same time increasing the overall slew rate of the panel. This is because the energy stored in the columns themselves can provide a much larger instantaneous current than a conventional amplifier. This allows Texas Instruments column drivers to have higher effective slew rates as well as lower power.

4 How to Use Smart Charge Sharing on the FPD33584 and FPD33620

In order to get the maximum benefit of charge sharing, the charge share time should be set based on the panel loading conditions. Panels with light RC loads can achieve the maximum power savings with less charge sharing than panels with heavy RC loads. Texas Instruments has designed the FPD33584 and FPD33620 column drivers so that the charge share time length can be controlled without external circuitry or additional input pins.

In general, it is recommends using a charge share time of 500ns to 1µs for most panel loads. Heavier loads (for example a panel with an equivalent load of 50kΩ and 150pF) may need a longer charge share time to achieve the maximum power savings and performance advantage. For assistance selecting the appropriate charge share time for your particular application, please contact Texas Instruments.

There are two ways to control the length of charge sharing on the FPD33584 and FPD33620. The control method is defined by three pins(CLK1_SEL, TIME0, and TIME1), all of which can be tied off within the TCP or COF package.

The first method for controlling charge sharing is through the CLK1 pulse width. This method is ideal for customers who want precise control of the charge share time and have the ability to change the CLK1 pulse width. In this configuration, charge sharing begins at the rising edge of CLK1 and ends at the falling edge of CLK1. To enable this configuration, the CLK1_SEL pin must be pulled high through a connection in the TCP or COF. The TIME0 and TIME1 pins should be left floating in this configuration.

A typical output waveform when the charge share time is controlled by the CLK1 pulse is shown in Figure 5.

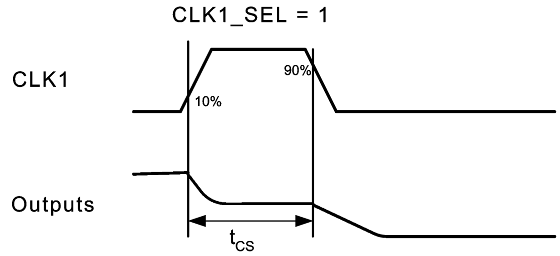

Figure 5. Charge Share Time Controlled by CLK1

The second method for controlling the charge share time is to use a given number of RSDS™ clocks. This method is enabled when the CLK1_SEL pin is either left floating or tied low. The TIME0 and TIME1 pins define 4 options for charge share time length. This solution is best for applications where the CLK1 pulse width either cannot be adjusted or has additional timing constraints that prevent it from being flexible enough to set the charge share time. Table 1 lists the charge share times associated with the different values of TIME0 and TIME1. The recommended use for most applications is [TIME1, TIME0] = [1,0]. Lighter panel loads or slower RSDS™ clock frequencies can also use [TIME1, TIME0] = [0, 1]. The 128 RSDS™ clock cycles option should only be used for panels with very heavy loads. In this configuration, charge sharing begins at the falling edge of CLK1 and continues for the number of RSDS™ clock cycles as defined in Table 1. A typical output waveform is shown in Figure 6, where t_{cs} = (# clocks in Table 1) * (PW_{RSDS})

Note that in both Figure 5 and Figure 6, the waveforms have been exaggerated to better illustrate the different methods of Smart Charge Sharing control. In general, the slew rates during Smart Charge Sharing are much faster than shown.

Table 1. Charge Share Timing Definitions Using TIME0 and TIME1

TIME1	TIME0	Charge Share Time
0	0	16 RSDS CLKs (approx. 250ns at 65 MHz)
0	1	32 RSDS CLKs (approx. 500ns at 65 MHz)
1	0	64 RSDS CLKs (approx. 1µs at 65 MHz)
1	1	128 RSDS CLKs (approx. 2µs at 65 MHz)

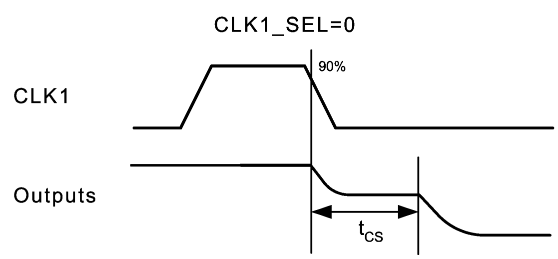

Figure 6. Charge Share Time Controlled by Clock Cycles

5 Summary

Texas Instruments proprietary Smart Charge Sharing technology can improve the performance of column drivers while also decreasing the overall system power consumption. The improvements are accomplished in a design that is pin compatible with a large portion of the RSDS column drivers on the market.

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