Application Report

DS250DF230 Design Considerations for RTV (QFN) Package

ABSTRACT

The DS250DF230 is available in two package variants with identical features sets – BGA and QFN. Of the two variants, TI recommends designing with the latter 32-pin RTV (QFN) package variant due to improved thermal efficiency that improves heat dissipation from the package. This document facilitates design-ins with the recommended alternative QFN package variant.

Table of Contents

List of Figures

Trademarks

1 Introduction

The DS250DF230 is available in two package variants with identical features sets – BGA and QFN. Of the two variants, TI recommends designing with the latter 32-pin RTV (QFN) package variant due to improved thermal efficiency that improves heat dissipation from the package. As a result, the QFN provides superior thermal coefficient performance to facilitate outdoor applications where PCB temperatures may increase up to 105°C.

The DS250DF230EVM is currently only available for evaluation with the BGA package, as the high-speed performance and the feature set is identical between the two package variants. For new designs and existing designs with the BGA package, it is important to account for the differences in pinout, schematic, and layout considerations when transitioning to the QFN package. This document facilitates design-ins with the recommended alternative QFN package variant.

2 QFN Pinout and Schematic Considerations

The following is a detailed comparison of differences between BGA and QFN packages.

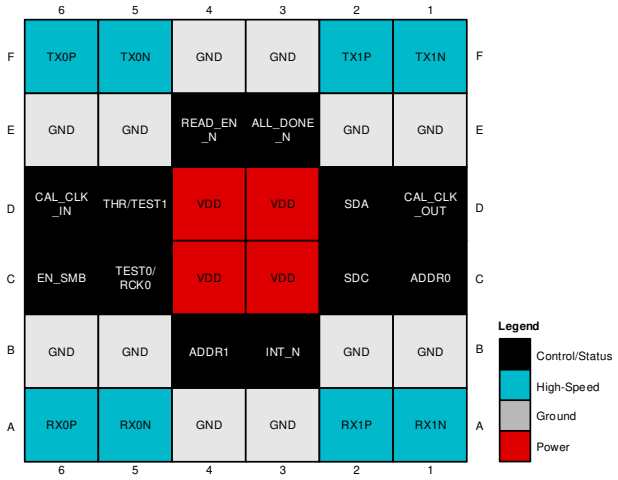

Figure 2-1. ZLS (BGA) 36-Package Pinout

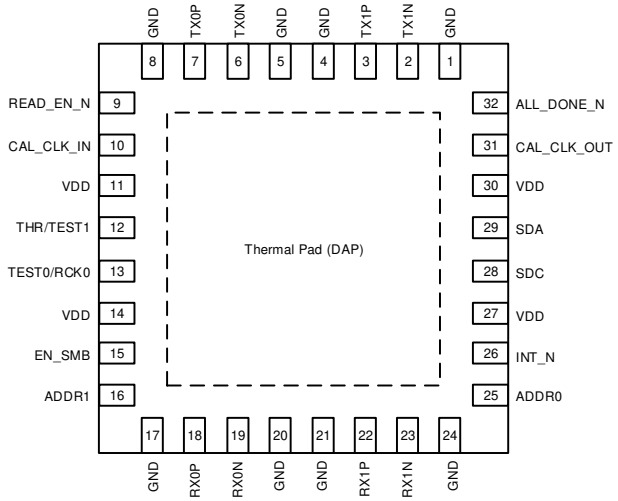

Figure 2-2. RTV (QFN) 32-Package Pinout

There are no differences from a schematic and pinout standpoint in terms of the number or availability of the high-speed, control/status, and power pins. The only difference in pin count is the number of GND connections. There are 12 balls on the BGA package routed to GND. There are 8 pins and a large thermal pad on the QFN package that are internally routed to GND.

3 RTV (QFN) Layout Considerations

The power supply recommendations and high-speed layout guidelines provided in the DS250DF230 data sheet are applicable for both BGA and QFN packages. Details in this section are specific to designing for the QFN package variant.

3.1 RTV (QFN) Footprint Recommendations

- Stencil parameters for the EP (Exposed Pad) such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP (WQFN) package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the EP. Stencil parameters for aperture opening and via locations are shown in the RTV package drawing.
- The EP of the package should be connected to the ground plane through a 3x3 via array. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process. Details about via dimensions are also shown in the RTV package drawing.

More information on the QFN style package is provided in QFN and SON PCB Attachment.

3.2 RTV (QFN) Layout Example

The example layout in this subsection demonstrates how all signals can be routed from the QFN using microstrip routing on a generic multi-layer stackup.

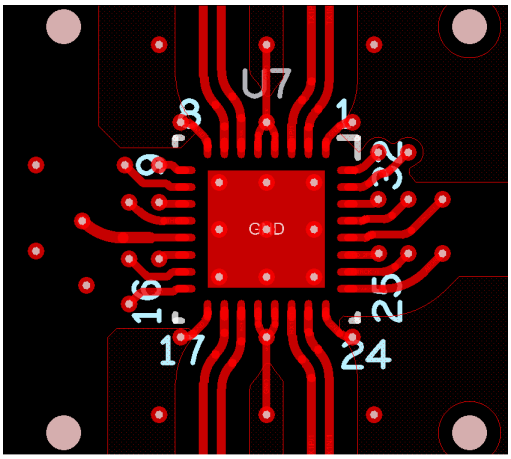

Figure 3-1. Top Layer

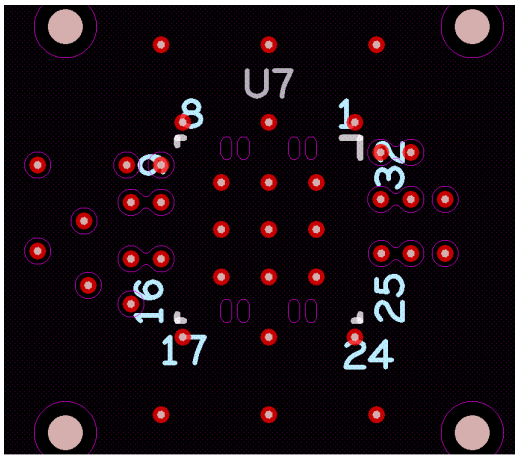

Figure 3-2. Layer 1 GND

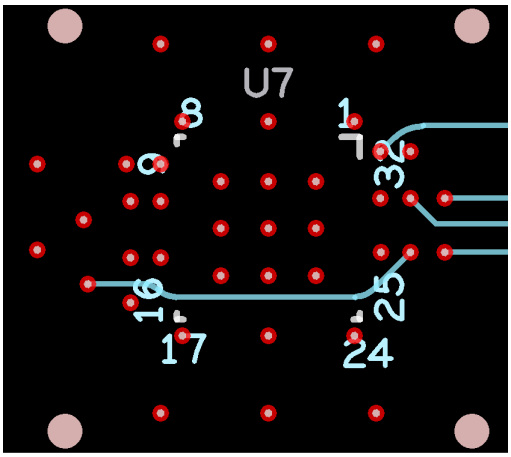

Figure 3-3. Internal Low-Speed Signals

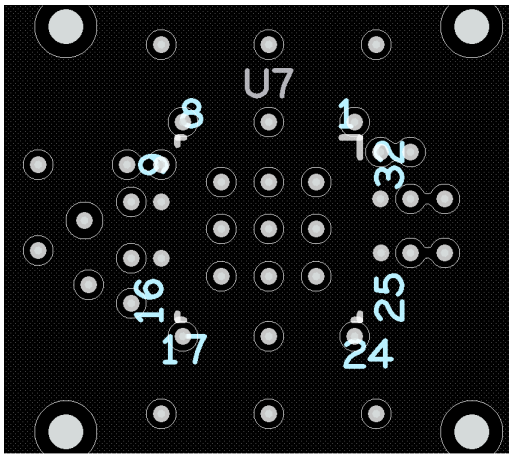

Figure 3-4. VDD Layer

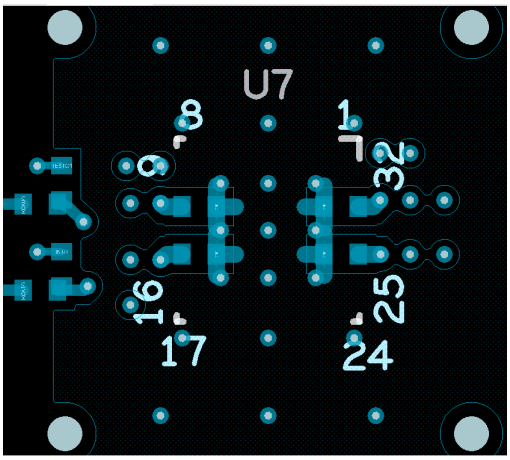

Figure 3-5. Bottom Layer

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