A New Intra-Panel Interface for Large Size/ High Resolution TFT-LCD

Applications

P-40: A New Intra-Panel Interface for Large Size/ High Resolution TFT-LCD Applications

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Abstract

In this paper, we describe a new intra-panel interface designed specifically to meet the needs of the LCD TV market and similar large size/ high resolution TFT-LCDs. We investigate the technical challenges and feature requirements of today's panels that prompted a new look at the panel interface.

1. Introduction

Historically, TFT-LCDs have been used primarily for computing applications. For the past decade, the needs of the data processing applications in notebook computers and CRT replacement monitors have driven the performance requirements of LCD panels. While there are still drivers on cost, power, and mechanical performance, the visual performance of LCD panels has reached a stage where it is good enough for computing applications and there is no significant advantage to improving the visual performance for computing. With the emergence of the LCD TV market, the fundamental visual requirements have changed. No longer are LCDs only expected to meet the requirements of data processing. In LCD TVs, they are expected to deliver a cinema-quality viewing experience equal or better than that of traditional CRTs, projection TVs, or plasma displays. The increased visual performance requirements are driving an all new set of features and techniques that are straining the current intra-panel interfaces.

2. Motivation for a New Interface

The trends in the LCD-TV market are towards larger size panels and higher resolutions to support true HDTV formats. In addition to the size and the data rate requirements, LCD TV is also demanding improved visual performance. This includes improved response time of the liquid crystal, more accurate and stable color temperature, higher contrast ratios, higher brightness, and higher color depth. Of course, these are merely the needs of today. The LCD TV market is changing so rapidly that it is difficult to predict what features and benefits will be needed 1 year from now, much less in 3-5 years.

When we looked at the interfaces of today, we determined that they could be modified to meet most of the needs of the LCD TV market today, but every additional feature was going to further tax the fundamental limit of the interface technology. We decided that continual, incremental modification of the current interfaces was going to be a slow and painful method of keeping up with the needs of the market. What was needed was an interface that started from a blank slate and was developed from the ground up to meet the needs of the LCD TV market of today with an eye on the flexibility that will be needed in the future.

The result was Point to Point Differential Signaling (PPDS™). In developing PPDS, we took the strengths of the current interfaces, specifically the low power, low EMI differential signaling, modified it to be point to point, and added in a higher level protocol to address the advanced features needed today as well as to reserve space and flexibility for the future. PPDS has been designed to be scalable to panel sizes up to 90", resolutions up to and exceeding 1920 x 1080, true 10-bit color, and to be able to easily expand to include features that have not yet been invented.

3. Point to Point Differential Signaling (PPDS™)

3.1 Physical Layer

The physical signaling layer of PPDS is based largely on the signaling levels of RSDS™. Both use a nominal differential swing of ±200mV, both are designed to operate on standard 50Ω transmission lines, and the common mode voltages are largely similar as well (1.3V for RSDS and 0.8V for PPDS). The key signaling parameters are shown below in Table 1.

Parameter	RSDS	PPDS
Differential Signal Level	±200mV	±200mV
Common Mode Voltage	1.3V	0.8V
Typical Output Current	2mA	2mA

Table 1. Comparison of PPDS and RSDS levels

Beyond the signaling levels, PPDS is very different from RSDS. As the name implies, PPDS uses a point to point interface architecture instead of the bus architecture used by most interfaces today. There are several advantages to the point to point architecture. First, the total number of input signals for each column driver is greatly reduced. In a typical 8-bit RSDS system, all 12 data pairs and the clock pair are received by each column driver. In a PPDS system only a single data pair and a clock pair are received. This reduces the total number of clock and data inputs to the column driver from 26 in RSDS to 4 in PPDS. The reduction in the total number of inputs allows the input pads on the TCP or COF to be wider and the overall manufacturing process to be more robust and yield higher.

Figure 1 shows the difference between the point to point architecture used in PPDS (top) and the bus architecture used in most other intra-panel interfaces today (bottom).
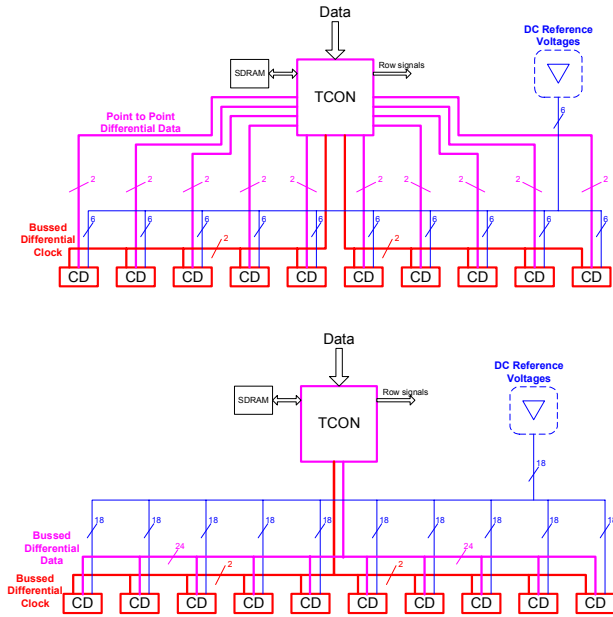
Figure 1. Typical 8-bit panel configurations for PPDS (top) and RSDS (bottom)

The second significant advantage to the point to point architecture is improved signal integrity. In a typical RSDS bus architecture, there are vias and stubs on every signal line where the bus connects to the column drivers. This creates a large number of impedance discontinuities that can cause significant reflections on the bus. In the point to point system, there are no vias and stubs, so the data signal maintains a higher level of fidelity compared to the bus architecture. In addition to eliminating vias and stubs, PPDS allows for simpler impedance control on the signal lines. In a bus architecture, every column driver provides a capcitive load on the bus. The net effect is to lower the effective impedance of the differential signals. In a typical WXGA system, if perfect 50Ω transmission lines are used, we have found that the actual differential impedance is closer to 75Ω than the ideal 100Ω. With a point to point architecture, each differential pair is only connected to a single column driver and the impact of column driver loading is eliminated. This allows PCB engineers to design the trace impedances based on the characteristics of the PCB material and the trace routing without having to estimate and account for the effect of column driver loading. The improved signal integrity allows the data rate to increase for PPDS over traditional bus architectures. Our initial simulations show that the physical interface of PPDS will be able to run up to approximately 400MHz on panel sizes up to 90" in diagonal. This is more than enough margin to accommodate the LCD TV designs of today and into the foreseeable future.

Because of the improved signal integrity, PPDS is readily scalable to higher color depths. With today's interfaces, increasing from 8-bit color to 10-bit color would add additional signals. Because PPDS can operate at high speeds over long distances, there are no system changes required to move from an 8-bit system to a 10-bit system. The interface will need to operate approximately 25% faster, and both the timing controller and the column driver silicon will need to change, but the layout of the timing controller to column driver interface should not change at all. This would include all connectors, TCP/ COF inputs, and trace routing.

As panels grow larger, electromagnetic interference (EMI) once again becomes a concern. We have studied the expected EMI performance of the PPDS interface and we expect that it will be at least as good as today's bus architectures. When compared to all bus architectures, the elimination of vias and stubs is a significant improvement in EMI. Every impedance discontinuity acts as a radiation source. A second major source of EMI in a typical system is the transmitter and receiver circuits in the timing controller and the column driver. The total number of transmitter circuits in the timing controller has been reduced by up to 50%, and the total number of receiver circuits in the column driver has been reduced by over 80%. The third major improvement in EMI is due to the incoming LVDS clock and the PPDS clock operating at different (and non-hamonic) frequencies. This has the effect of lowering the maximum emission peak at the harmonics of the LVDS clock relative to RSDS.

When compared with an RSDS bus, a PPDS interface will run at a faster data rate, which will reduce some of the EMI benefits, but when compared with other common interfaces, such as mini-LVDS, the overall data rates are very comparable. In these situations, we believe that the elimination of stubs and vias and the reduction in the number of transmitter and receiver circuits will result in a measurable improvement in the overall EMI performance.

3.2 Data Ordering and Transmission

Because the PPDS system uses an advanced column driver architecture, the data is formatted differently than in traditional systems.

In most interfaces, the data is sent to the column driver one output at a time. For example, in an 8-bit RSDS system, the first 8 bits of data that are received by the column driver correspond to the complete data word for the first output. Data bits 9-16 correspond to the complete data word for the second output, and so on. In a PPDS system, the data is sent one bit at a time. For a 384 output column driver, transmission begins with a sign bit (transmitted data is 1's complement format) for all 384 outputs. This is followed by the least significant bit for all 384 outputs, and so on through the MSb. This is shown in Figure 2 below.
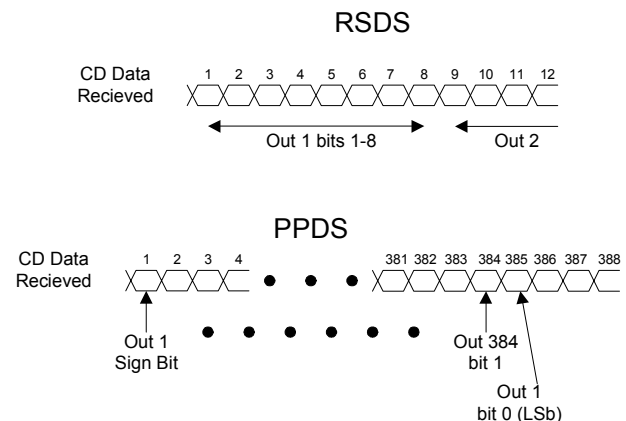

Figure 2. Data formatting for PPDS

3.3 PPDS Protocol

Unlike all of the common intra-panel interfaces of today, the PPDS interface includes a higher level protocol that adds additional benefits to the overall system. The PPDS protocol allows for the elimination of most of the column driver control signals and enables support for advanced features. The total reduction in data signals from an RSDS based system to the PPDS architecture is shown in Figure 3. The overhead of the protocol contributes less than 5% to the overall data rate and does not create any additional system or design constraints on the interface.

Overall, the protocol is split into 5 required intervals and 1 optional interval. All 5 intervals are sent from the TCON to the column driver every line, and each interval either configures the column driver for proper operation or transmits RGB data.
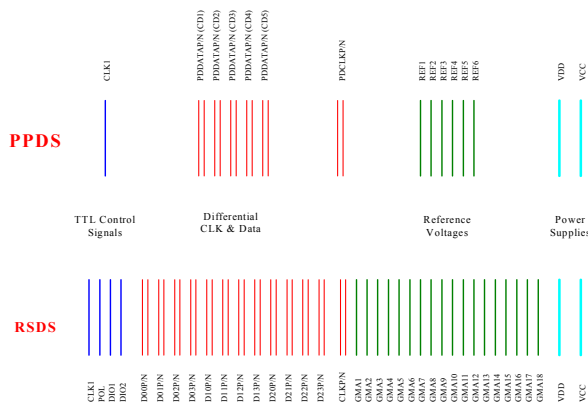

Figure 3. Total number of traces for the PPDS interface compared to RSDS

3.3.1 Interval 1: Data Configuratoin

The data configuration interval allows the embedding of most of the column d river control signals. In this interval, the traditional TTL level signals of POL, INVERT, and SHL along with feature-specific configuration bits. The only TTL signal that is not embedded in the data configuration is the CLK1 signal that coordinates the synchronous driving of the column driver outputs. Embedding control signals within the protocol allows for the reduction in interconnect width, as well as the ability to integrate additional feature support for future application requirements.

3.3.2 Interval 2: Preamble

The preamble is a training sequence that allows each column driver to automatically deskew the clock and data to achieve the most robust data timing. As panels increase in size, the data and clock skew difference becomes large at the column drivers at the end of the panel. For a traditional interface with no preamble and deskew capability, the timing margin can significantly constrain PCB design and drive strength. In systems using the PPDS interface, those constraints are significantly relaxed because every column driver independently deskews the clock and data signals every line.

3.3.3 Interval 3: Data Transmission #1

In this first data transmission interval, the sign bit and least significant bit are sent for every output (a total of 768 bits for a 384 output column driver).

3.3.4 Interval 4: Output Transition

The output transition interval is a break in the data transmission to allow the column driver outputs to enter their driving state. When outputs on all the column drivers begin driving the new data to the panel, the total noise in the system increases dramatically. Typically, this is seen as a relatively large droop in the analog supply (50-100mV), but it also has the possibility to couple into the digital signals and corrupt the data. In order to avoid data errors due to this system noise, the PPDS protocol suspends data transmission during this high-noise time in the line.

3.3.5 Interval 5: Data Transmission#2

In the second data transmission interval, the remaining data bits are sent.

3.3.6 Interval 6: Optional Interval

There is the possibility for the system designer to add in additional clock cycles in order to adjust the overall timing. We expect that most system designers will not need to use this optional interval.

3.3.7 Feature Support

In addition to the reduction of TTL control signals and the improved signal integrity due to the data deskew feature, the PPDS protocol allows for a number of advanced features that are not easily implemented in other interfaces. At the forefront is the ability to extend to true 10-bit color without a change in the overall system architecture. Because the PPDS interface has been designed to meet the frequency requirements of high color depth, high resolution panels, the overall system design can be re-used from today's 8-bit LCD TVs to tomorrow's 10-bit LCD TVs. This gives system manufacturers a faster time to market and a competitive advantage over those who need to support separate system architectures for their 8-bit and 10-bit panels.

There are also control features in the protocol that allow for further customization of the column driver. For example, in order to reduce the total number of part numbers procured, system designers strive to use a single device to satisfy several different designs. Given a 420 output column driver, it can be used as both a 384 output column driver for 15:9 aspect ratio applications and as a 414 or 420 output column driver for 16:9 aspect ratios. Which configuration the column driver should be in can be sent via the PPDS protocol. In fact, the protocol would allow a combination of both 384 and 420 output configurations on the same panel.

The protocol also enables completely new features such as National's Line Delay Compensation which programs each column driver to begin their output drive at a slightly different time. The advantages of Line Delay Compensation are that it can maximize the charging time of the panel by coordinating the column driver output drive to the gate driver propagation delay. A side benefit is that it also decreases the instantaneous current draw on the analog supply because all of the column driver outputs are not changing synchronously. For more information on Line Delay Compensation please refer to Dick McCartney's presentation at this conference.

4.   Conclusion

We have developed a new intra-panel interface specifically designed to meet the needs of the emerging LCD TV market. The physical layer combines the advantages of differential signaling

with a point-to-point data path, providing robust data transmission required to drive large displays. The protocol embeds column driver control within the data interface, enabling support for advanced features while reducing the overall interface width. A complete PPDS system is easily extended to provide control for new features and increased color depth as needed for future generations of LCD TV's.

5.   Acknowledgements

6.   References

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