Distinguished Paper: A Third Generation Timing Controller And Column

Driver Architecture Using Point-to-Point Differential Signaling

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60.1: A Third Generation Timing Controller And Column Driver Architecture Using Point-to-Point Differential Signaling

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Abstract

Many assume LCDs will quickly dominate the TV market by simply scaling existing LCD monitor panels to wider formats (e.g. 16:9 HDTV) and larger sizes. However, a number of TV requirements push beyond the state-of-the-art monitors of today; response time, brightness, contrast, color envelope, color temperature, and progressive scan-and-hold issues require a re-engineering of the monitor solution. Building upon the strengths of National's LVDS and RSDS technology solutions in digital video-data communications, we have created a completely new architecture that fully addresses the needs of TV while supporting existing platforms. The Point-to-Point Differential Signaling (PPDS ^{TM}) architecture is more than a data link between the timing controller and the column driver. It is an architecture that supports very large displays with features like multiple windows each with its own gamma, various gamma optimizations, color balance at every gray level, minimal bezel size, a 30-bit and beyond color path to the display surface, four-color mosaics and numerous other benefits.

1.   Background and History

With each major format advancement in the LCD industry, there has been a complementary, enabling advancement in electronics to mark the way. For example, prior to SVGA (800 x 600) panels, the interconnect between the motherboard and display panel in the notebook PC was CMOS 3.3 or 5V logic. LVDS was developed to address the higher data demands of SVGA requiring a new solution for moving data across the notebook PC (NBPC) hinge with fewer wires and lower EMI. LVDS quickly became the industry standard for the connection to the display panel, and it remains the standard today.

Likewise, the data path between the timing controller (TCON) and the column driver (CD) began as CMOS logic in first-generation displays. RSDS™ technology was introduced circa 1996 as a second-generation technology coincident with the introduction of XGA (1024 x 768) panels for NBPCs. In similar fashion to the benefits that LVDS provided to the connection between the motherboard and display panel, RSDS technology reduced the bezel size, costs, weight and EMI from the data path hardware

between the TCON and column driver CD. Together with RSDS technology, mini-LVDS and other multi-drop bus architectures have formed a class of second-generation solutions, though RSDS technology has become the dominant solution for both NBPC and monitor applications.

Figure 1 illustrates a first-generation, dual-bank, CMOS logic interface. Dual banking was used to cut the data rate in half by providing two banks of data busses, one bus of RGB wires for every other CD. This approach required 36 wires for 6-bit grayscale and 48 for 8-bit. Figure 2 shows the improvement with RSDS technology over this CMOS logic solution in terms of signal wires. The RSDS solution requires only 18 wires for 6-bit and 24 for 8-bit. Both examples are XGA.
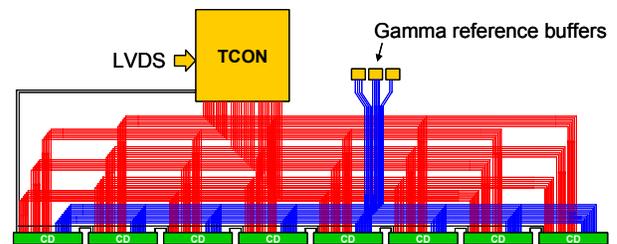

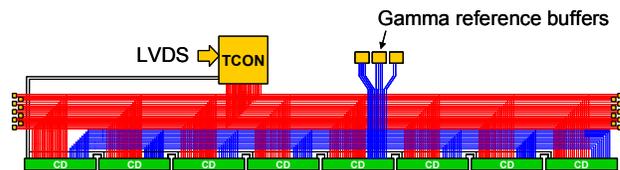**Figure 1.** *1st Generation, Dual Bank CMOS interconnect*

Figure 2. *RSDS™, 2nd GenerationDifferential Bus*

LCD TV brings forward a completely new set of challenges that are broader than simple data signaling issues. The demand for up to WUXGA formats (1920 x 1200) on display sizes beyond 50 inches are problematic for second-generation interconnect solutions. The longer transmission distances (due to the larger sizes) and higher data rates (due to the larger pixel formats) combine to push clock and data registration beyond stable limits. To accommodate these applications, some second-generation solutions have been
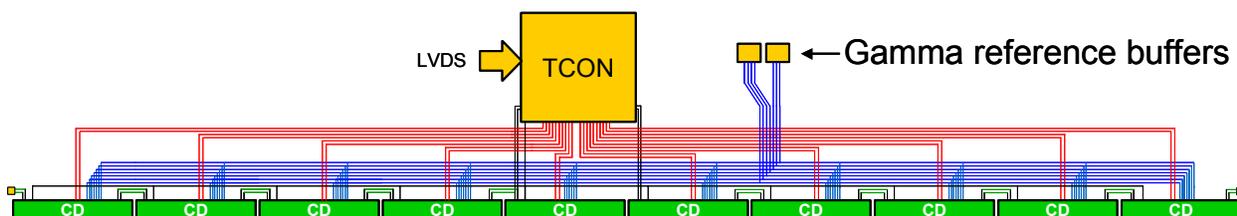

Figure 3. *3rd Generation, Point-to-Point, Differential Signaling (PPDS™)*

upgraded with a cascade alternative in which the bus is received and re-transmitted between each CD to preserve signal integrity.

TV's expanded formats and display sizes, however, aggravate other problems that aren't addressed by improvements in the data path alone. For example, brightness uniformity, temperature-induced gamma gradients and other panel irregularities are much more significant in larger, high-resolution panels. Much of the reason for this is that the transient response of the LCD panel is negligible at low frequencies and over short distances, but is much more of a factor in the display quality when operated at higher frequencies and extending over longer distances. Compensating for the transient effects of the panel requires advanced panel signaling and this signaling is enabled largely through the coordination between the TCON and the CD. The interface between the two includes both data and control signals, and higher performance panel operation places a greater demand on the control dimension of this interface.

The challenges to LCDs from television do not end here. Response time, brightness, contrast, color envelope, color temperature, and progressive scan-and-hold requirements conspire to demand a new approach to the display electronics solution. The point-to-point differential signaling (PPDS™) architecture was developed to accommodate the much-expanded role of the drive electronics needed for advanced displays. It represents a new class of solutions, a third-generation TCON and CD interconnect, with both a data and control link emphasis. Figure 3 illustrates one of the configurations of the PPDS solution for a WXGA panel (1280 x 768 or 1366 x 768) with 8 or 10 bits of grayscale. Comparison with Figures 1 and 2 shows the physical compactness of this approach.

2.0 PPDS™ Architecture

In order to provide a platform from which to significantly advance the performance of the LCD drive electronics system, we have taken two significant departures from the second-generation architecture. The first is an alternate approach to the standard R-DAC column driver. The second is an alternative to the multi-drop bus architecture, replacing it with a direct, point-to-point link between the TCON and each CD.

This PPDS link communicates not only the gray level data, but also contains a header with each display line that controls the driver. This header contains extensions for future features and eliminates the need for additional control signals between the TCON and CD, or between each CD, further simplifying the interconnect. This link forms the centerpiece of the new architecture. It is a single-channel differential pair, a Point-to-Point Differential Signal (PPDS). Figure 4 provides a functional diagram of a typical PPDS solution for a TV or a high-end monitor showing the response time compensation (RTC) overdrive

block integrated with the TCON[1]. RTC accelerates the LCD optical response to allow moving images to appear without smearing, and is a necessary feature of LCD TVs.

2.1 Advanced Column Driver DAC

Prior to about 1994, the LCD industry was in its infancy. A few gray levels (moving from an initial 2 then 4, 8 and eventually 16) were supported using an analog switch multiplexer DAC. This architecture allowed any output to connect directly to any one of the external global references. Because voltages were not buffered at the output of the CD, there weren't any voltage errors introduced, assuring part-to-part uniformity of the output voltage. At the time, output buffer designs introduced far too much voltage error that would appear as a boundary between drivers.

Around 1994, driven by the need for more gray levels for the NBPC application, the CD industry discovered how to design an output buffer that was small, had low offset and gain errors, and used low power. This advancement enabled a transition to the R-DAC architecture used today.
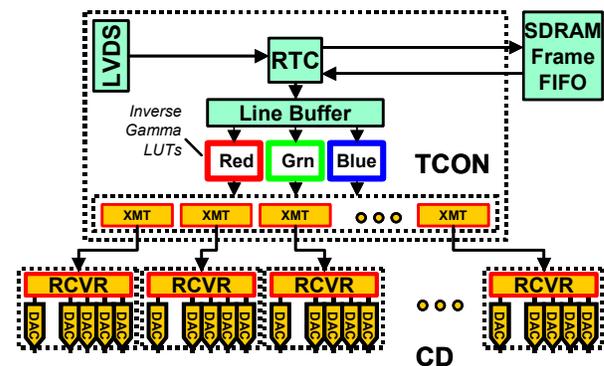

Figure 4. *Typical PPDS™ Functional Diagram*

The R-DAC architecture is a near ideal solution for the NBPC application because it efficiently provides an adequate number of gray levels (64) while intrinsically correcting for the gamma of the display. When all the individual R-ladders of each CD are referenced to the same global voltages, the R-DAC architecture assures identical, part-to-part gray voltages. However, the architecture has its shortcomings when it comes to higher grayscale precision as R-DAC die area grows with the number of gray levels. Because of the higher cost of true 8-bit R-DAC column drivers, the NBPC industry has employed special dithering features in the graphics engine to expand the 64 gray levels four-to-one, achieving an approximate 8-bit gray-level resolution. For monitor applications, where the added performance of true, 256 gray levels is generally required, the 8-bit R-DAC CD is much larger and more expensive than its 6-bit counterpart. Maintaining a low-cost CD driver die while providing up to the 10 bits of

grayscale ultimately required for TV applications, severely strains the R-DAC architecture.

Rather than push the R-DAC configuration into a solution for which it is not well suited, we have chosen to design a different DAC topology into the CD with the advantage of much smaller die size and much more gamma flexibility. Unlike the R-DAC whose non-linear transfer characteristic is hardwired into the resistor ladder, this advanced DAC is linear over its dynamic range. This allows the inverse gamma function to be decoupled from the DAC and placed in a digital look-up table (LUT) in the timing controller, upstream of the column driver. Furthermore, a great advantage of this DAC topology is that the number of bits of grayscale precision does not affect its size, so that progression to 10 bits of grayscale precision does not translate directly into a much larger die-size.

2.2   The Cyclic DAC

The cyclic DAC is elegant in its simplicity. There is much written about cyclic DACs also known as algorithmic DACs[5]. In its essence, the cyclic DAC requires only two matched capacitors and a few switches to implement. Figure 4 illustrates the basic configuration of the cyclic DAC used in PPDS. The general algorithm is to pump charge into or out of C2, cycle-by-cycle, depending on the one and zero content of the digital word being converted. For example, let V_{ref} in Figure 4 be 8 volts and let's convert 101 to a voltage. The binary number 101 is 5 in decimal. This DAC will convert 101 to $5/8^{ths}$ of the 8 bit range, in this example, 5 volts. To begin the output is set to zero by positioning SW1 to ground and closing SW2 and SW3. First the LSB is used to determine whether to SW1 selects V_{ref} or ground. Because it is a 1, SW1 will select V_{ref}, 8 volts. Next, SW2 is closed and 8 volts appears across C1. Next SW2 is opened and SW3 is closed and because C1 and C2 are equal, 4 volts appears across C2 at the output.

The process begins again as SW3 is opened. This time the next more significant bit is a zero and SW1 selects ground. When SW2 is closed, C1's voltage is zero. When SW2 is opened and SW3 is closed the voltage at the output moves from 4 to 2 volts. Finally, SW1 again selects 8 volts because the next more significant bit is a one, C1 has 8 volts until SW2 is opened and SW3 is closed. Since C2 has 2 volts and C1 has 8 volts the resulting voltage is 5 volts ((8+2)/2), the expected value. You can see that the choice of the V_{ref} voltage can be arbitrary and that more bits of precision only requires more DAC cycles rather than additional hardware.

The cyclic DAC is a much better choice of DACs over the R-DAC for the TV application for two key reasons. The small size required for 10 or 12 bit conversions and because it allows the gamma function to be implemented in the TCON rather than hardwired into the CD. In PPDS, we provide a 10-bit linear DAC range for both the upper and lower drive range for an 8-bit gray level system and a 12-

bit DAC (upper and lower) for a 10-bit gray scale system. Additional bits of conversion require only faster conversion rates not additional circuitry. These two bits of guard band allow mapping of virtually any gamma function into voltages in the CD.
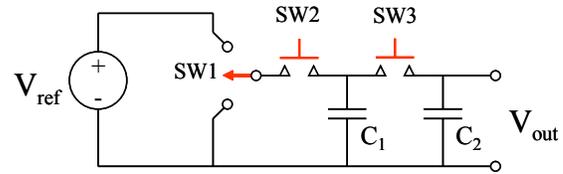

Figure 4. *The simplified cyclic DAC*

2.3   Point-to-Point Architecture

The point-to-point architecture has several advantages over the multi-drop bus. Because the point-to-point connections to the column driver operate simultaneously rather than being time-multiplexed over a common bus resource, the data rate to the CD is typically an order of magnitude slower than the burst rate on the multi-drop bus. This slower, more continuous data flow allows the digital-to-analog conversion to occur over a longer, more continuous time, enabling the cyclic DAC column driver.

Another major advantage of the point-to-point architecture is its tolerance to imperfections in the continuity of the characteristic impedance of the interconnect link. Multi-drop busses are intolerant of partial reflections because these reflections produce different results at different points along the path. Because there are receivers distributed along the path, these reflections limit the data rates of the link or impose impractical levels of fidelity in the link characteristic impedance. Furthermore, each stub from the bus to the receiver contributes to the reflections on the bus. With point-to-point signaling, only one receiver exists on the link and it is located at the point of termination. Consequently, the point-to-point link can be operated at much higher data rates than the equivalent multi-drop bus. The point-to-point link can also be self-terminated, requiring no additional resistors.

It should be noted that the PPDS link can stand alone or can be cascaded through each CD. While cascading is not required to improve the signal fidelity of the PPDS link, cascading does provide a method to connect all the CDs through line-on-glass signal paths for applications where chip-on-glass (COG) and wire-on-array technology is practical and advantageous.

The point-to-point architecture does require a line buffer in the TCON, but this small overhead is more than offset by the advantages of the PPDS system and in particular, the smaller die size of the CD. One of the key benefits of the advanced DAC used in the PPDS CD is that a high-voltage, 8- or 10-bit PPDS CD will be substantially smaller than its 8- or 10- bit R-DAC counterpart.

3.0 Benefits of PPDS Architecture

Unlike second-generation solutions, the PPDS architecture is more than a physical signal path between the TCON and the CD. It is an architecture that enables further innovation to address the needs of today's displays as well as displays of the future. There are numerous benefits of the PPDS architecture, and a number are summarized below:

3.1 Independent Gamma LUTs

One key benefit of the PPDS architecture is the fully programmable, independent gamma. Because the CD provides a linear DAC, the conversion from incoming gray level to outgoing digital voltage takes place in a LUT in the TCON, rather than being hardwired in the CD as it is today. This allows the TCON to be designed to compensate for any display transfer function for any number of display colors. It even allows for the four-color mosaics such as RGBW or for mosaics that allow two or more colors to share a single column line such as the Pentile mosaic.[2,3]

3.1.1 Independent RGB Improves MVA

Providing independent RGB gamma tables allows the TCON to precisely correct the color temperature of each gray level in, for example, a vertical alignment display panel.[4] MVA panels are used in monitor and TVs because of their wide viewing angle benefits. However, one weakness is that the gamma transfer characteristics for each color are slightly different. Independent RGB gamma LUTs allow each color to be gamma corrected independently, providing constant color temperature across all gray levels and extending the acceptability of the technology into higher-performance applications.

3.2 Programmable Header Reduces Discrete Control Signals

The communication protocol between the TCON and CD includes a header transmitted at the start of every display line. This header controls CD features that are conventionally controlled by discrete control signals such as shift direction or the output polarity. It also contains fields to specify, for example, the amount of time that the driver is in the charge-sharing state at the start of each line. Charge sharing is a feature used to recover energy from the panel and thereby reduce the power and heat from the CDs. The header contains a field to control the number of outputs per CD used in the case of a driver having various output formats such as 384 and 414. Some field definitions of the header are overlaid with others to allow compacting of data. These field definitions vary line-to-line to provide a lower control rate for features that change infrequently.

3.3 Reducing Scan-and-Hold Effects

This flexible header feature of the PPDS protocol supports future needs and optimizations that may be required. For example, the progressive scan-and-hold aspect of an LCD requires special treatment to prevent the loss of image quality compared with scan-and-erase technologies such as CRTs and plasma displays. This self-erase feature prevents part of the previous image frame and part of the new image frame from being simultaneously present on the display. PPDS fully supports a self-erase Black Frame Insertion.

3.4 Thinner Bezels and Lower System Costs

The PPDS architecture has been designed to minimize the wires required between the TCON and CD while increasing the data and control information that flows. The PPDS link that connects the TCON to each CD is capable of more than 600 M-bits per second supporting up to WUXGA (1920 x 1200). WXGA (1280 x 768) requires less than 200 M-bits per second. The PPDS, two-wire differential link signals at equivalent levels to RSDS signals, but doesn't require external termination components, enabling both COG and low-cost PCB interconnects.

The I/O to the CD is minimized in every way with the PPDS architecture. Because the CD does not use an R-DAC, it does not need the up-to-20 gamma reference voltages that are used to tune the gamma curve. Instead, rather than the limited control that gamma tuning provides, the full gamma shape is available in the LUT in the TCON. A maximum of 6 reference voltages are required for the PPDS linear DAC, and these references can be buffered internally or externally depending on the CD design and application.

4. Conclusions

The PPDS architecture is a new generation of LCD panel electronics that provides the performance and flexibility required by the rapidly growing flat panel television and monitor markets. The architecture is based on a new point-to-point differential signaling structure that minimizes wires and silicon size. Its many important end-user benefits include thinner bezels, fully programmable gamma, great color uniformity across wide temperature ranges, cinema quality (30 bit) grayscale and lower system costs.

5. References

[1] R. I. McCartney, A Liquid Crystal Display Response Time Compensation Feature…, SID Symposium Digest, XXXIV, Page 1350, 2003

[2] Lee, B. W. et al, TFT-LCD with RGBW Color System, SID Symposium Digest, XXXIV, Page 1212, 2003

[3] Brown Elliott, C. H. et al., Co-Optimization of Color AMLCD Subpixel Architecture…, SID Symposium Digest, XXXIII, Page 172, 2002

[4] Lee, Seung Woo et al., Driving Scheme for Improving Color Performance of LCD's…, SID Symposium Digest, XXXIV, Page 344, 2003

[5] R. Jacob Baker, David E. Boyce, Harry W. Li. *CMOS: Circuit Design, Layout, and Simulation*. IEEE Press/John Wiley, August 1997

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